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Air Force Avionics Laboratory

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NEW SOLID STATE DEVICES II

MICROWAVE INTEGRATED CIRCUITS

MICROELECTRONIC MEMORIES

DESIGN AND PRODUCTION OF HIGHLY ACCURATE AND STABLE SURFACE WAVE BARKER CODE CORRELATORS

T.M. Foster
C.R. Vale
R.L. Thomas

Westinghouse Defense and Electronic Systems Center

ABSTRACT

A very stable and precise 30 MHz, 13-bit Barker code correlator has been developed for radar pulse compression. The correlator uses X-propagating surface waves on an ST-cut quartz substrate with Al transducers. A study was performed to determine the factors affecting repeatability of the center frequency. The frequency was set to an accuracy of 1 KHz by making a series of slightly different photoreductions of a master transducer pattern and selecting the reduction which yielded the desired frequency. In production quantities the center frequency has been repeatable to ± 5 KHz by carefully controlling the orientation of the photomask with respect to the crystal axes. Frequency deviation over the temperature range of -40°C to +90°C has been less than 2 KHz. By accurately controlling amplitude, frequency and phase, a 22 dB ratio of correlation peak to maximum sidelobe level has been achieved compared to a theoretical maximum of 22.28 dB.

INTRODUCTION

This paper describes the development and production of 30 MHz 13 bit Barker code surface wave correlators to replace correlators (or decoders) consisting of 13 bulk wave delay lines for pulse compression in three production radar systems. The Barker code is generated in these systems by an electronic encoder which operates independently of the decoder, and hence, the frequency of the decoder must be independently adjusted to that of the encoder. For proper target detection these systems require at least a 21 dB ratio of correlation peak to maximum sidelobes, compared with a theoretical maximum of 22.3 dB for a 13 bit Barker code. In addition, the decoder is required to maintain this 21 dB ratio over a temperature range of -40°C to +90°C. In order to achieve this performance, the correlator must have transducers with very accurate and stable amplitude, frequency and phase responses.

FREQUENCY CONTROL

We have found in practice that in order to obtain a 21 dB ratio of correlation peak to maximum sidelobes, the center frequency of the decoder must be within approximately 8 KHz of the frequency of the encoder. This can be seen in Figure 1, which shows the response at the center frequency and at 9 KHz away from the center frequency. The correlation peak does not decrease significantly at 9 KHz off the center frequency but the valley between the peak and the first sidelobe increases until it is higher than the first sidelobe, decreasing the peak to sidelobe ratio to 21 dB. Figure 2 shows further degradation of the peak-to-sidelobe ratio as the frequency deviation increases. The response for frequency increments of approximately 16 KHz is shown starting with the center frequency at the bottom. The sidelobes increase rapidly and the main lobe decreases until the peak-to-sidelobe ratio reaches unity at approximately 35 KHz off the center frequency.

In order to allow for possible frequency errors within the radar systems other than those due to the decoder, the frequency deviation limit for the decoders was set at ± 5 KHz instead of the ± 8 KHz required for the system. To obtain a device with a center frequency within ± 5 KHz of the desired center frequency, the following procedure was used: The original photomask was made on a computer-controlled plotter at 20 times the estimated final size. Since the velocity of surface waves on the quartz used was not known to the desired accuracy, the exact photo reduction ratio could not be determined without making devices and measuring the center frequency. The camera was set for a reduction of 20:1 and a series of photo reductions was made near this setting by moving the camera mount in small increments to produce slightly larger and smaller reductions, corresponding to frequency increments of approximately 0.05%. Devices were made with each mask and checked for frequency of best correlation. These data points were used to plot a rough curve of frequency vs. camera setting. Then another series of masks was made with 0.01% frequency increments and centered at the camera setting nearest 30 MHz. One of these masks was usually the final mask for making the decoders in production.

DEVICE DESCRIPTION

A photograph of the decoder is shown in Figure 3. The launching transducer has 7 pairs of interdigital aluminum electrodes and the receiving transducer has 13 sets of 7 pairs, each in the appropriate position to yield the phase relationship necessary for decoding the Barker coded signal as it propagates along the surface. The substrate is X-propagating ST-cut quartz. This cut was chosen because it has a surface wave velocity which is nearly constant over the temperature range of -40°C to +90°C. Figure 4 shows that the peak-to-sidelobe ratio is greater than 21 dB over the temperature range of -60°C to +100°C, which is a wider range than the system requirement.

The quartz substrate is glued to a printed circuit board to aid in assembly into a package. Gold leads are bonded to the aluminum transducer pads using thermocompression bonding. The other end of the lead is bonded to the printed circuit board which is, in turn, connected to hermetically sealed pins mounted in the package. Transformers are used at the input and output to match the impedance of both transducers to 75 ohms. A metal shield is placed above the substrate to prevent electromagnetic feedthrough from the input to the output, which produces a spurious signal. A metal lid is solder-sealed to the package to prevent long term degradation of the performance due to corrosion of the aluminum or condensation of water vapor on the substrate.

FREQUENCY ERRORS

The errors inherent in this manufacturing process were estimated in order to determine whether it would be possible to produce decoders at the correct frequency with a high yield.

There are several possible sources of frequency error, which can be classified as either errors in the surface wave velocity or errors in the size of the transducer pattern. Size errors can occur in the photoexposure process and cause the decoder pattern to be longer or shorter than the photomask unless proper care is taken. The use of collimated light greatly reduces size errors, however, and we estimate that the total frequency error due to incorrect size is less than 100 Hz.

Much larger frequency errors can result from having deviations from the correct surface wave velocity. One source of these velocity errors is misorientation of the pattern with respect to the crystal axes. Since the pattern is registered with respect to a reference edge, an error in the orientation of the pattern or the crystal axes with respect to this edge can cause velocity and frequency errors. Our calculations of frequency error show that X-axis misregistration will cause no more than 84 Hz deviation from the desired frequency.

The most serious error occurs as a result of deviation of the quartz crystal's face normal from the desired direction. The surface wave velocity as a function of the direction of the plate normal is shown in Figure 5.[1] ST-cut quartz corresponds to an angle of 132.75° on this graph. The slope of velocity vs. angle at this point is approximately 0.94 meters per second per angular degree. Crystal manufacturers can hold the face normal to ± 15 minutes of arc for substrates cut from different crystals and to less than 15 minutes for substrates cut from the same crystal. This angular error corresponds to a frequency error of 2.3 KHz.

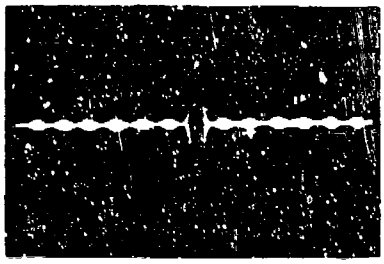
Another possible source of frequency error is the variation of surface wave velocity from one quartz crystal to another due to causes other than axis misregistration, such as impurities in the quartz. Crystal manufacturers do not specify the surface wave velocity to the 2 parts in 10^4 precision required to assure a frequency accuracy of better than 5 KHz out of 30 MHz. However, the velocity uniformity from one batch of quartz to another has been excellent, and less than 10% of approximately 200 decoders made in production to date have been more than ± 5 KHz from the center frequency.

CONCLUSION

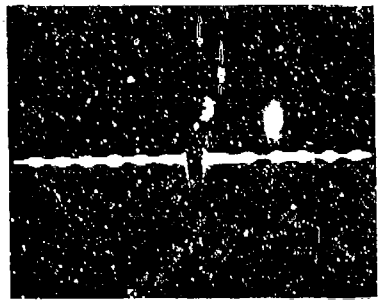
In conclusion, a 30 MHz bulk wave Barker decoder has been replaced in production by a surface wave tapped line decoder which achieves a 21 dB peak-to-sidelobe ratio and a frequency accuracy of ± 5 KHz over a temperature range of -60°C to +100°C.

FOOTNOTES

1. A.J. Slobodnik, Jr. and E.D. Conway, Microwave Acoustics Handbook, Volume 1, AFCRL-70-0264, Air Force Cambridge Research Laboratories, 1970, p. 59.



13 Bit Barker at f_c



13 Bit Barker at f_c + 9 KHz

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Figure 1. Decoder Response When Peak-to-Sidelobe Level Decreases Below 21 dB

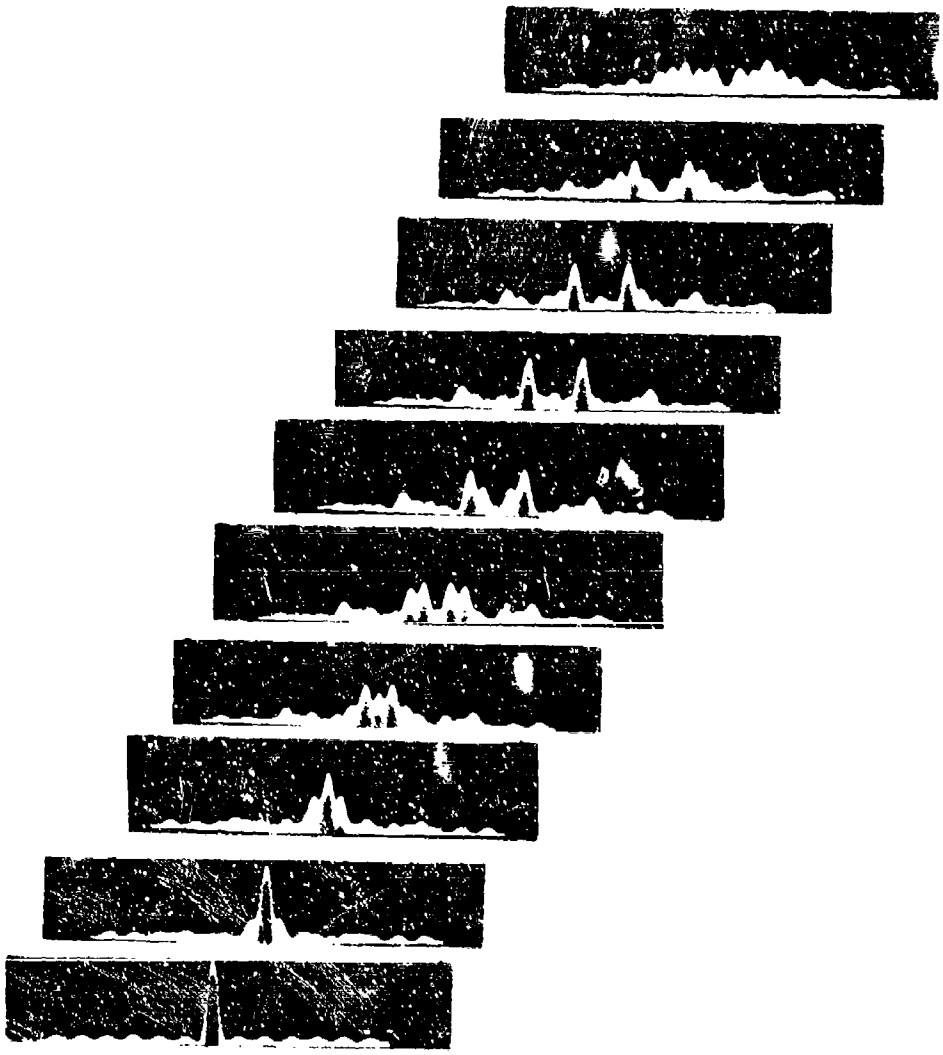

Figure 2. Decoder Response at 16 KHz Frequency Increments

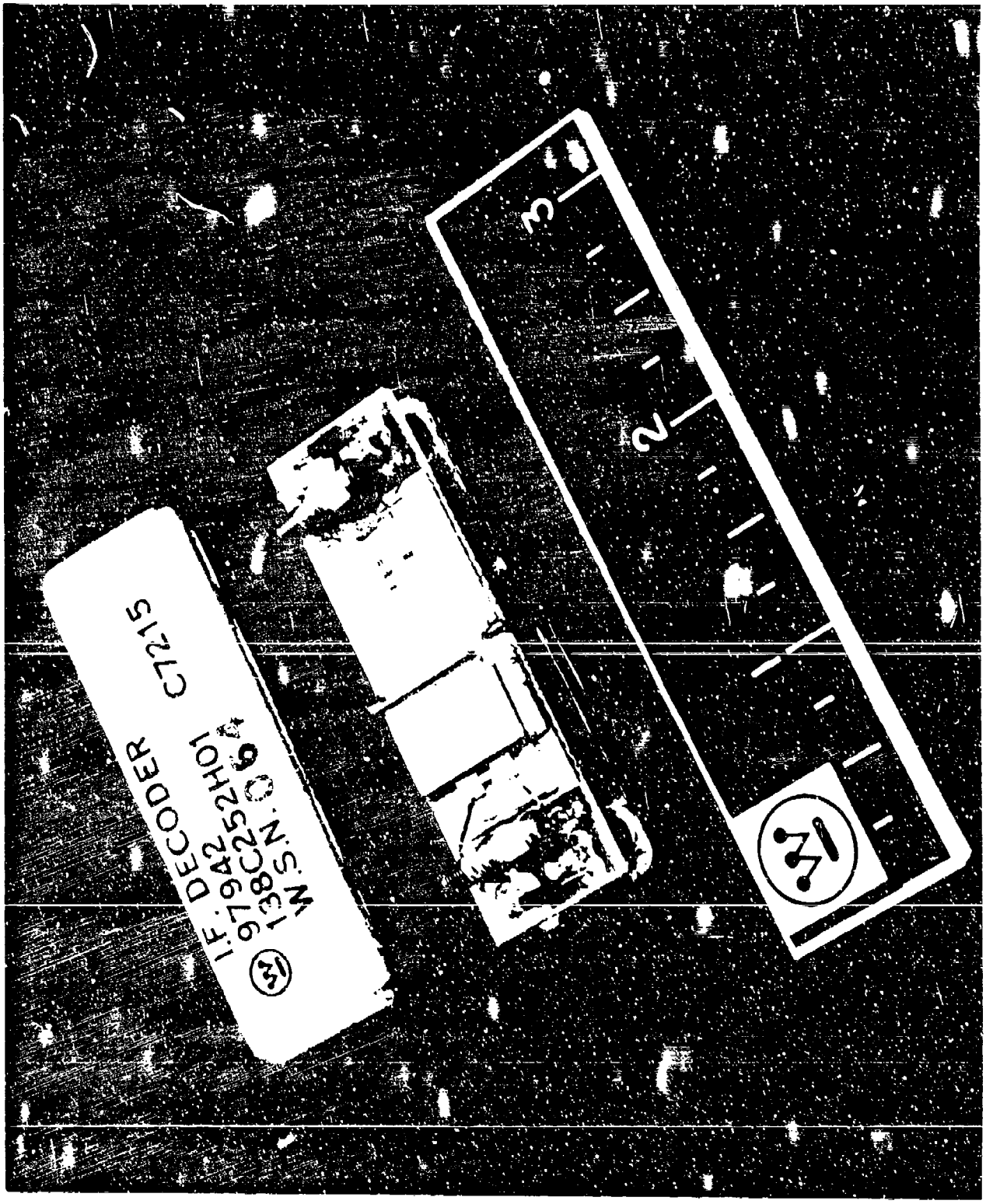

Figure 3. Photograph of Production Decoder

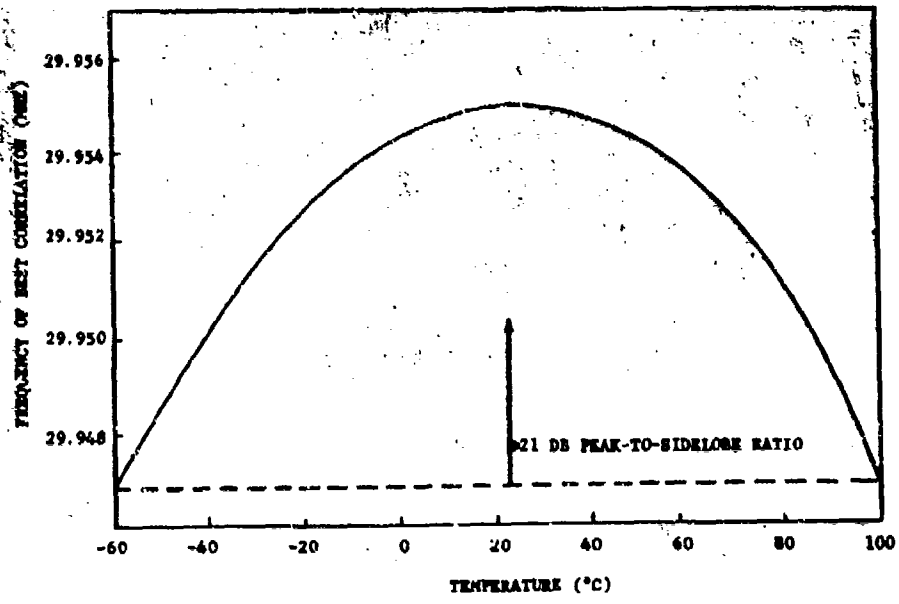

Figure 4. Frequency of Best Correlation Vs. Temperature for ST-Cut Quartz

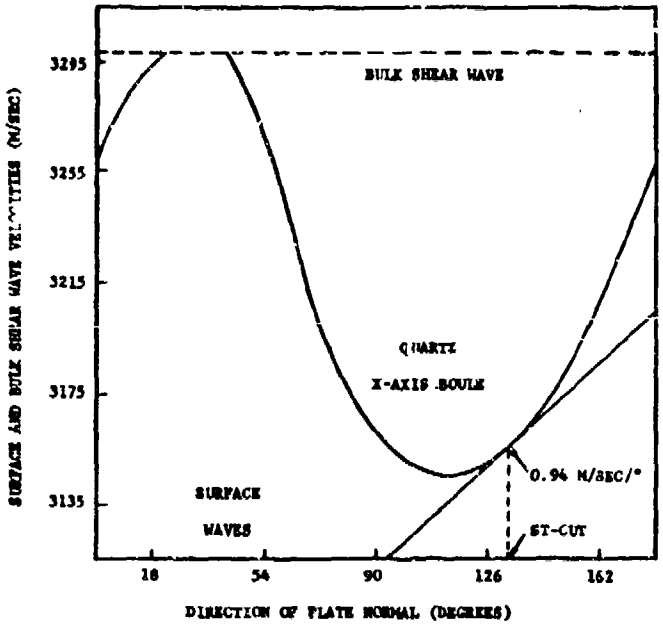

Figure 5. Surface Wave Velocity Vs. Direction of Plate Normal

LOW DISPERSION VHF SURFACE WAVE ACOUSTICAL FILTER

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Systems Development Division

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ABSTRACT

A low dispersion filter has been developed at 70 MHz using surface wave acoustics. The filter has a -0.3 dB bandwidth of 7 MHz and a skirt selectivity which provides a fall-off from -0.3 dB to -35 dB in 2 MHz. Group delay ripple is limited to ± 25 nanoseconds out of a total delay of 2 microseconds. Filter syntheses at other frequencies are easily obtained by using existing computer programs.

Great progress has been made by numerous authors in demonstrating the essential properties of filters utilizing acoustic surface waves. The type filters being discussed are those which consist of a series of interdigital fingers on the surface of a piezoelectric crystal or piezoelectric film on a nonpiezoelectric crystal. The interdigital finger-pairs are spaced on approximately half wavelength centers such that the electrical field structure is in synchronization with the acoustic wave for the center frequency band of the transducer. The geometry of a surface wave filter is such that if the adjacent finger-pairs are of alternating polarities the field lines between the electrodes generate acoustic waves that propagate in both directions underneath either transducer. The secondary transducer thus receives half the energy.

Work has been carried out by different investigators toward providing an adequate description of the surface wave transduction process and characteristics related thereto. Much of this work has been based on the assumption that the energy coupled at each finger-pair is very small compared to the total energy which passes by the transducer. This assumption is the basis for using the impulse response model described by Tancrell and Holland in the March '71 issue of IEEE. This result is identical to that generated previously using an equivalent circuit model by Smith, et. al., in the IEEE Transactions on Microwave Theory and Techniques, 1969. In both cases it was shown that the frequency response of transducers can be represented by a Fourier transform. Much design work has been reported in the literature based on this approach to calculate properties of surface wave acoustic filters.

This approach has succeeded in explaining the major characteristics of surface wave acoustic filters. Perhaps the most desirable characteristics in acoustic surface wave filters is their reproducibility. In principle if a filter of a given bandpass and dispersion characteristic is designed it can be reproduced to an exceedingly high degree of precision at low cost. This should make the filter particularly useful for applications in which a large number of filters are needed. The present design approaches which make use of the assumption that the acoustic wave is sampled lightly at each finger-pair provides an excellent means for achieving gross filter characteristics. It cannot be used to achieve the very low dispersion characteristics which was the objective of the filters to be described. It will be shown that a very pronounced phase shift is due to the loading used to set up the metallic finger pattern. Key deficiencies of the lightly sampled approach are the ignoring of the direct loading of the metallic finger pattern and the periodic loading of the electric circuit.

There are some efforts being expended in order to achieve improved description of surface wave transducers. None have been applied to low dispersion, flat top frequency response, filters. The authors have improved on the lightly coupled sampling approach by creating a periodic loading of the piezoelectric surface. This loading leads to periodicity which causes an attenuation in a portion of the filter bandpass. The presence of the metallic loading leads to a 15-25 nsec time delay discontinuity at the center frequency of the filter. This corresponds to a five degree change in slope of the phase characteristic at the same point.

With very lightly coupled materials, such as quartz, reasonably good results can be obtained using only the impulse model. Properties of quartz can be made relatively insensitive to temperature for appropriate propagation directions. Thus quartz is the clear choice where precise work is desired. This same consideration was involved in the Barker Code Demodulator described in a paper by Thomas, et. al., at the Ultrasonic Symposium in December 1971. The design of that filter required a compensation for a 4 dB attenuation along the length of the filter. Many detailed characteristics of the substrate as well as the synthesis technique must be considered to achieve a good reproduction of the decoded Barker signal.

Since the frequency characteristics can be represented as the Fourier transform of the active finger-pair lengths, synthesis is then based on the following procedure:

(1) Computation of active finger lengths to provide desired frequency bandpass by using an impulse response. For the square frequency response filter this would be a $\frac{\sin x}{x}$ except for the finite length of the transducer. A good approximation is achieved by suitably tapering the $\frac{\sin x}{x}$ time side lobe amplitudes.

(2) Computation of frequency response of two cascaded transducers representing the input and output of the filter. We have used constant finger overlap lengths for the second transducer. (By virtue of reciprocity it is immaterial whether the frequency selective or constant finger length overlap transducer is used as the input or output unless specific matching conditions dictate one arrangement or the other. We shall refer to the frequency selective transducer as the primary and the constant-finger-overlap transducer as the secondary element.)

(3) Optimization of response of two transducers. By virtue of the linearity of the Fourier transform, the active region of the filter is divided into N (N = 100 for our program) "channels" as shown in Figure 1.

Each transducer finger intersecting a particular channel must, because of the interger finger length constraint, launch or receive acoustic waves uniformly over the width of that channel. Due to the assumed linearity of the acoustic medium, the transmission through a single channel is equal to the sum of the transmission between each launching finger edge and each receiving finger edge. Furthermore, because of the assumed nonattenuation of the propagating wave and the assumed equipotential of all conductively connected points, the channel transmission (except for delay) between any launching-receiving pair of finger edges is the same as between any other pair.

The program developed takes each of the 100 channels of the active region in turn, computes the transmission through that particular channel and adds this contribution to a running sum of all channel transmissions.

This arrangement provides for computation of the frequency response of the two transducers as a unit. Optimization was then carried out by letting each finger in sequence occupy a greater or lesser number of channels. The optimization routine stops when no improvement can be obtained by varying the length of any finger.

The remainder of this paper will be a discussion of two filters that were developed with the objective of providing dispersionless operation with steep filter skirts and a nominally flat response. Figure 2 shows the interdigital structure. Quartz was used for the filter, metallization is evident by virtue of the lighter color. The time side lobes of the filter are tapered to an approximate cosine pattern in order to provide an optimum square shape for the frequency response. The detailed taper of the side lobes is modified by the synthesis procedure described earlier.

The properties of the filter are illustrated by Figure 3. This shows the center frequency of 70 MHz with steep filter skirts and low spurious response. The bulk of this spurious response are bulk waves which go through the crystal, reflect and come back to the surface to interact with the secondary transducer. Since these can all be eliminated with surface treatment they will not be considered further here. Figure 4 shows more detailed characteristics of the amplitude response as well as the phase characteristics. Except for a slightly attenuated region in the upper half bandpass this response appears to be that of a reasonably rounded top filter with some minor periodicities throughout the bandpass region. These minor periodicities in amplitudes vary between a tenth and 2/10th of a dB and are largely due to multiple reflections in the crystal. Most of which can be eliminated by proper surface treatment. The triple transit echo can also be suppressed by taking reasonable precaution. It should also be noticed that the phase characteristic is a straight line except for a break at the center and the same periodicities which amount to approximately a ripple of $\pm$ 2 degrees. In addition to these periodicities however, the phase characteristics have a distinct break in which the phase shifts from approximately 7 degrees per MHz to approximately 12 degrees per MHz or a difference of about 5 degrees. Since the phase slope is relative only the difference is significant. This change in phase slope levels to a distinct delay step in the approximate center band frequency of 70 MHz. It should be noted that except for this distinct shift in slope, phase is substantially dispersionless across the bandpass and shows no tendencies to be dispersive even at the band edges.

Figure 5 shows the group delay characteristics of this filter. We can see that there are numerous periodicities with frequencies of 300 and 600 KHz and they can be related to the forementioned effects.

The curved top of this filter was due to the fact the synthesis was carried out ignoring the characteristics of the secondary transducer. Figure 6 shows a flattened top amplitude response by including the secondary transducer in the synthesis. The response is reasonably flat. It should be noticed that the same bulk acoustic wave leakage is evident. Figure 7 shows a more detailed view of the amplitude response and the fine periodicities of the group delay response. They are clearly multiple reflections of both surface

and bulk waves which can be controlled, as mentioned before, by suitable treatment of the surfaces. The large periodicity across the bandpass was a part of the synthesized pattern by virtue of a requirement placed on the program. Thus only the relatively fine periodicities represent deviations from the computed response which is within $\pm$ 1/10th of a dB except as will be shown in the next figure. Figure 8 superimposes the experimental and calculated responses of the filter. The computed response is flat top except for the periodicity mentioned earlier and a slope which represents quarter wave length periodicity of the equivalent circuit. The measured response is in good agreement with computed response below the center frequency. A nonsymmetric attenuation along with the break in the phase characteristics of the previous filter is due to metallic loading of the piezoelectric surface.

The essential effect of the metallic loading can be analyzed by the straight forward development of the propagation constant of electromechanical energy along the periodic transmission structure for which an expression is available, for example, as from Mathai and Young page 385. Figure 9 shows the maximum attenuation versus $\frac{\Delta z}{z}$.

Two curves are shown, one for attenuation in dB per finger-pair and one for 25 finger-pairs. Since the attenuation is due to both primary and secondary transducers, this is typical of the filters described in this paper.

If we take the filter of Figure 3, as an example, Figure 10 then shows that for a $\frac{\Delta z}{z}$ value of 0.11 percent, a reasonably good match with the predicted attenuation is achieved. This figure indicates the size of the attenuation due to the periodic metallic structure. This particular comparison (for $\frac{\Delta z}{z}$ 0.11 percent) appears to agree very well with the computed results. This same figure shows the modified phase characteristic due to the band stops. The five degree per MHz break in phase characteristics is at least reasonably close to the value of four degrees calculated for the above value of $\frac{\Delta z}{z}$. It then appears that the nonsymmetry of the single filter can be explained in terms of periodic metallic loading due to the finger-pairs. It is thus necessary that this periodic loading be introduced into the synthesis process when filters are designed in order to achieve low dispersion surface acoustic wave filters. Based on the results of this study, for instance, if the affected phase break of four degrees is introduced into the synthesis process the residual phase 1 degree break would correspond to the difference between the actual five degrees shown measured in an earlier figure such that the actual break would be 1 degree. Similarly if the attenuation characteristic is suitably synthesized to within $\pm$ 1/10th of a degree a filter reproducible to a $\pm$ 1/10th of a degree should be feasible. With these improvements the surface wave acoustic filter should be amenable to synthesis in many applications requiring a large number of filters with precise reproducibility at a low cost.

It should be noted that the attenuation due to the metalization periodicity is insufficient to explain the difference between the computed and measured bandpass characteristics of the flat top filter (Figure 6). Since the positve slope of this filter is directly attributable to the cross field model, we must directly question the use of this model vs the in-line model for quartz.

Though the cross field model has been shown preferable for lithium niobate, it has not been shown to be viable for quartz.

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1. R. H. Tancrell, M. G. Holland, "Acoustic Surface Wave Filters", Proc. IEEE, Vol. 59, No. 3, pp. 393-409; March 1971.

2. W. Richard Smith, Henry M. Gerard, Jeffrey H. Collins, Thomas M. Reeder, H. J. Shaw, "Design of Surface Wave Delay Lines with Interdigital Transducers", IEEE Trans., Vol. MTT-17, No. 11, Nov., 1969.

3. R. L. Thomas, C. R. Vale, T. M. Foster, "Design and Fabrication of Precise and Repeatable Surface Wave Barker Code Correlators", IEEE Ultrasonics Symposium, Dec. 8, 1971.

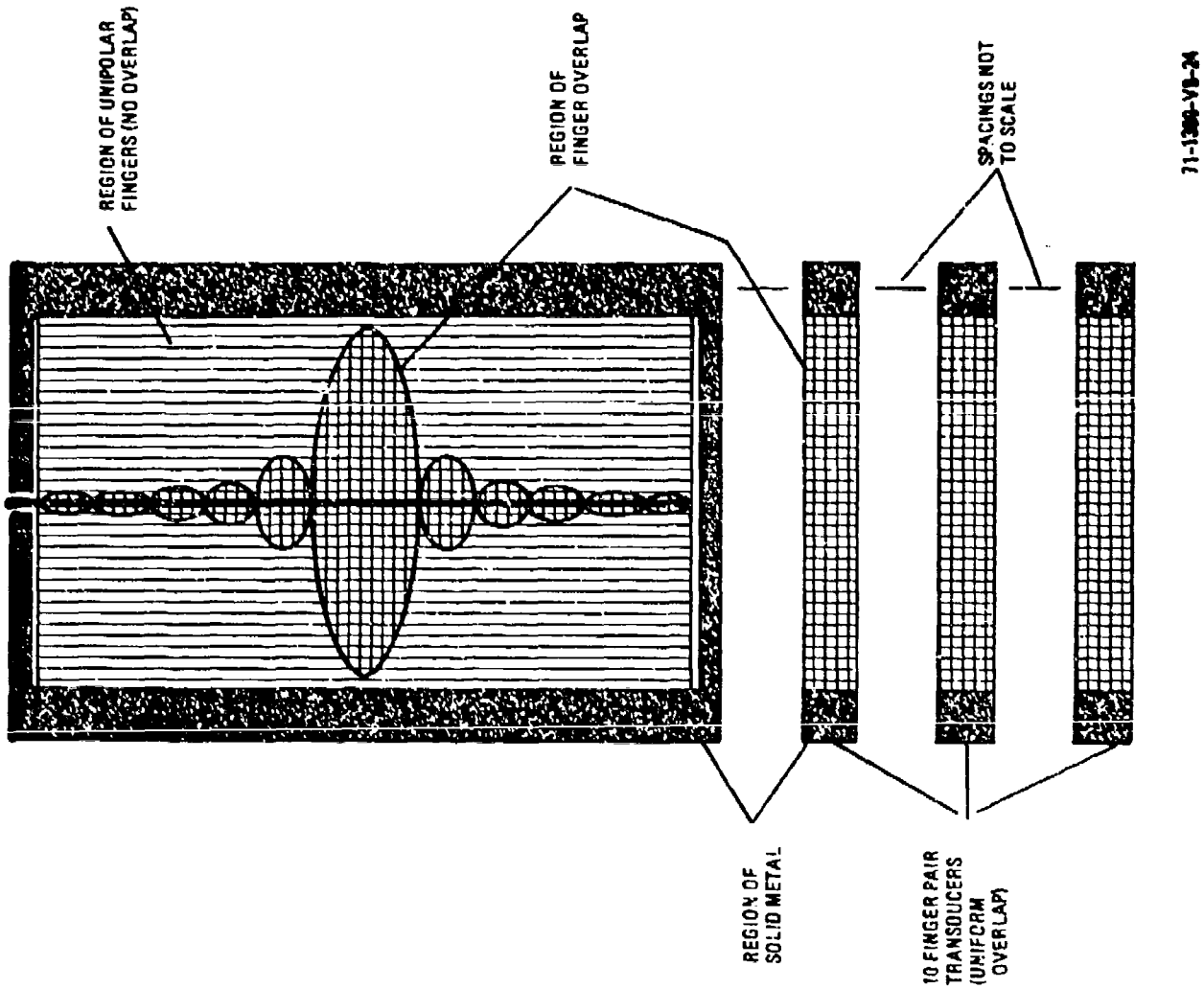

Figure 1: Diagramatic Sketch for Computer Synthesis.

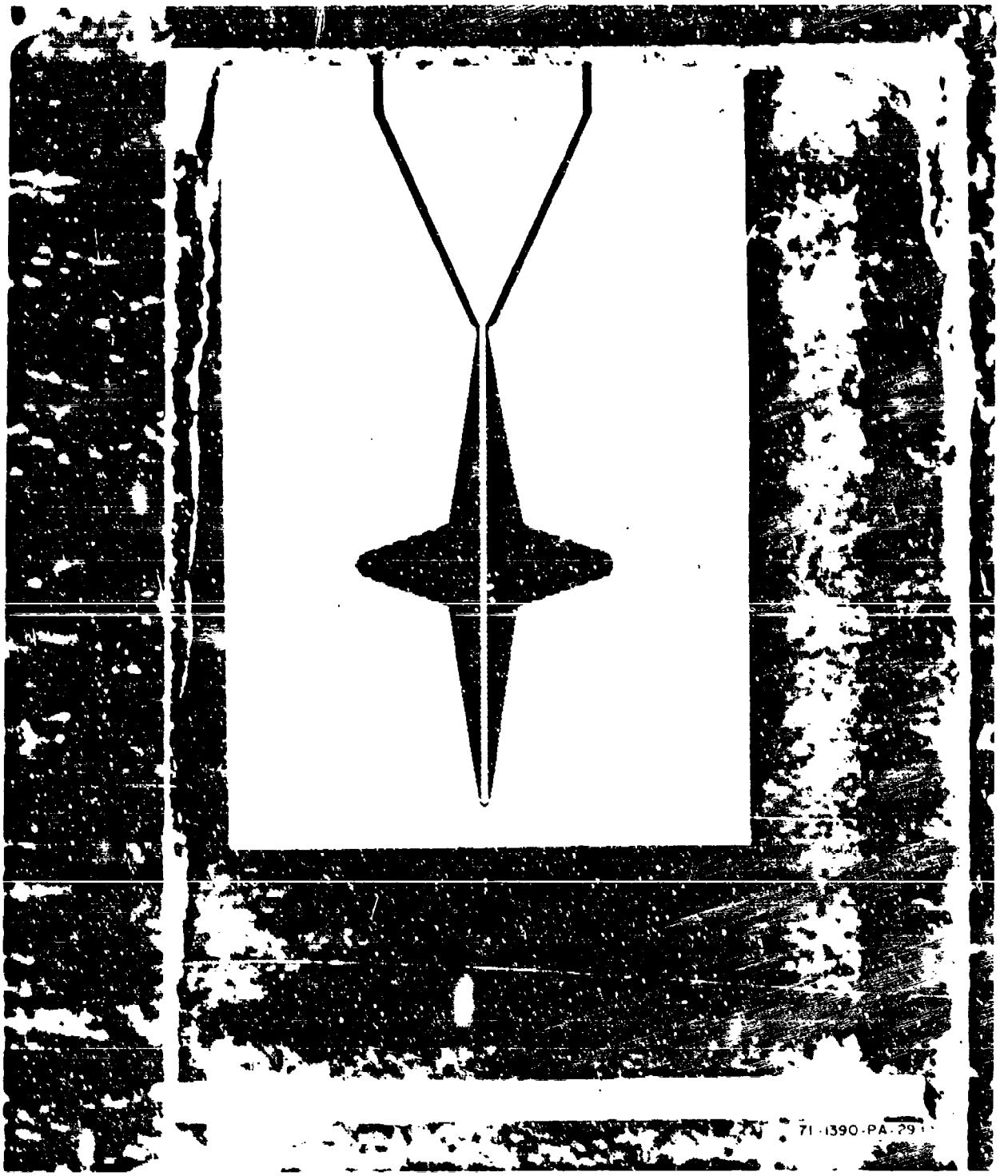

Figure 2: Filter Interdigital Structure (COM 5).

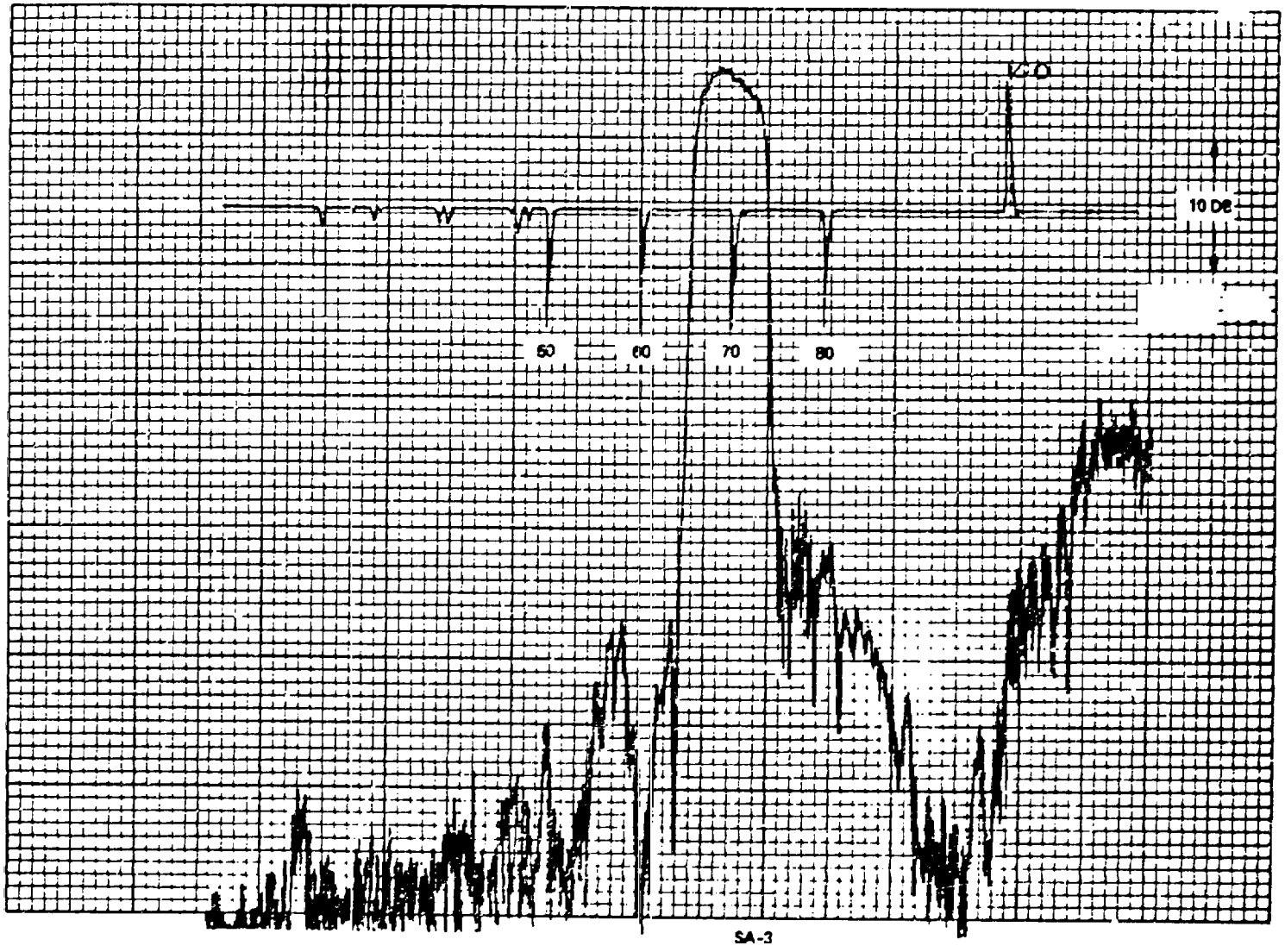

Figure 3: Overall Filter Response (COM 5).

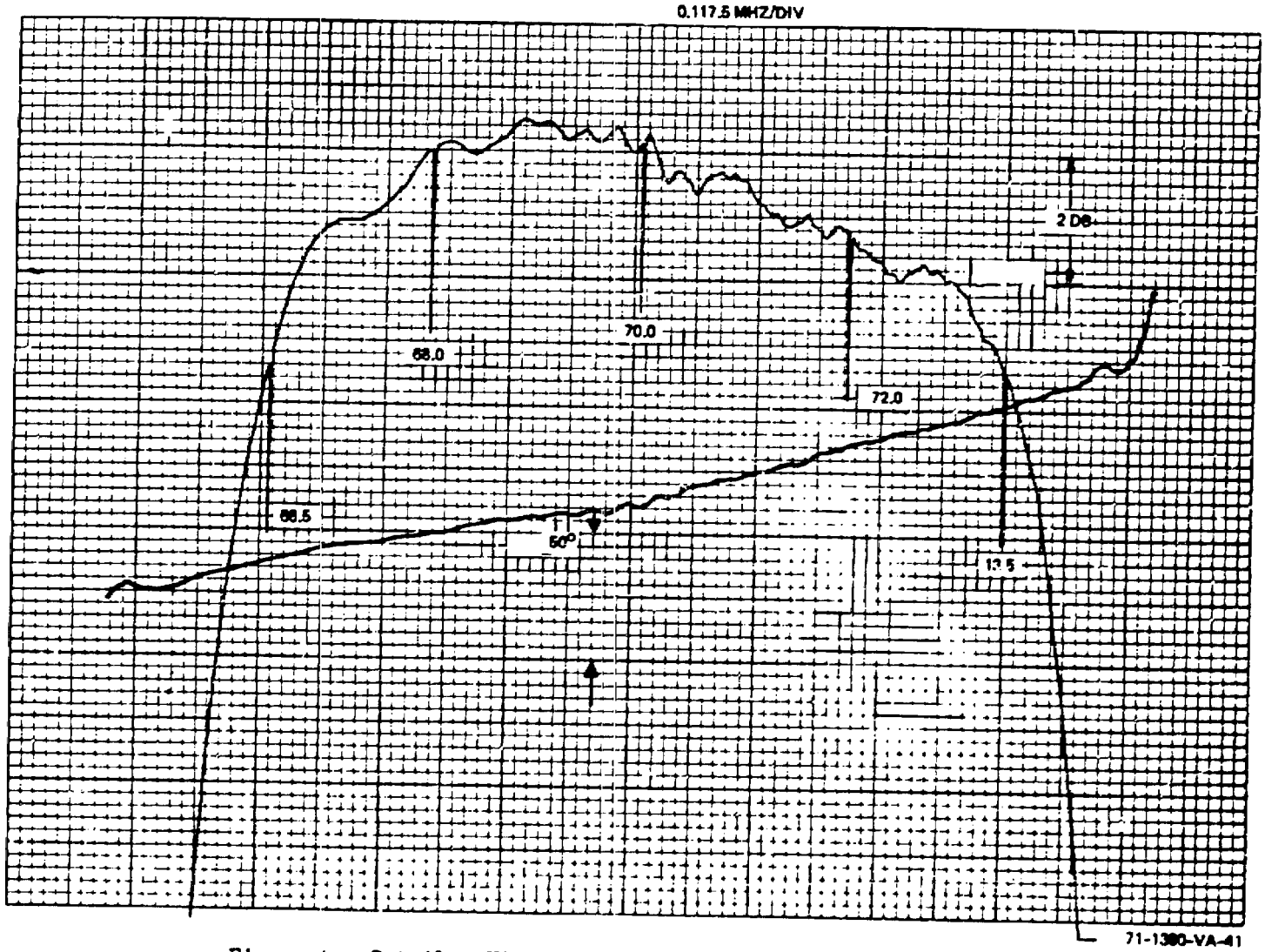

Figure 4: Detailed View of Filter Response (COM 5).

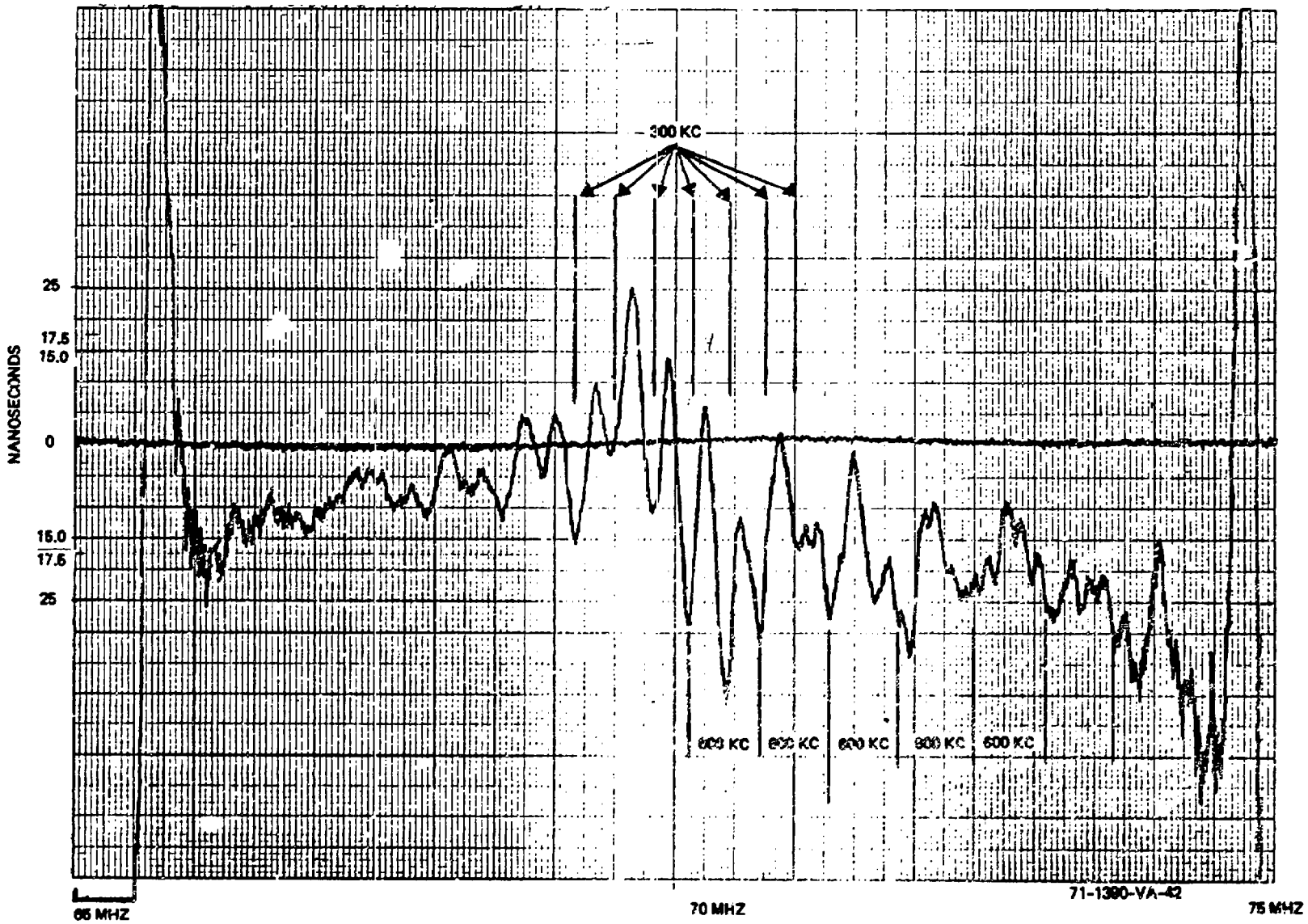

Figure 5: Group Delay Characteristics (COM 5).

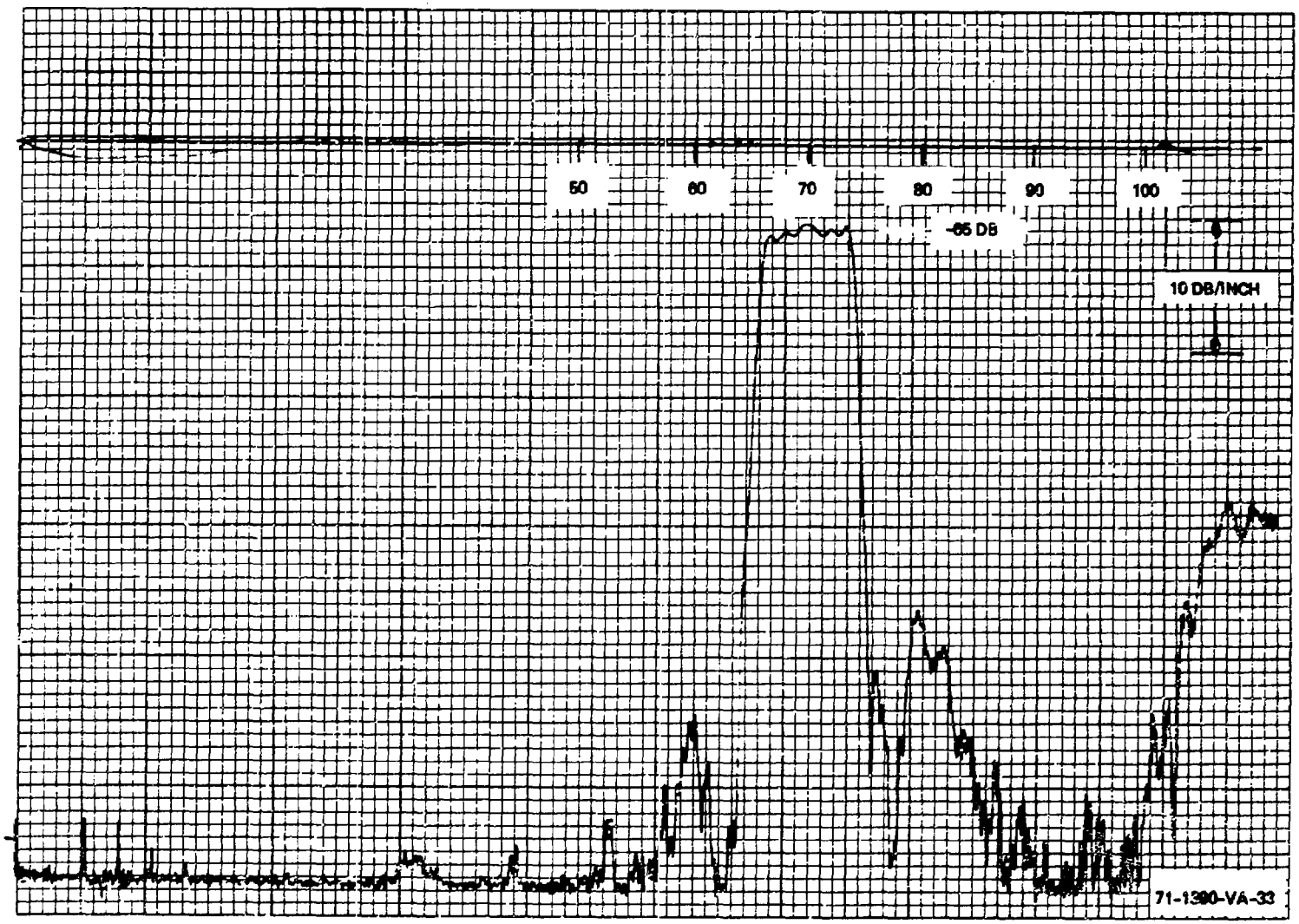

Figure 6: Square Top Filter Response (COM 6).

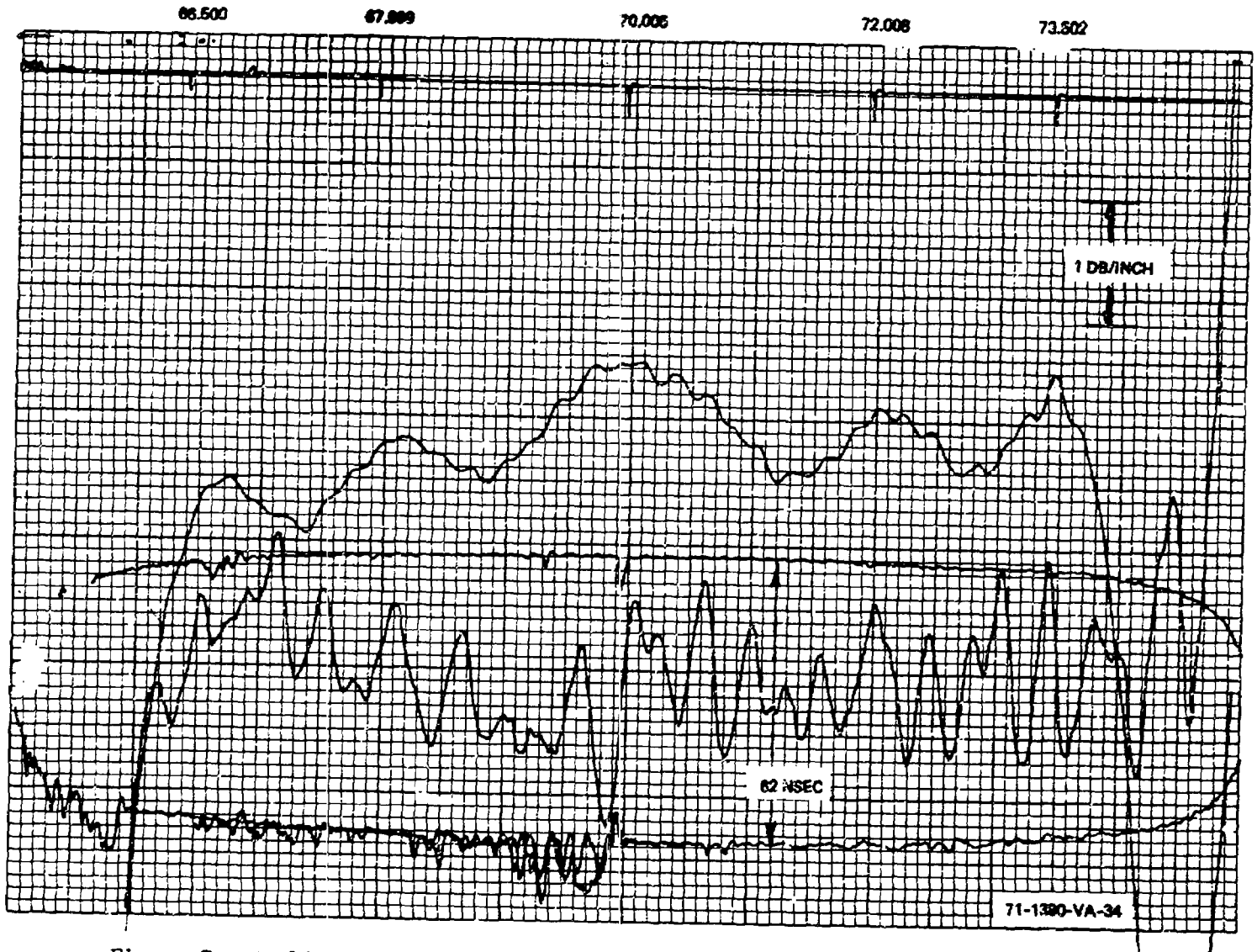

Figure 7: Amplitude and Group Delay of Square Top Filter (COM 6).

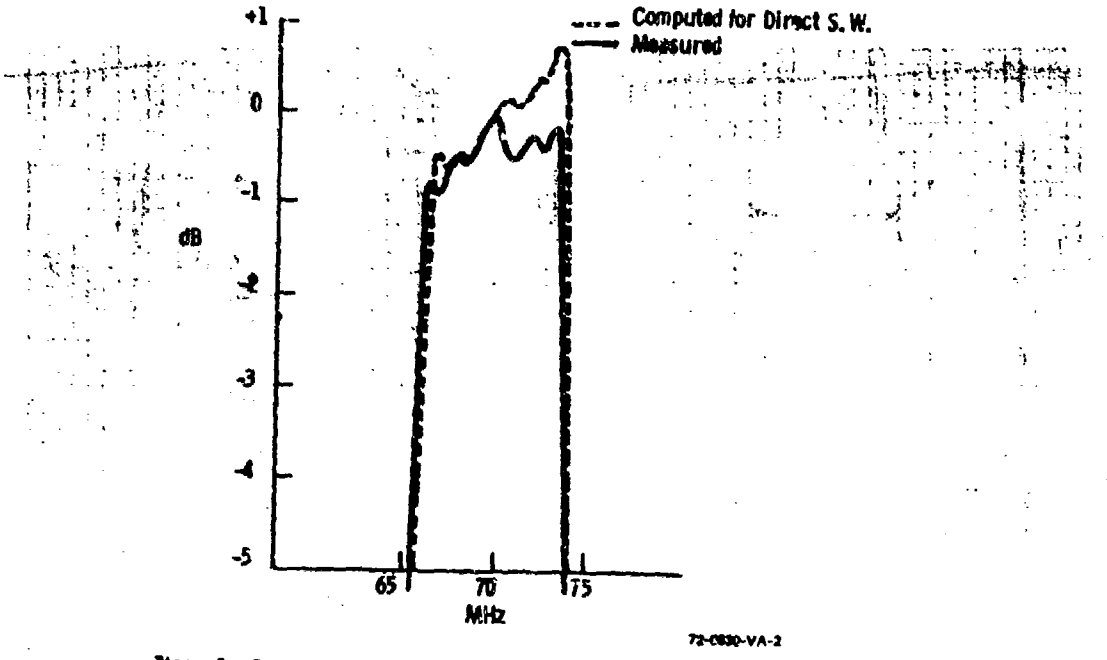

Figure 8: Comparison of Experimental and Computed Filter Responses (CCH 6).

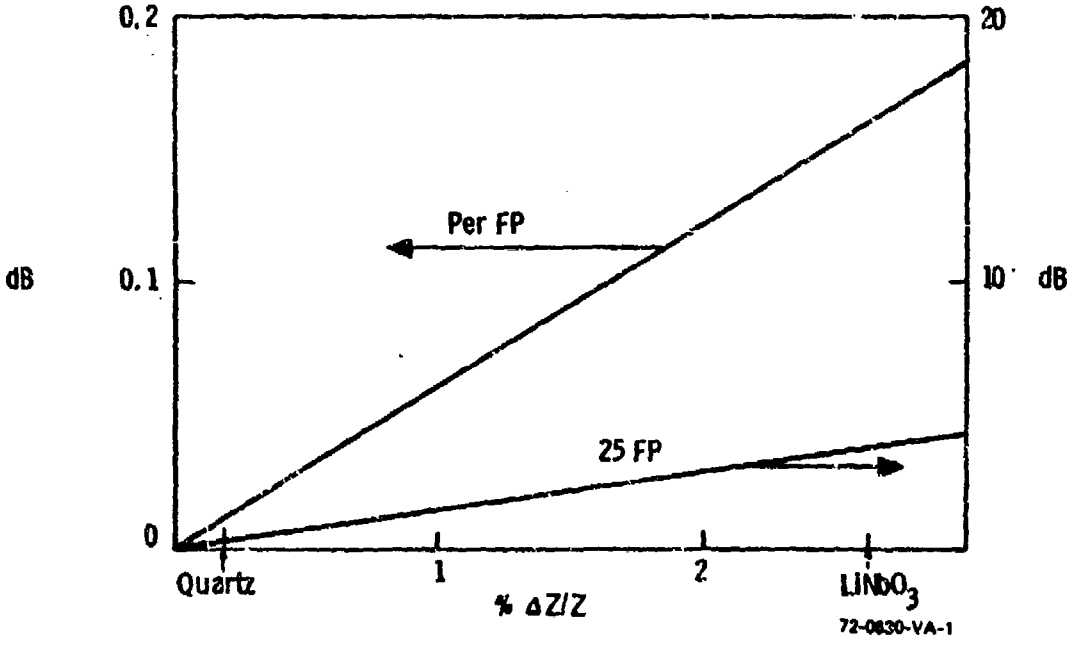

Figure 9: Metallic Loading Attenuation vs. Δ z/z.

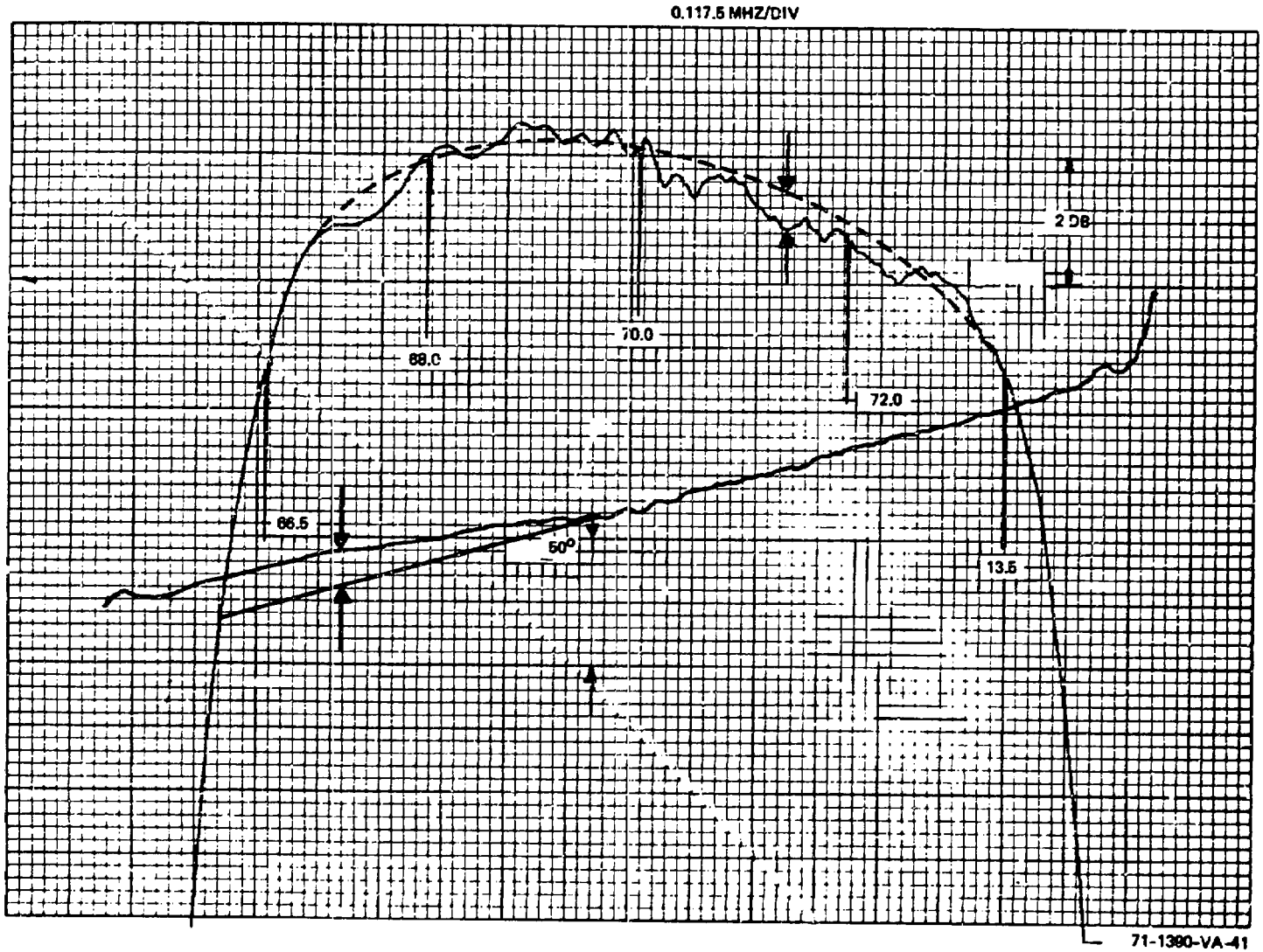

Figure 10: Computed and Experimental Results for $\Delta z/z = .11\%$ (COM 5).

MATCHED FILTERING WITH SURFACE ACOUSTIC WAVE DEVICES

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ABSTRACT

A review is made of the present state of surface wave matched filters. Recent work at the Naval Research Laboratory and other laboratories in phase coded and frequency modulated devices is described, and salient features of various matched filters are presented.

SUMMARY

Within the past few years, advances in surface acoustic wave (SAW) technology have resulted in the compact implementation of a variety of matched filtering devices ranging from bi- and poly-phase coded tapped delay lines to linear and nonlinear frequency modulated devices. The purpose of this paper is to report on the state of the rapidly developing surface wave technology, to present recent work at the Naval Research Laboratory and several other laboratories and to summarize the salient features of the various surface wave matched filter implementations.

Conventional photolithographic processes limit transducer patterns to line widths of about one micron. This corresponds to an operating frequency of about 800 MHz on commonly used material such as lithium niobate ($LiNbO_3$) and quartz. With computer

controlled scanning electron beams, line widths of a tenth micron with line stabilities of 0.03 microns are being achieved. Nevertheless, many matched filtering devices are being fabricated with center frequencies below 100 MHz because of various system considerations, and consequently, the critical parameter is time delay, or equivalently propagation length. Transducer patterns of up to six inches long and longer, containing thousands of individual metallized lines have been fabricated and time-bandwidth products into the thousands are presently being achieved. Fig. 1 shows a few representative delay lines developed at Hughes Aircraft Company. These are circulating and reflecting 100 microsecond delay lines consisting of two 50 microsecond linearly dispersive transducers on ST-cut quartz. The center frequencies range from 30 to 60MHz with compression ratios varying from 560:1 to 2000:1.

One of the simplest methods of achieving matched filtering with SAW devices is to phase code a tapped delay line. Bi-phase M sequence codes have been implemented with responses very near the theoretical limits. However, bi-phase codes are inherently restricted by relatively high time sidelobes, and consequently, poly-phase and complimentary-pair codes have been investigated. Although perfect cancellation of sidelobes is theoretically possible in these cases, practical values of about -25 dB are being achieved.

Although basically nondispersive, surface wave delay lines may be made dispersive by proper transducer design. Linear and nonlinear FM matched filters have been proposed along with various weighting procedures. Fig. 2, provided by North American Rockwell, shows the dispersion of a representative transducer pattern designed for 300MHz operation on ST-cut quartz, but deposited on a faster substrate, aluminum nitride on sapphire($A\ell N/A\ell_2O_3$). Although not designed for $A\ell N/A\ell_2O_3$, the transducer behaves

very well and demonstrates one advantage of $A\ell N/A\ell_2O_3$: the extension of the bandwidth of SAW devices with existing transducer technology.

The pulse expansion and compression properties of the transducer pattern of Fig. 2 deposited on ST-cut quartz are shown in Fig. 3, indicating very good characteristics and near theoretical time side lobe levels.

A conservative estimate of compression ratios possible for various substrate materials is given in Fig. 4 suggesting that compression ratios of 10,000:1 and more may be achieved in the very near future.

Within the past few years, matched filtering with surface acoustic waves has yielded devices with ever increasing compression ratios. Delay lines with ratios in the thousands are being fabricated and new materials and advances in transducer technology promise even higher performance.

ACKNOWLEDGMENTS

The authors wish to acknowledge the help of J.C.Aukland, J.Burnsweig, Dr.E.H.Gregory and R.A.Kempf in providing background from various industrial laboratories.

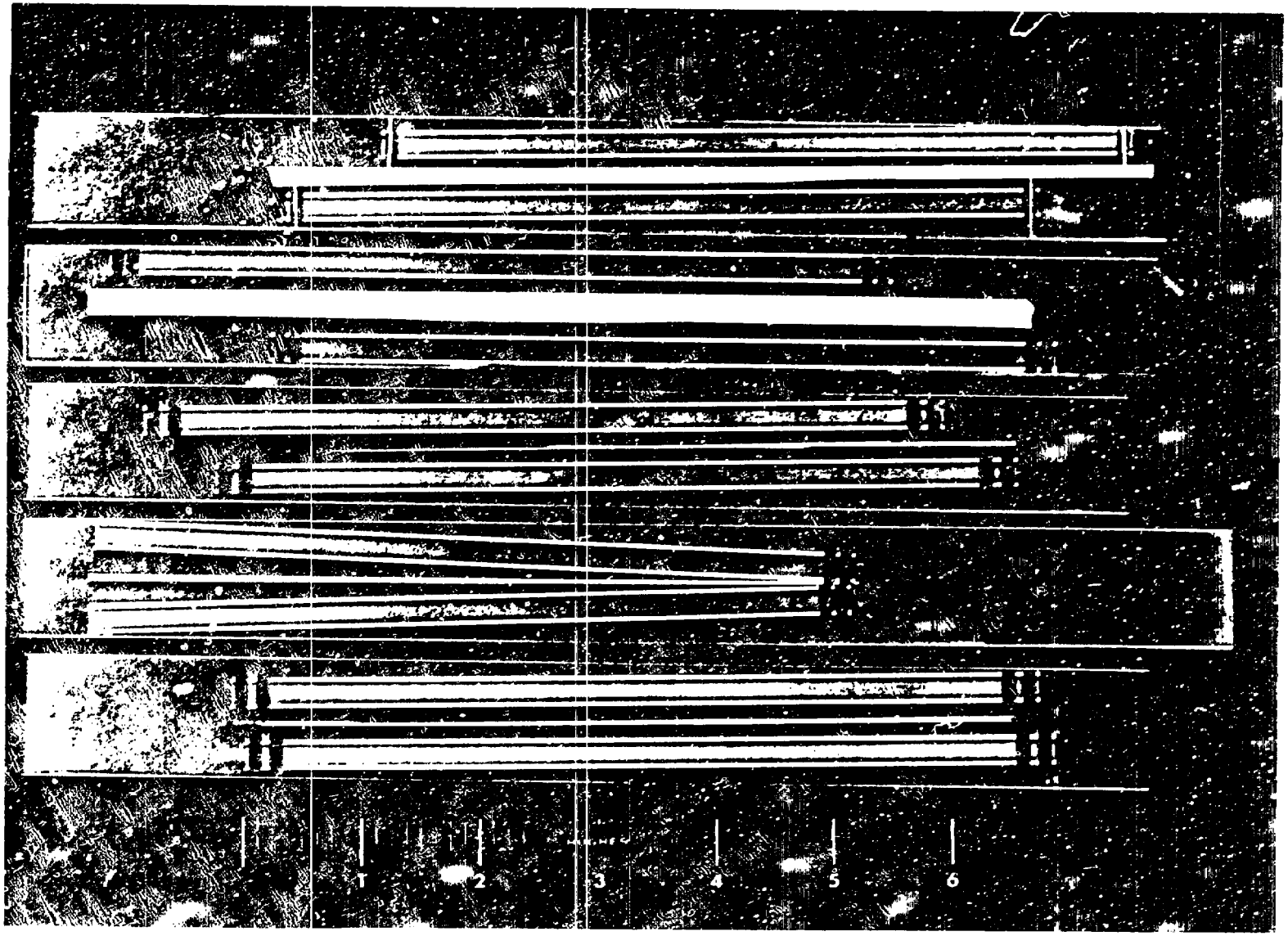

Figure 1: Photograph of several 100 microsecond delay lines with compression ratios to 2000:1 (from Hughes Aircraft Company)

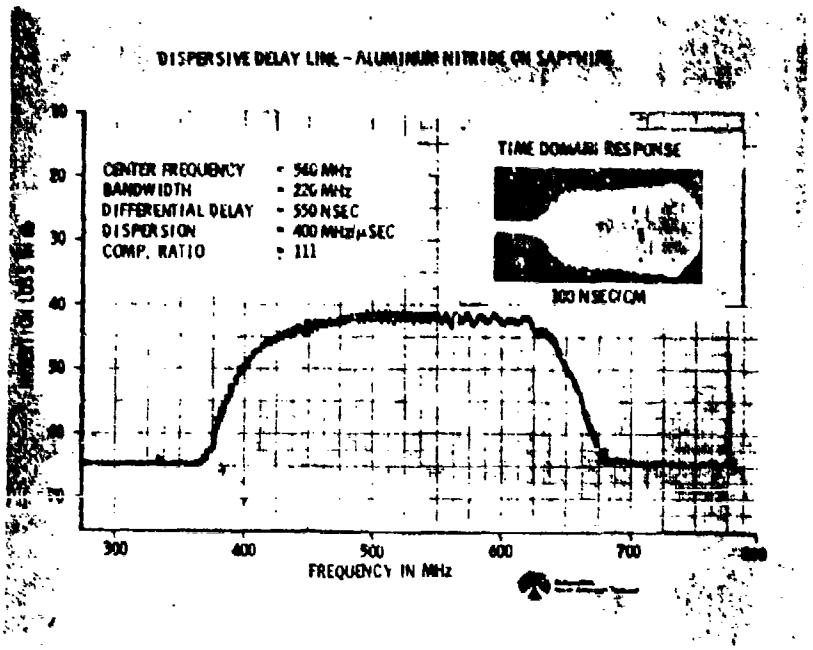

Figure 2: $A\ell N/A\ell_2O_3$ dispersive delay line (from North American Rockwell)

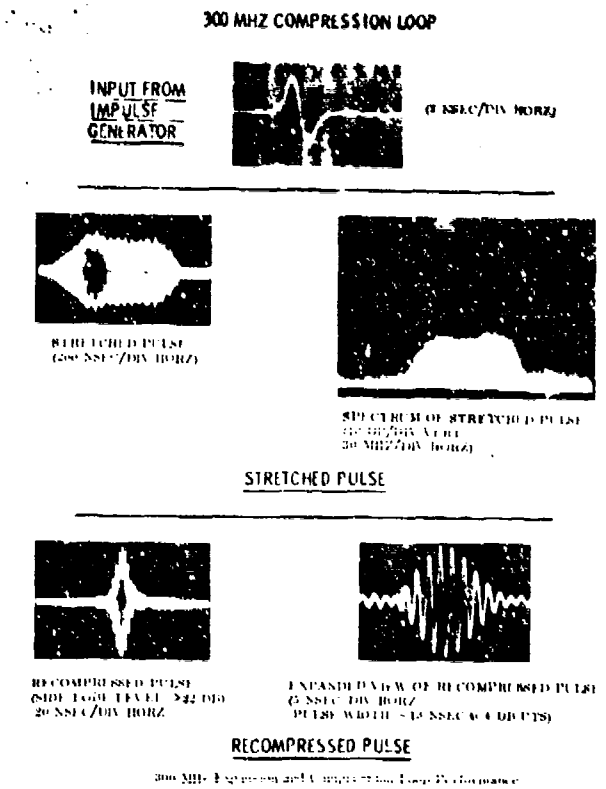

Figure 3: Pulse expansion and compression at 300MHz on ST-cut quartz (from NAR)

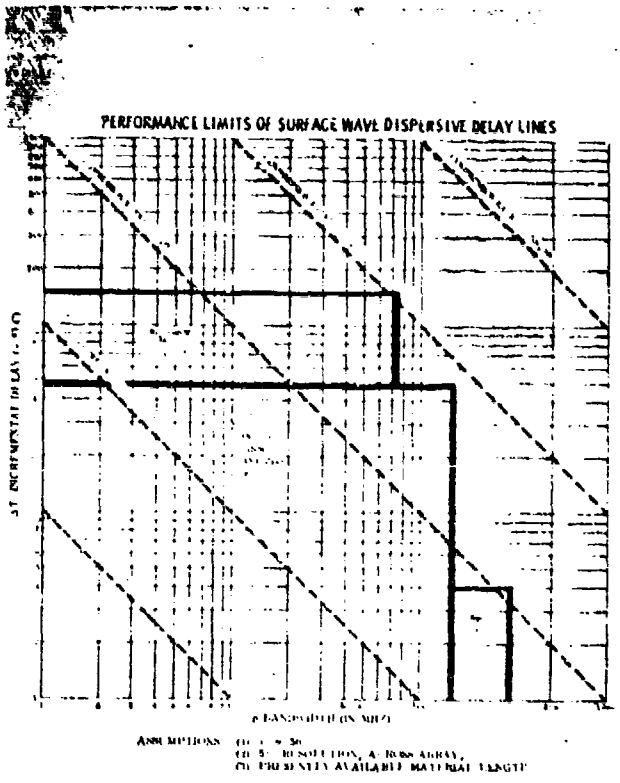

Figure 4: Performance limits of various surface wave delay line substrates (from NAR)

IC PACKAGES AND HERMETICALLY SEALED-IN CONTAMINANTS

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ABSTRACT

An extensive analysis of gas in integrated circuit packages has revealed a lack of adequate control by the semiconductor industry. Contamination mechanisms, gas analysis procedures, fine and gross leak test inadequacies, and specification recommendations will be discussed.

IC PACKAGES AND HERMETICALLY SEALED-IN CONTAMINANTS

R. W. Thomas

RELEVANCY

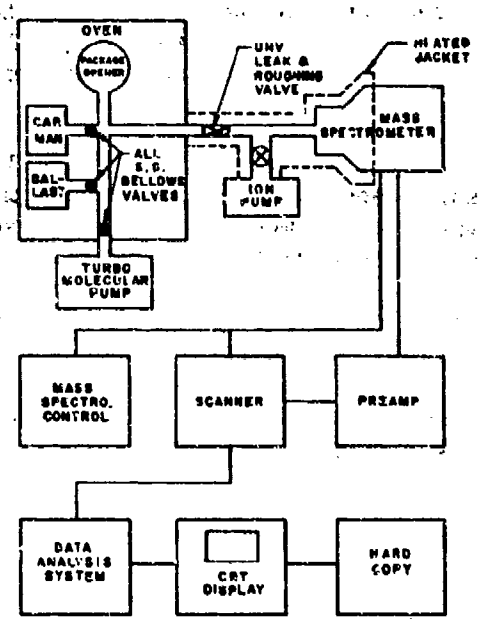
An extensive analysis of gas in integrated circuit (IC) packages has revealed that there are wide variations in the ambient gas from lot to lot, manufacturer to manufacturer, and with different package designs. These uncontrolled gas ambients became relevant when RADC found that a high percentage of field failures returned for analysis contained large amounts of water vapor. Further, it was found that water vapor behaved as a necessary, but not always sufficient condition for failure, the most noted exception being the distilled water electrochemical etching of nichrome resistors in radiation hardened circuits.

The contamination of the chip ambient has become more prevalent with the proliferation of ceramic packages and solder sealing glasses. The entire blame for hermetically sealing water and other contaminants in the packages cannot fully be laid on the semiconductor industry. MIL-M-38510 and MIL-STD-883 did not specify the remaining chip ambient after sealing. Even more important, there was no data available which gave tolerance levels for integrated circuits in general or specific device types in particular. Further investigation revealed that quantitative water analysis was very difficult and that few companies could afford the equipment necessary for such an analysis.

After establishing through failure analysis that hermetically sealed-in contaminants were a real-world problem both in state-of-the-art devices and those which have been in the field for several years, a program was initiated to develop an accurate gas analysis facility. Such a facility now exists at RADC. The development, design, system sensitivity, and the results of an extensive IC gas analysis program are the subject matter of this presentation.

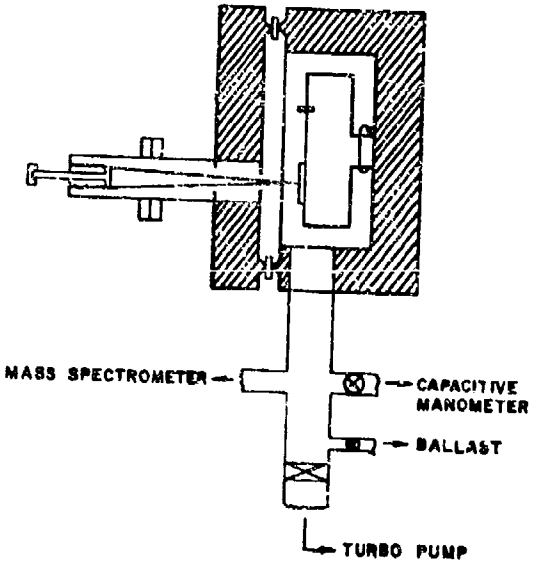
RADC GAS ANALYSIS SYSTEM

The system fabricated at RADC for package gas analysis has been under continuous development for three years. The present version was fabricated entirely from stainless steel, with copper sealed ultra-high vacuum flanges and welded stainless steel bellows valves. Ultra-high vacuum fabrication techniques such as notching the internal machine screws for gas relief, polishing large surface areas, and minimizing internal volume were vitally important in achieving maximum performance. Materials such as glass, teflon, viton, and vacuum grease were removed from the system as originally designed to obtain low outgassing rates. The present system is shown in figures 1 and 2.



I.C. GAS ANALYSIS SYSTEM

FIGURE 1



PACKAGE OPENER

FIGURE 2

The ionization gauge was removed from the original system after it was found to be the cause of secondary reactions and regurgitation. The ion gauge was replaced with a digital capacitive manometer which has a low outgassing rate and makes an excellent mass-independent calibration system.

To open the package, a hardened steel needle either punctures or splits the package depending on the package material or design. Up to twenty packages may be mounted on an indexed rotating holder and analyzed during one vacuum bakeout cycle.

The system volume was designed so that the expanding gas from a flat-pack results in a system pressure of 1×10^{-5} torr, the high pressure limit of the quadrupole mass spectrometer. To accommodate larger packages, a ballast is valved into the system and adjusted to obtain the proper pressure.

In making quantitative gas analysis measurements, one is confronted with an overwhelming number of mass-selective and gas history-sensitive mechanisms. For instance, all leak valves, vacuum pumps, ionizing chambers and electron multipliers are mass-selective devices. The electron multiplier and ion pump are particularly gas history-sensitive. To make the analysis even more complicated, it was experimentally determined that once the package was opened, each gas specie diffuses from the package at a different rate. It quickly became evident that only a dedicated computer, operating in real time, could analyze and correct for a number of variables operating simultaneously.

SYSTEM PARAMETERS

The system scans the mass range from 1. to 100. atomic mass units in one second. The absolute accuracy is presently 1.% of the constituent measured. The sensitivity of the system is constituent dependent and varies from 10. parts per billion for oxygen to 6 parts per million for water and hydrogen. All other gases fall into this range. At the time of writing, this is considered to be state-of-the-art. It is expected that, by improving vacuum techniques and using more sophisticated statistical analysis procedures, these system parameters will continually improve.

RADC IC GAS ANALYSIS PROGRAM

RADC is currently conducting a multilevel program to solve the sealed-in contaminants problem. An ultra-clean package sealing system is currently under development. This system will seal controlled quantities of contaminants into IC packages to determine tolerance levels of sensitive circuits to water vapor and other contaminants. The sealer will also permit the packaging of standard ambients for round-robin calibration and sensitivity checks of other gas analysis systems.

Lot sampling of new devices and packages will be expanded. This will allow various sealing systems to be fingerprinted by mass spectrometry to detect possible changes or degradation in sealing integrity and purity.

Working in cooperation with the Physics of Failure Laboratory at RADC, a considerable amount of data has been gathered on contamination-produced failure mechanisms. A brief synopsis of this work is included in the following section. This work will be expanded to include a study of the effect of various stresses on the chip ambient.

The components found in some IC packages indicate that some additional work should be done on the effectiveness of present fine and gross leak tests.

RESULTS OF GAS ANALYSIS INVESTIGATION

A small but significant percentage of the packages opened contained residual amounts of helium and freon. This led to further experimentation and the discovery that water, freon, and neon could be inserted into the "hermetically" sealed package by a one-way thermomechanical valve action at the lead frame, if the package was bombed at an elevated temperature (150°C.).

Water was found in IC packages in amounts exceeding eight times the water contained in air at 50.% relative humidity and 25.° C. The circuit failures in these packages were directly related to the excess water.

The thermal stressing of ceramic IC packages will increase the water and carbon dioxide content at lower temperatures (150.°C.), and change to methane and hydrogen at temperatures of 350.°C. This observation can be directly related to improper curing of the binder used in the sealing glass.

From the analysis of more than fifty samples from a particular manufacturing line it was possible to observe groupings in the gas composition. Changes in this fingerprint indicated changes in the sealing frit, purge gas, oven sealing ambient, and procedural changes in the sealing operation. Feasibility was demonstrated in establishment of norms for specific packages and sealing procedures, which could then become the basis for lot acceptance specifications.

CONCLUSION

The conclusion is self-evident. There is a definite need at the present time for a hard look at the presently-used sealing procedures, gas analysis techniques and specifications for ensuring an inert chip ambient. RADC, through its Air Force

Sealing operations.

$BLIP_{TM}$ - BEAM LEADED INTERCONNECT PACKAGING

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ABSTRACT

This paper describes a microcircuit packaging approach which eliminates flying wire bonds, a major failure mode in microcircuits, and utilizes beam leads formed independently from the active devices. Both intra- and interconnections are made with beam leads thereby eliminating all flying wire bonds. $BLIP_{TM}$ is a multilayered micropackaging concept that is keyed to a disciplined system of component management, interconnection requirements that include integral beam leads, assembly processes and testing of the in-process or completed functional circuit.

I. INTRODUCTION

Hybrid technology has been highly successful in achieving a dramatic reduction in size and weight. The density and complexity of today's hybrid circuits have led to new approaches in fabrication, such as multilayer conductors and beam leaded or flip-chip integrated circuits.

A major disadvantage of the present methods of microcircuit packaging has been that of cumulative processing with an inability to functionally test the circuit until after final assembly when the majority of labor and material costs have been expended. $BLIP_{TM}$ makes use of parallel processing with functional testing capability prior to commitment of costly material such as integrated circuits.

II. THE BLIP CONCEPT

The major features of BLIP are illustrated in Figure 1. The die plate is composed of a photopolymer material laminated to a base plate which may be a standard substrate such as alumina or beryllia. The substrate may be metalized and form one level of interconnection and may also contain resistor elements. The photopolymer material forms cavities in which circuit components nest and, by means of alignment marks, allows the precise attachment of circuit components independently of the interconnect network which is the second BLIP

component. The interconnect network is a multilayer conductor pattern with integral beam leads for connection to the components as well as to the outside world or second level interconnection.

III. DIE PLATE FEATURES

The substrate is first processed through standard vacuum deposition and photoetch steps to obtain the desired conductor and resistor patterns. The dry film photopolymer serves as a spacer and therefore its thickness is determined by component heights and by the interconnect network thickness. After the lamination step, the photopolymer is exposed and developed to form device cavities to allow attachment of active devices to the substrate. Keying or alignment marks are also formed during this step around each cavity so that the component may be precisely aligned when it is mounted.

The substrate size is limited only by the uniformity of metalization desired during vacuum deposition and therefore a large number of die plates may be formed on a single substrate. After lamination and photoimaging, the die plate is ready for component attachment. This may be performed before or after the substrate is broken into individual die plates.

IV. THE INTERCONNECT LAMINATE

The interconnect laminate is made up of alternating layers of a suitable dielectric such as epoxy glass and conductor paths which serve to interconnect all components. Although the number of conductor layers is not unlimited, three have been found adequate for the most complex of hybrid designs, so far implemented.

The most important feature of the interconnect laminate is the integral beam leads that are formed to make connections to the active devices. These project over the component windows and are formed to make contact with a device bonding pad as illustrated in Figure 2. The external connections are also beam leads so all flying wire connections are eliminated.

Connections between layers are made by plated through holes or vias. The vias are first formed by photochemical etching then electroless and electrolytic plating are used to form the electrical connection.

V. THE ASSEMBLY PROCESS

The fabrication of the interconnect laminate and the baseplate are both batch processes with each lot capable of producing hundreds of parts. Furthermore, they are parallel processes, each operating independently of the other. After they have been processed, tested, and inspected, they are ready for the final assembly steps.

The interconnect laminate and the baseplate, loaded with components, are now bonded together. Individual circuits may be bonded, if the substrate has been separated into single die plates, or all circuits on a substrate may be bonded simultaneously. Alignment is straightforward since beam leads and device bonding pads are both visible.

After curing the bonding adhesive, the circuit is now ready for ultrasonic bonding of the beam leads to the components. Beams are presently bonded one at a time but the adaptation of a wobble or compliant bonder appears quite feasible.

Assembly errors are reduced with $BLIP_{TM}$ because subassembly (die plate and interconnect) orientation can be easily checked. This leads to a reduction of labor skill required and therefore a cost reduction. It further minimizes troubleshooting because of the ease of visual inspection.

VI. PACKAGING

A major improvement in packaging density is achieved by eliminating the traditional hermetically sealed flat pack. This reduced surface area and volume requirements and also eliminates fan out restrictions imposed by the flat pack. The environmental protection required for the unpackaged $BLIP_{TM}$ module is achieved by a vapor deposited conformal coating of parylene whose barrier properties are superior to the silicones.

Parylene is the generic name for members of a unique polymer series developed by Union Carbide Corporation. The basic member of the series is poly-para-xylylene but the two types of interest, designated Parylene C and D, are chlorinated and dichlorinated modifications, respectively.

The replacement of a hermetically sealed package with another form of environmental protection must take into consideration all the common components of a microcircuit such as semiconductors, capacitors, and resistors. In the case of semiconductors, silicon nitride offers much potential for protecting these sensitive devices but ceramic chip capacitors and nickel-chromium resistors are also very susceptible to humidity.

If parylene is to serve as a replacement for hermetically sealed packages, the barrier properties of the material are of prime importance. These properties are given in Table 1 and compared with those of the more common organic coatings.

Table I

Barrier Properties of Some Representative Organic Coatings

	N_2 (1)	O_2 (1)	CO_2 (1)	H_2 (1)	H_2O (2)
Parylene C	0.6	5	14	110	1
Parylene D	4.5	32	13	240	0.25
Epoxies	4	5-10	8	110	1.8-2.4
Silicones	-	50,000	300,000	45,000	4.4-7.9
Urethanes	80	200	3,000	-	2.4-8.7

(1) Gas permeability, cc-mil/100 in^2 - 24 hrs; ASTM D1434-63T

(2) Moisture Vapor Transmission, gm-mil/100 in^2 - 24 hrs; ASTM E96-63T

The material is deposited from the vapor phase in a "soft" vacuum, with the mean free path of the parylene molecule on the order of 0.1 cm. The result is a truly conformal deposition rather than the line of sight type coating one usually associates with vacuum deposition techniques.

Because of these attractive characteristics, Northrop initiated a program to study parylene coatings on $BLIP_{TM}$ microcircuits. A deposition system was designed and built (see Figure 3) and a series of preliminary tests conducted. The results of the preliminary tests, discussed below, were encouraging enough to justify a large scale military qualification type test program which is presently underway.

VII. ENVIRONMENTAL TEST RESULTS

A. IONIC Contamination Test

A major concern of any semiconductor passivation coating is that the coating does not introduce ionic contamination. For this test a group of PNP (2N2907) unpassivated transistors were parylene coated and submitted to a humidity test in accordance with MIL-STD-810B.

One hundred eighty of these parts were mounted in unlidded flat packs. The leakage current (I_{CBO}) was measured at an ambient temperature of 120°C prior to parylene coating, after the coating was applied, and after the 10-day humidity test which exposed the parts to 85 percent relative humidity and a temperature variation of 25° to 71°C on a 24 hour cycle. Leakage currents remained constant during and after the test, indicating that parylene did not cause any ionic contamination but did protect the parts from the humidity environment.

B. Humidity

In the presence of an electric field and moisture, thin film nickel-chromium resistors are very susceptible to electrolysis. To determine the effectiveness of parylene as a moisture barrier, one hundred eighty seven nickel-chromium thin film resistors were mounted in unlidded flatpacks and parylene coated. These resistors, of various form factors and values, (see figure 4) were powered at several different power densities to ensure condensation on at least some of them. A control lot of 55 unprotected resistors were also tested and all resistors underwent the MIL-STD-810B test described in Section A above.

Resistor values were read and recorded before and after the parylene deposition and after the humidity test. The parylene coated resistors showed no change in value whereas 10 of the 55 uncoated resistors had catastrophic failures or major resistance changes (≥ 20%) with some of the failures occuring in the first 24 hours of the test. Because some of the resistors in each lot were unpowered and some powered at densities as high as 150 watts/square inch, failure of all resistors in the unprotected group were not anticipated because condensation did not occur on all resistors.

C. Radiation Induced Ionization

Radiation induced ionization in the parylene coating could cause functional failures in a microelectronic circuit. To determine this, a 2N3960 transistor was employed, using the test matrix below.

	Reverse Bias	No Reverse Bias
Parylene coated	6 units	6 units
No parylene coating	6 units	6 units

Leakage currents and DC current gain at 100 microamperes and 1 milliampere were recorded before and after radiation. Exposure levels were 7×10^4 n/cm^2 and 1×10^6 rad/Si. Comparison of before and after data showed no significant difference between coated and uncoated devices with and without power applied. This indicates that parylene does not trap a charge or have other deleterious effects, due to radiation, on sensitive semiconductor devices.

D. Nuclear Testing

Results of recent underground tests on parylene coated BLIP$_{TM}$ circuits, when compared to uncoated circuits, demonstrate that parylene improves the survivability of a circuit in a thermo-mechanical shock environment.

VIII. FUTURE DEVELOPMENTS IN BLIP

A large factor in manufacturing costs of highly complex hybrids is the troubleshooting and rework caused by defective active devices. The ability to test a circuit functionally prior to the permanent attachment of any active devices would overcome this problem and BLIP offers that potential. If the active devices were attached with a long shelf life epoxy, the interconnect laminate could be aligned over the die plate and electrical connection made by means of mechanical pressure. The entire circuit could then be functionally tested before any bonds are made and before the epoxy is cured. Chip replacement would then be a matter of extracting the die from the uncured epoxy and replacing it with a new die. Troubleshooting and rework could then be accomplished early in the assembly process with a reduction in damage due to rework.

If the circuit checks functionally good at the time of the "pressure test," it would be advantageous to bond the beams immediately. The die plate and interconnect are already aligned and electrical contact is being made at all the required points. If a form of wobble or complaint bonding could be utilized at this point, the assembly could be bonded with no additional handling or alignment.

IX. CONCLUSIONS

BLIP has been demonstrated to be a multilayer hybrid packaging concept which essentially eliminates flying wire bonds. It utilizes standard active devices rather than the new, face-down devices which are presently more expensive and less available.

BLIP does not involve any radical new technology but rather the evolution of proven processes that have been in widespread use for a number of years. The elimination of flying wire bonds and the use of beam lead bonds is a major reliability factor because

BLIP density is presently equal to current thin film density and will surpass it with the application of improved design rules covering such areas as line width and spacing, via size, and via pads. The use of miltilayer conductors eases design and layout constraints and provides the required termination density for the newer, more complex active devices. Its application to very large functional blocks with advantages in testing and final packaging within the same manufacturing format is a next important stage of its usefulness.

X. ACKNOWLEDGEMENTS

The authors wish to express their gratitude to the many people within Northrop who contributed to this project.

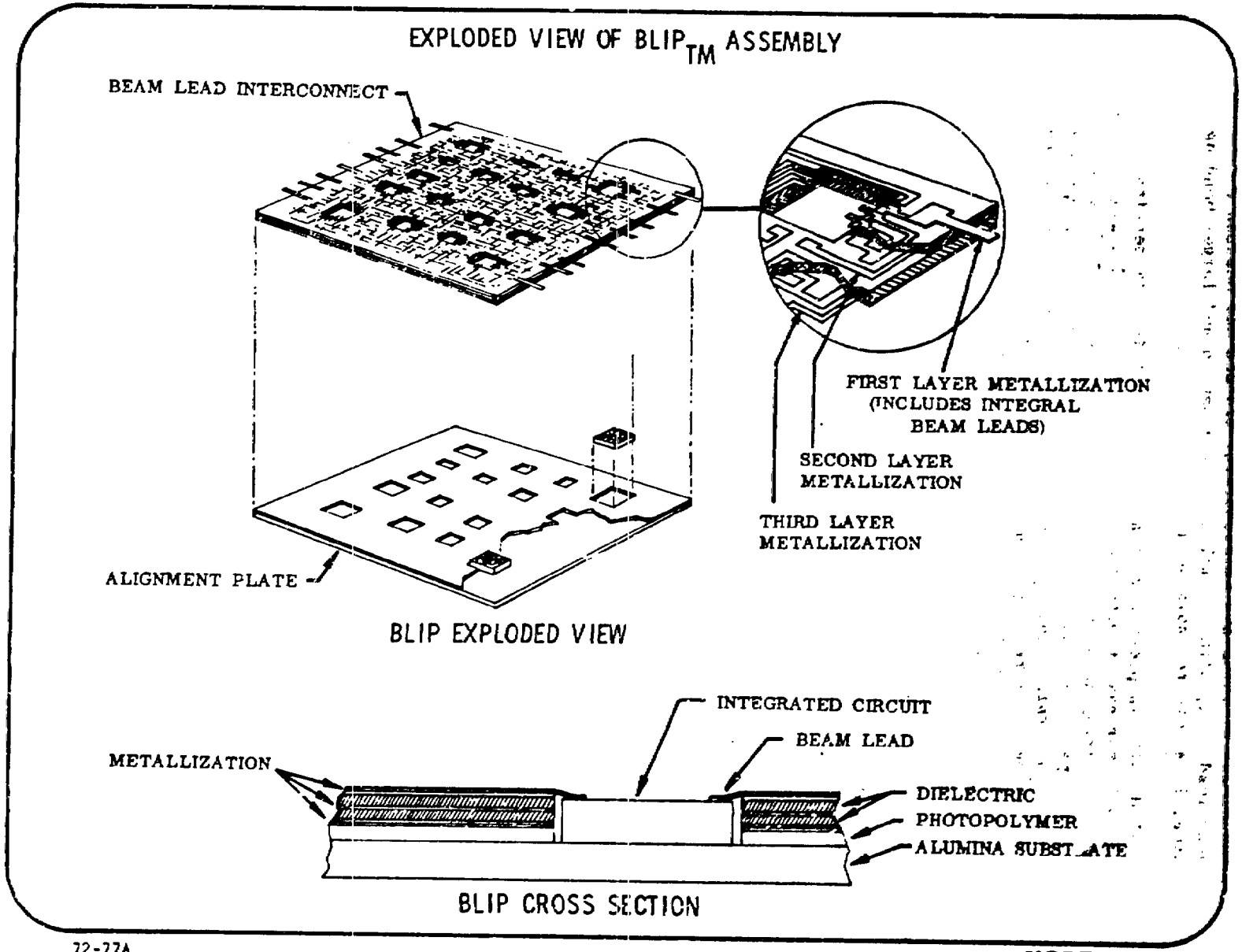

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FIGURE 1 EXPLODED VIEW OF BLIP$_{TM}$ ASSEMBLY

NORTHROP
Electronics Division

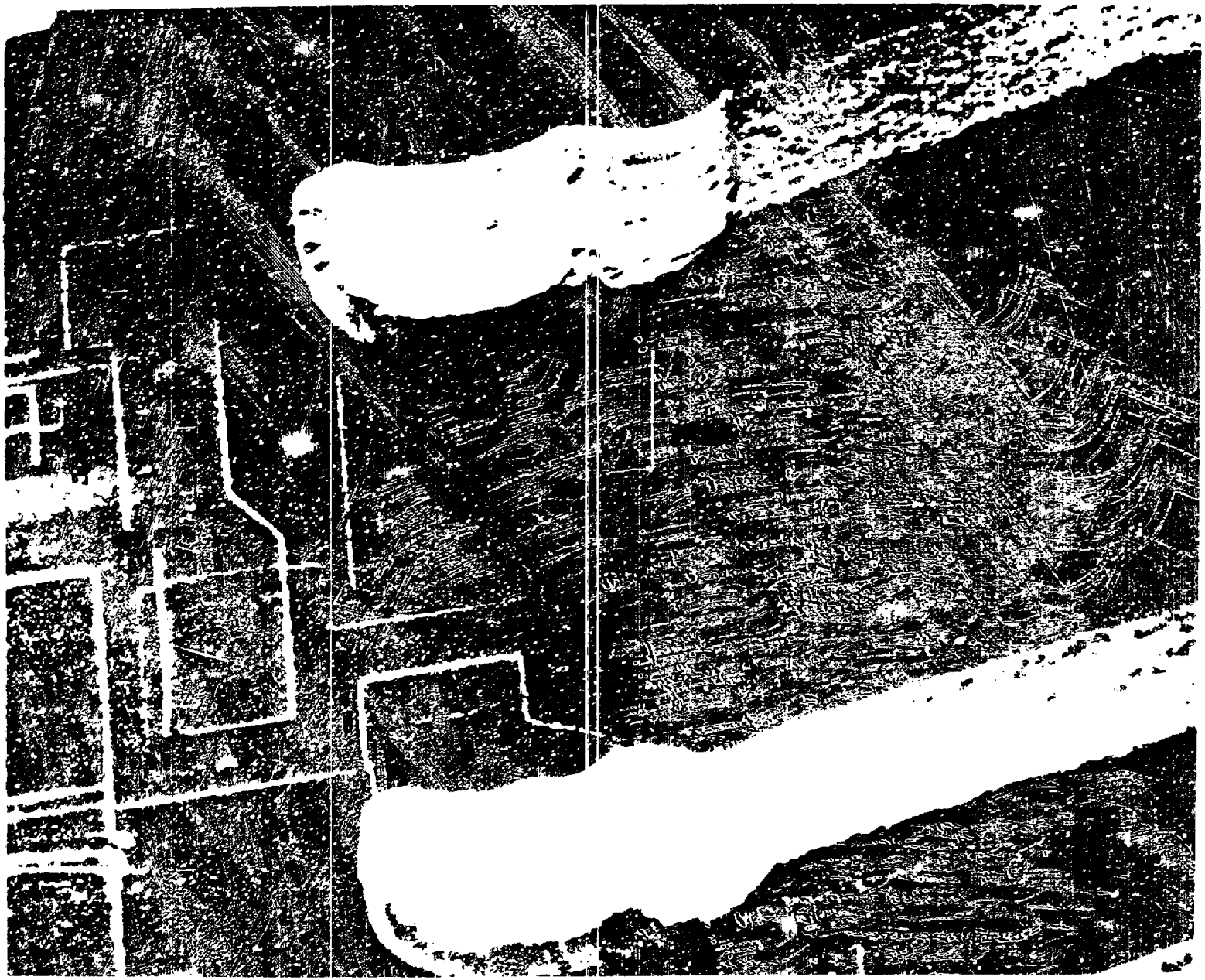

FIGURE 2 SCANNING ELECTRON MICROSCOPE PHOTO OF BEAM LEADS AFTER BONDING

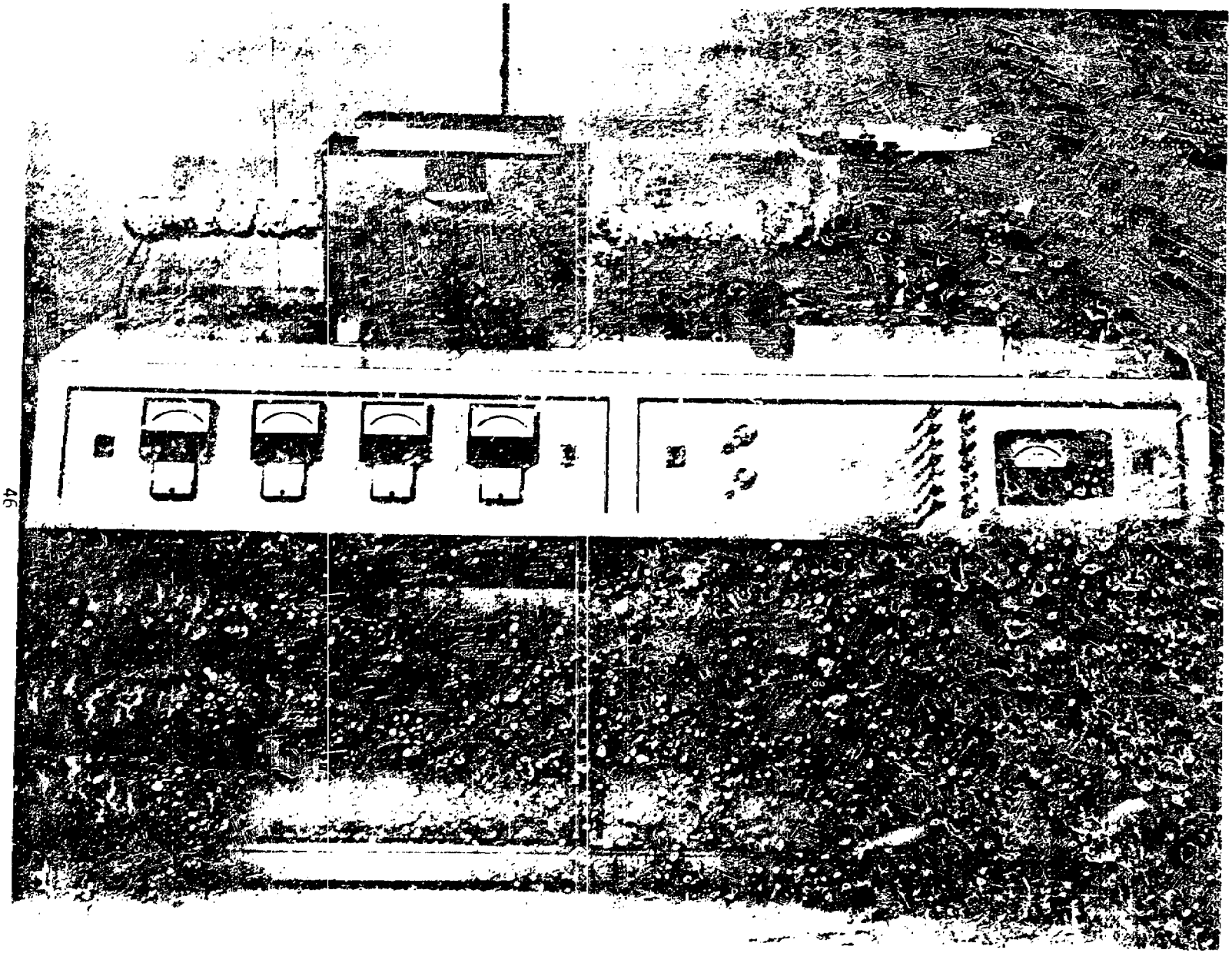

FIGURE 3 PARYLENE DEPOSITION SYSTEM

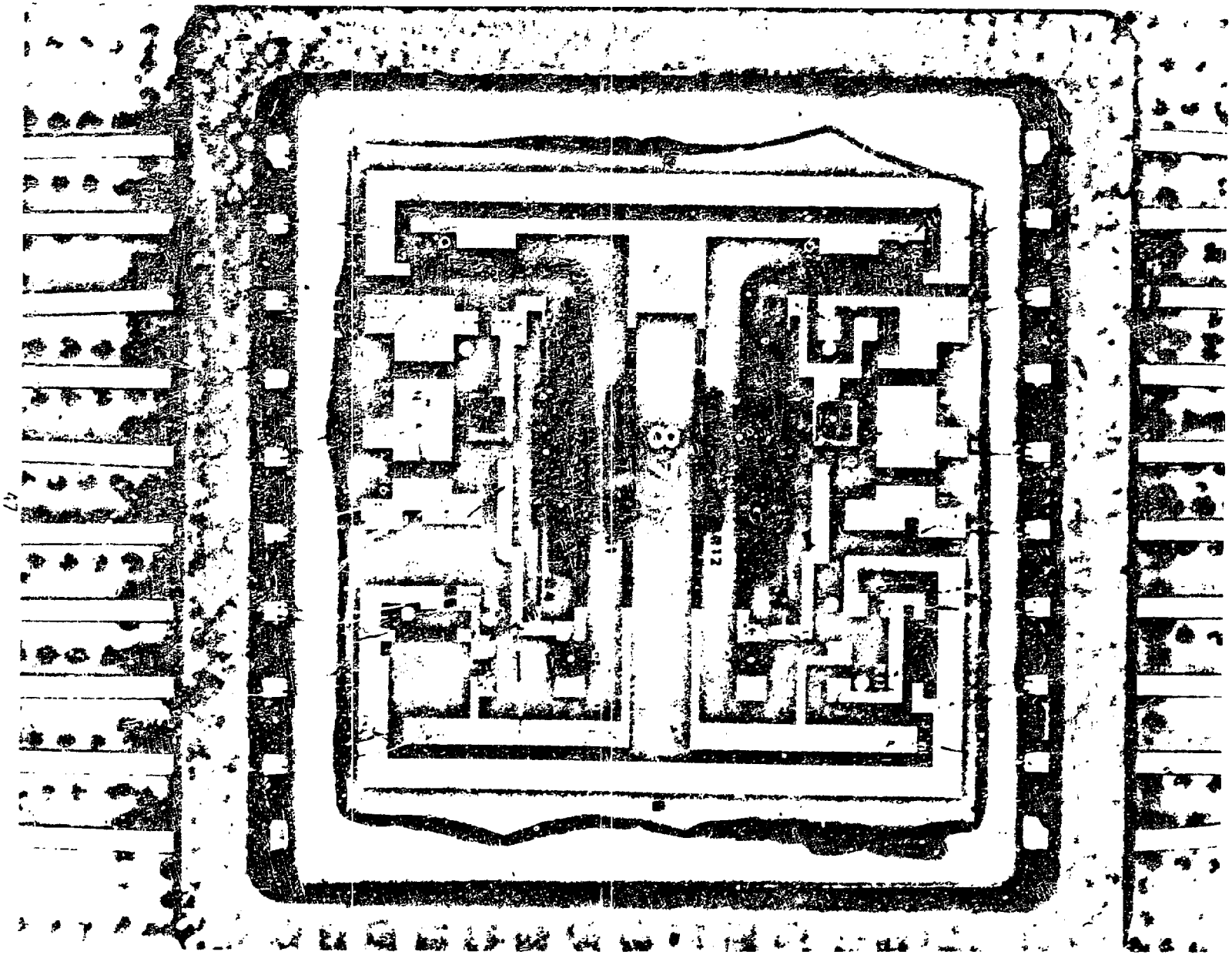

FIGURE 4 RESISTOR HUMIDITY TEST CIRCUIT

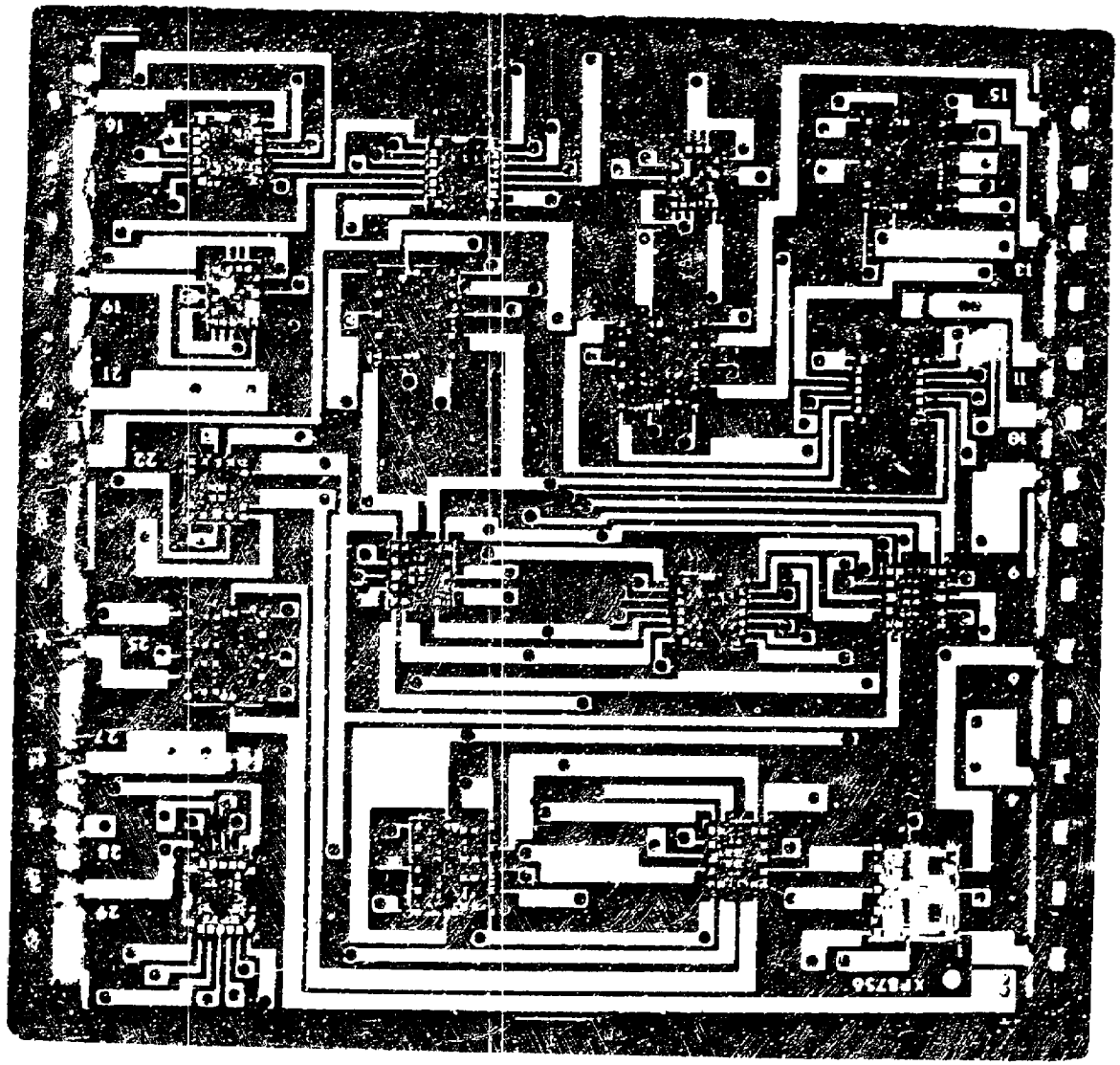

FIGURE 5 1" X 1" BLIP$_{TM}$ HYBRID UTILIZING 3-LAYER METALLIZATION

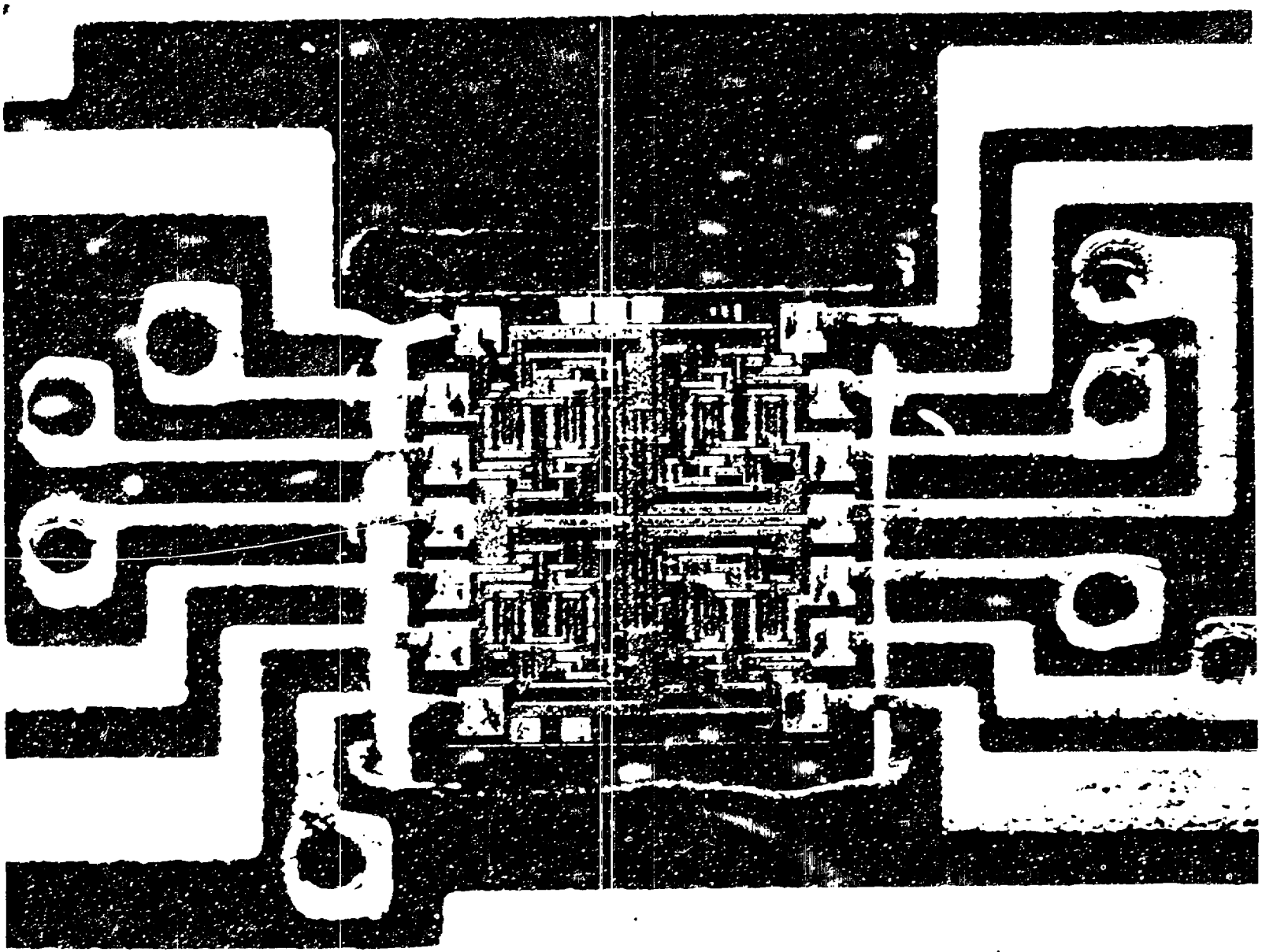

FIGURE 6 MICROPHOTOGRAPH OF ACTIVE DEVICE WITH BONDED BLIP$_{TM}$ BEAM LEADS

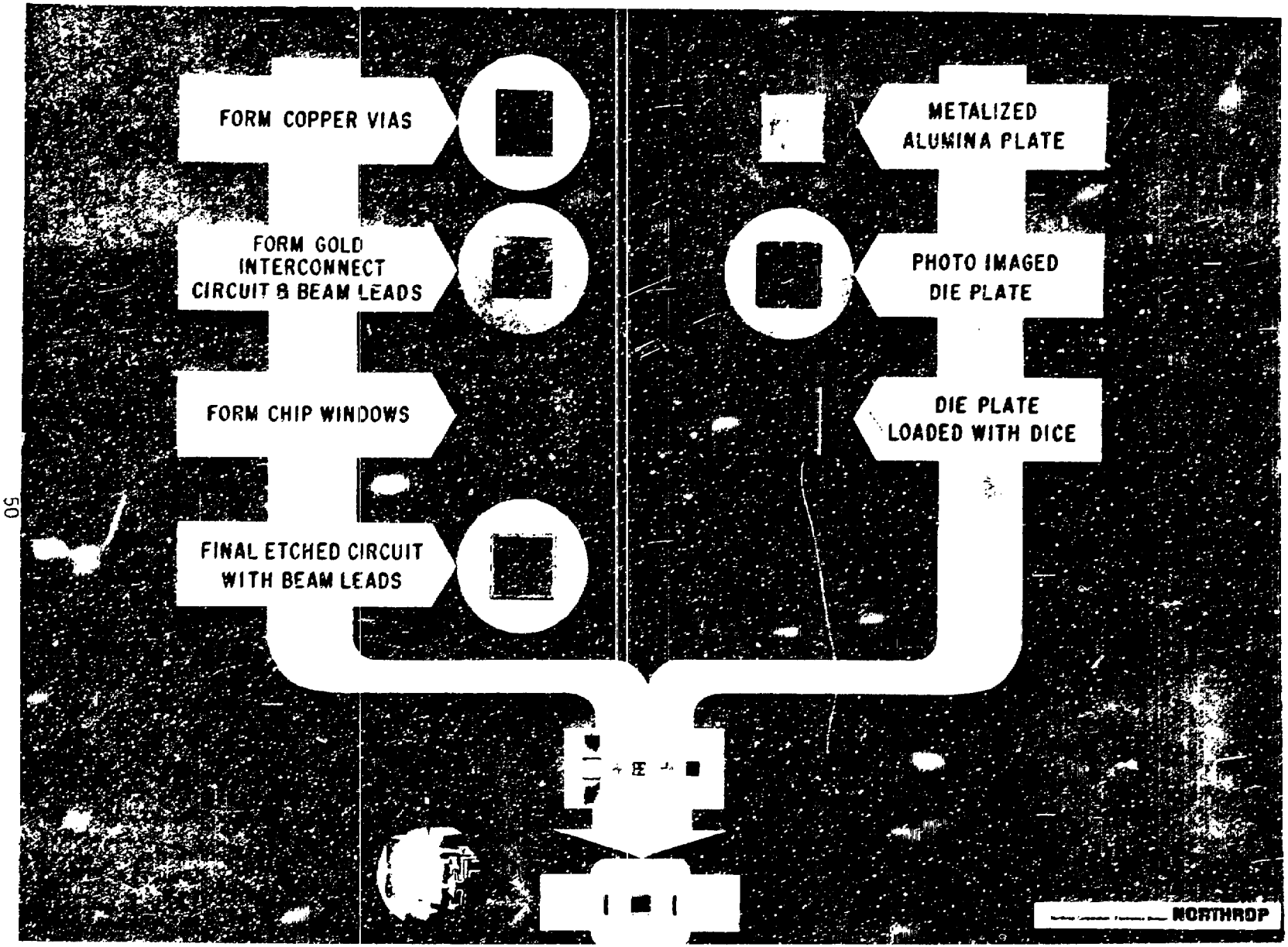

FIGURE 7 BLIP$_{TM}$ PROCESS FLOW DIAGRAM

A UNIVERSAL PACKAGING SYSTEM AS APPLIED TO THE ALL APPLICATIONS DIGITAL COMPUTER

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ABSTRACT

A universal packaging system is described which will serve the requirements of military and space electronics during the latter part of the decade. Design features and fabrication techniques associated with the All Applications Digital Computer Building Block Module and its Zero Force Cam Operated Connector are highlighted.

In addition, the design of the Higher Level Package, which retains a multiplicity of modules, is covered.

INTRODUCTION

A hardware design and development program for the packaging of the All Applications Digital Computer (AADC) has been in progress, under NASC sponsorship, at the Kearfott Division of the Singer Company since June 1970. A primary objective of this effort has been the evolution of a packaging system that has universal application. Packaging techniques are being perfected concurrent with the development of micro-electronic devices that are to be used in military and space electronics during the latter part of the decade.

The program calls for the design, development, and prototype fabrication of:

- A "Building Block Module" capable of retaining a three-inch diameter silicon wafer or hybrid substrate
- Higher Level Package containing a multiplicity of Building Block Modules.

SYSTEM DESCRIPTION

The All Applications Digital Computer packaging system has as its basic element the Building Block Module which provides the hermetic enclosure, interconnect, mounting and heat exchange mechanism for the electronic elements. The module is illustrated in Figure 1.

Electrical connections to the module are made via two 152-Pin Cam Operated Connectors as shown in Figure 2.

A series of Building Block Modules which may constitute a complete electronic system, will be retained in the Higher Level Package; this package provides the cooling air distribution and internal-external interconnect system. Figure 3 is an exploded view of the major elements showing the physical relationship of the Building Block Module, Cam Operated Connector and interconnect system.

The following paragraphs will describe in greater detail the characteristics of the major elements and the engineering tradeoffs that were made in arriving at an optimized system.

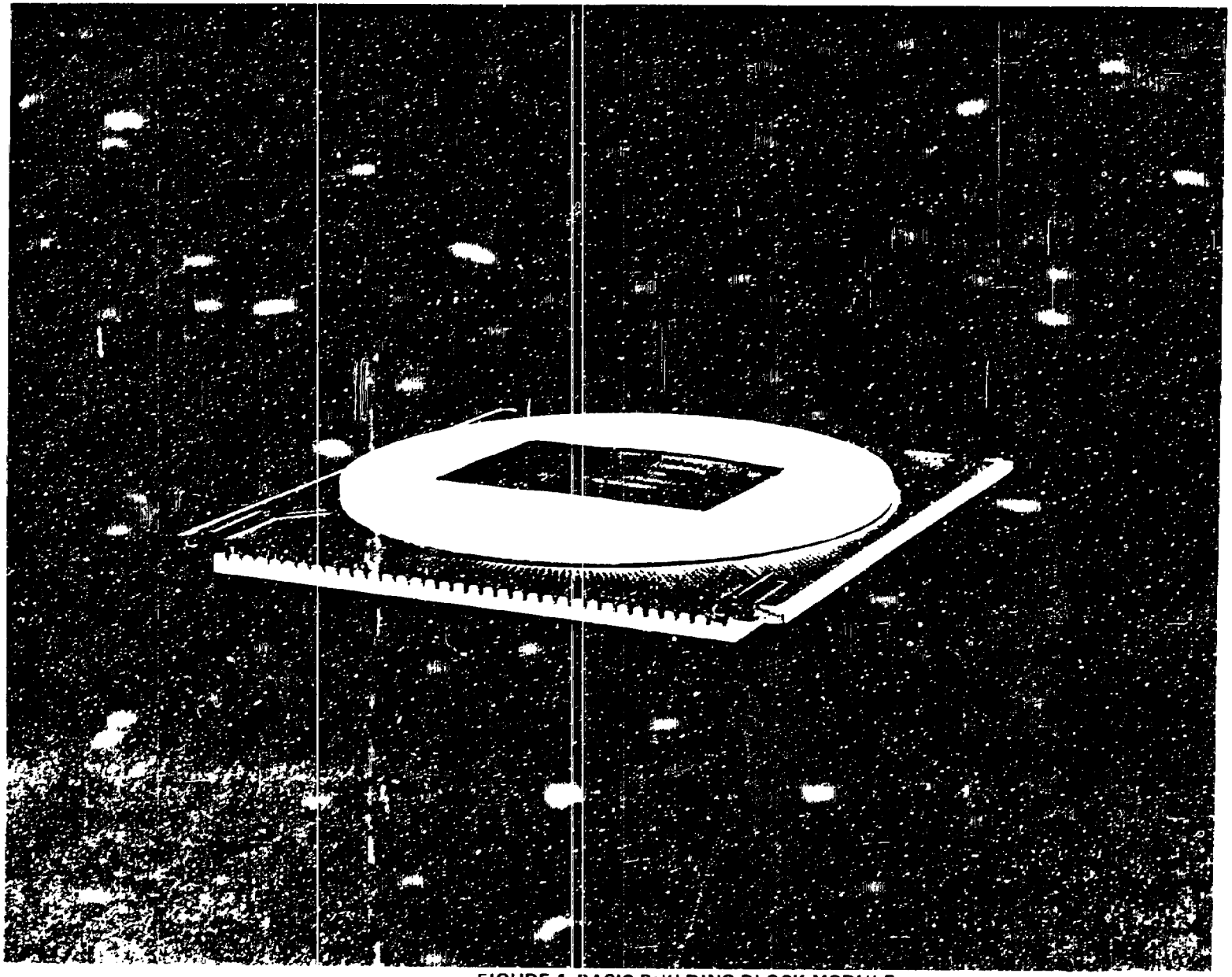

FIGURE 1 BASIC BUILDING BLOCK MODULE

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FIGURE 2 CAM OPERATED CONNECTOR

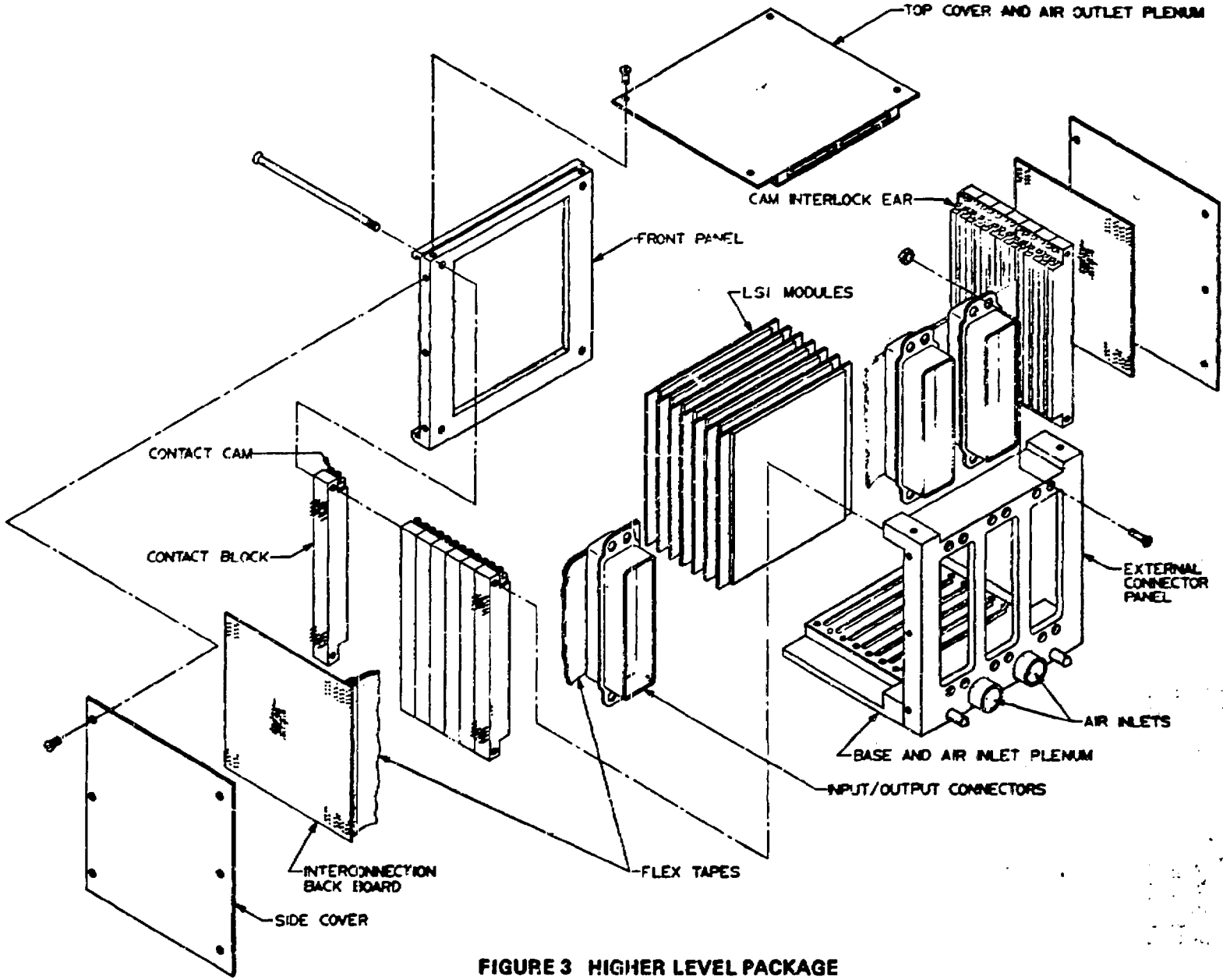


FIGURE 3 HIGHER LEVEL PACKAGE

The AADC Building Block Module illustrated in Figure 1 is capable of retaining a three-inch diameter silicon wafer or a three-inch diameter hybrid circuit substrate. The module's unique features are tabulated below.

- External Connections - 300
- Power Dissipatior - Up to 50 watts
- Maximum Power Density - 7.5 watts/square inch
- Environment - MIL-E-5400 Class 4X - 200°C max
- Hermetic Seal
- Provisions for Guiding, Keying and Clamping
- Interface with Zero Insertion Force Connector
- Integral Heat Exchanger
- Vibration Resonant Frequency - above 2000 Hz
- High Speed Circuit Compatibility (10 nsec delay)
- Size - 4 inches x 4 inches x 0.400 inches width (20 watt module)
- Weight - 0.43 pound (20 watt module)

DESIGN TRADEOFF

The final configuration was arrived at after an extensive design trade-off process which concerned itself with four major areas:

- Module thermal and electrical characteristics
- Interface with the next higher level package
- Mounting, interconnection, and line routing to the 3-inch diameter wafer or hybrid substrate
- Module manufacturing processes and lid sealing

The trade-off process was concerned with configurations that provided for efficient heat removal while optimizing the interconnection and line routing requirements.

Conventional techniques (Figure 4) that make use of conductive cooling to heat exchangers at the card edge, were dismissed as being inefficient.

By mounting the heat exchanger directly behind the power dissipating elements (Figure 5), a more efficient thermal design with a considerably shorter conducting path is possible. This latter design, however, is deficient since it requires a 300-pin connector having high insertion and removal forces.

The integral ceramic heat exchanger design illustrated in Figure 1 retains the thermal advantages of direct cooling while eliminating the connector problem. The design provides for:

- Zero insertion force connectors
- Short line lengths
- Direct connections eliminating the need for intermediate circuit boards
- Integral heat exchanger

Table 1 summarizes the characteristics of the various design approaches.

INTEGRAL HEAT EXCHANGER MODULE DESIGN

The integral ceramic heat exchanger unit consists of a ceramic slab containing the line routing from the 152-external connector pad terminations, along each of the two edges, to the 3-inch diameter wafer. A molybdenum-titanium metallized sealing ring facilitates hermetic sealing of a ceramic or Kovar cover. Keying pins, which guarantee a unique module location in the Higher Level Package are brazed to the base slab. External connections are made via a set of 152-Pin Cam Operated Connectors contacting the pads on .050 centers. The heat exchanger, wh[illegible] can be sized to be compatible with the power dissipation of the module, is cemented to the base slab.

Table 2 summarizes the module's thermal characteristics for various material combinations, flow rates, and heat exchanger designs.

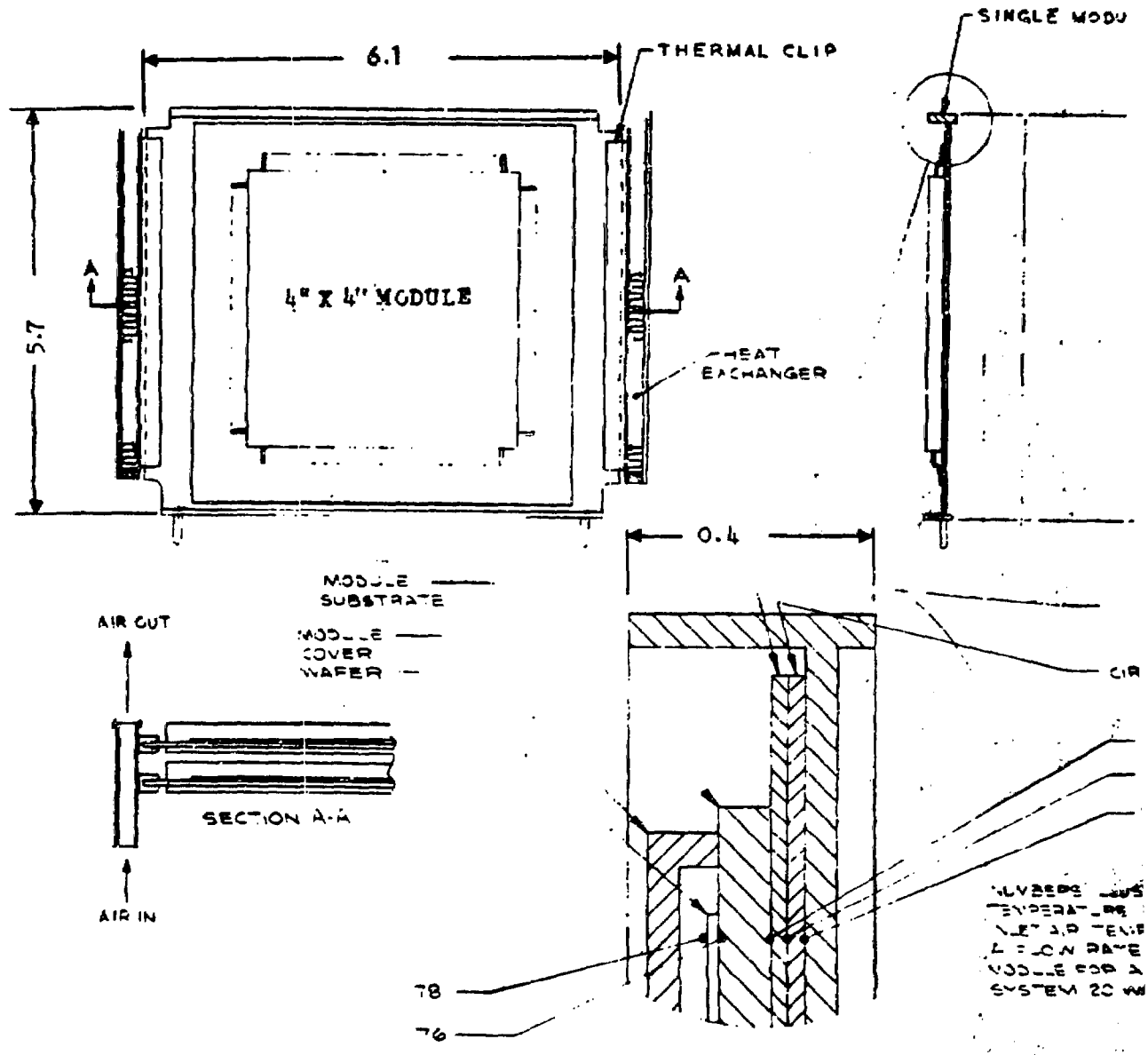


FIGURE 4 CONDUCTIVE COOLING CONFIGURATION

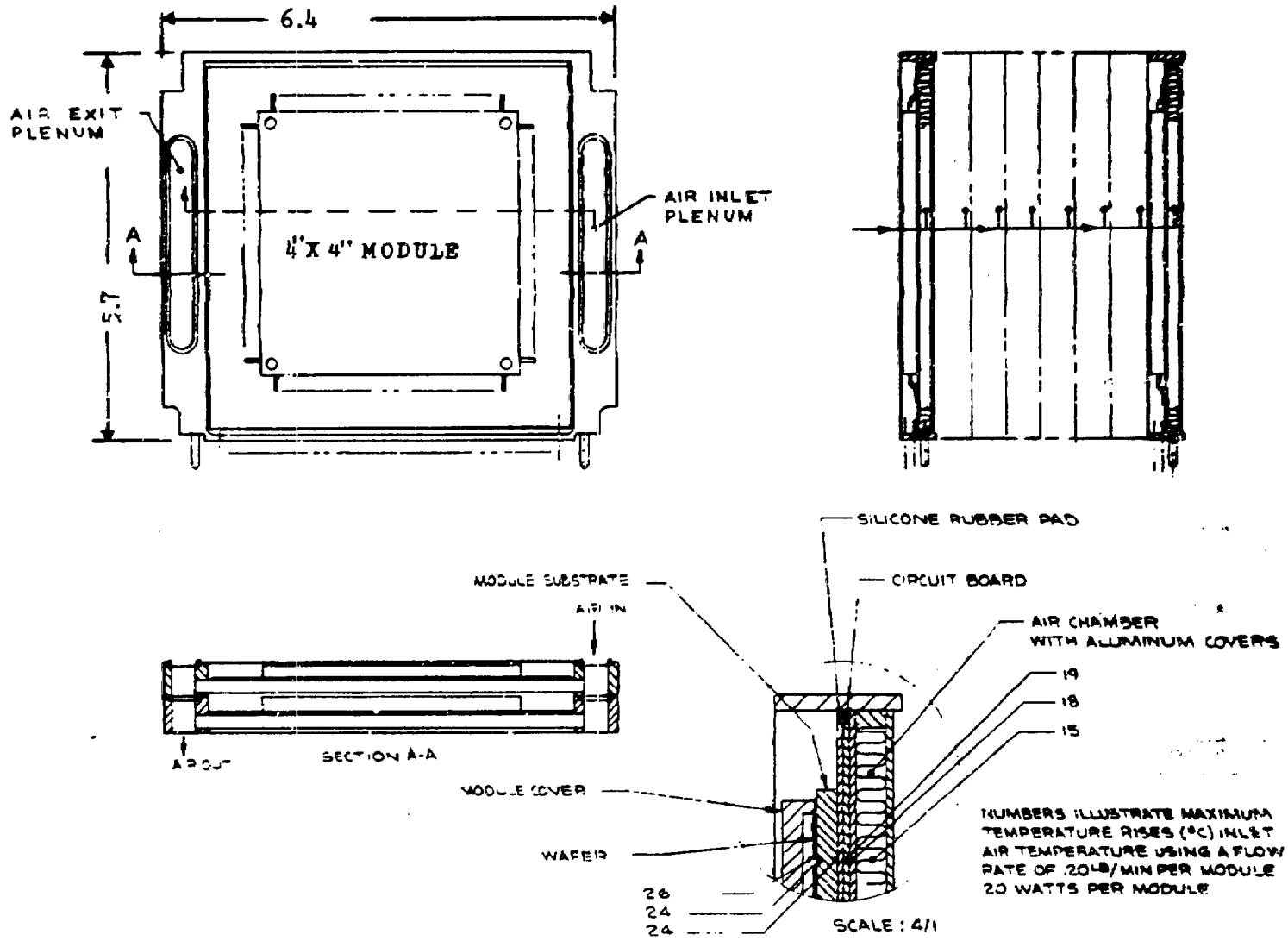
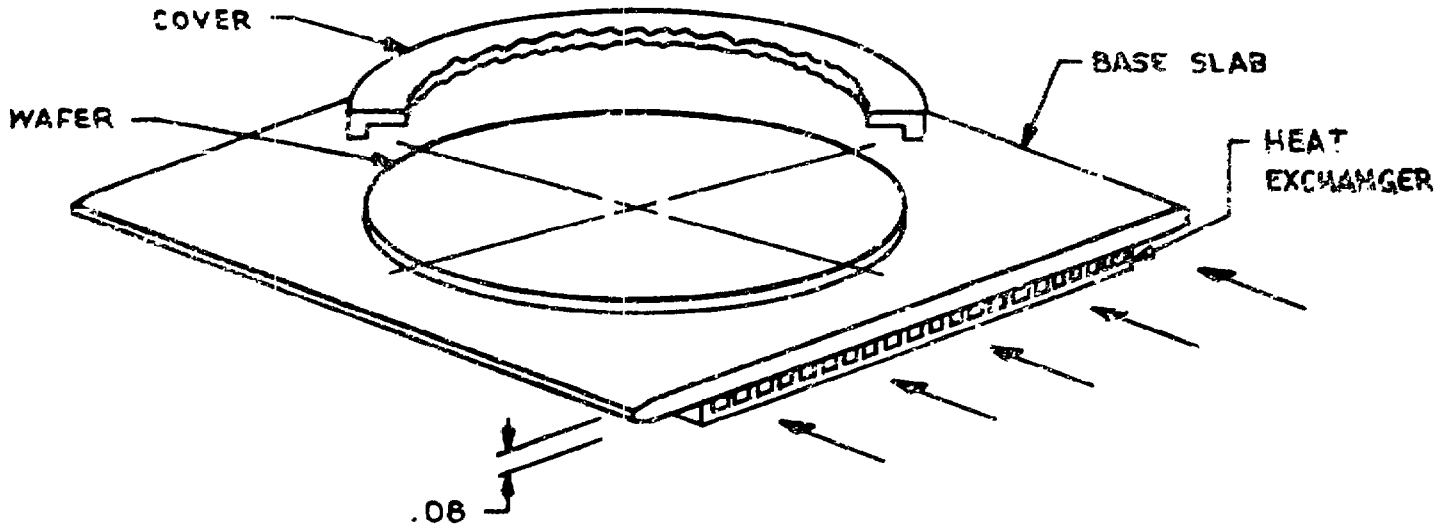


FIGURE 5 DIRECT COOLING CONFIGURATION

TABLE 1. MODULE DESIGN COMPARISON TABLE

DESIGN APPROACH NO.	MODULE									HIGHER LEVEL PACKAGE 12 MODULE SYSTEM		
	DESCRIPTION	SIZE	VOL. IN^3	WEIGHT	MAX. COMP. TEMP. 32°C COOLING AIR AT .2LB/MIN	MAX. COMP. TEMP. 32°C COOLING AIR AT .1 LB/MIN	RESONANT FREQUENCY	EXTERNAL CONNECTIONS	MODULE TO BOARD SOLDER CONNECTION	APPROXIMATE OUTLINE DIMENSIONS	APPROXIMATE VOLUME	APPROXIMATE WEIGHT
I	CONDUCTIVE COOLING FIGURE 7	5.1 x 5.7 x .40	13.8	.60	100°C	130°C	400	PRESSURE CONTACT 50-150LB OR ZERO FORCE CAM OPERATED	300	7.8 x 4.5 x 7.3	252 IN^3	11.0 LBS.
II	DIRECT COOLING FIGURE 6	6.4 x 5.7 x .50	18.2	.68	55°C	70°C	400	PRESSURE CONTACT 50-150 LBS OR ZERO FORCE CAM OPERATED	300	6.4 x 6.5 x 8.5	365 IN^3	11.5 LBS.
III	INTEGRAL HEAT EXCHANGER INTEGRATED FIN FIGURE 1	4.0 x 4.0 x .48	6.4	.48	90°C	62°C	2100 [illegible]	ZERO FORCE CAM OPERATED CONNECTOR	0	4 7/8 x 5.6 x 6.8	190 IN^3	6.8 LBS.

TABLE 2. WAFER INTERFACE TEMPERATURES - 20 WATT MODULE, 30°C INLET AIR TEMPERATURE



MATERIAL	AL_2O_3 BASE-AL_2O_3 HEAT EXCHANGER				BeO BASE-BeO HEAT EXCHANGER				AL_2O_3 BASE-BeO HEAT EXCHANGER			
FIN	CONTINUOUS		INTERRUPTED		CONTINUOUS		INTERRUPTED		CONTINUOUS		INTERRUPTED	
COOLING AIR LBS/MIN	0.1	0.2	0.1	0.2	0.1	0.2	0.1	0.2	0.1	0.2	0.1	0.2
AVG. WAFER TEMPERATURE	65.1	57.0	59.7	49.7	62.9	53.3	59.4	48.0	63.9	53.9	60.5	48.7
AXIAL GRADIENT	18.2	15.3	17.0	14.2	3.2	3.0	3.1	3.1	5.8	4.8	5.3	5.1
MAX WAFER TEMPERATURE	72.3	70.9	66.0	62.3	63.8	53.8	61.0	48.5	65.3	55.5	62.7	50.6

DETAIL DESIGN AND FABRICATION

Having described the general configuration, thermal characteristics, and material tradeoffs, bonding and module sealing considerations will be highlighted.

Table 3 summarizes the various material and sealing combinations that were considered. The dry-pressed solid, ceramic slab employing a Kovar or alumina cover proved to be optimum for the following reasons:

- Minimum sealing surface is introduced
- Maximum heat transfer area is available
- Limited manufacturing complications are introduced

COVER SEAL

Units employing Kovar and ceramic covers have been designed and fabricated. Cross sections are illustrated in Figure 6. A weldable Kovar cover is preferable since heating can be confined to the rim area during sealing. A unit which has been laser welded is illustrated in Figure 7.

WAFER CONNECTIONS AND ASSEMBLY

Interconnections to test slabs have been made using ultrasonic bonding. Ball or thermal compression bonding can be utilized also. Other techniques which employ batch interconnection processes utilizing kapton-mounted aluminum flat foil leads are in the developmental stage.

MODULE TEST

Six modules have been delivered to NAFI for evaluation and environmental testing. Favorable thermal and structural test results have been obtained. A detailed test report is currently being prepared.

CONNECTOR

The Kearfott Division of the Singer Company has developed and delivered to NAFI a 152-Pin Cam Operated Zero

TABLE 3. MODULE-MATERIAL COMBINATIONS

COMBINATION NO.	BASE	COVER	BASE COVER SEAL	LEAD SEAL	HEAT EXCHANGER
1	KOVAR	KOVAR	RESISTANCE WELD LASER OR ELECTRON BEAM WELD SOLDER COLD WELD	GLASS	CERAMIC KOVAR
2	KOVAR	CERAMIC	SOLDER	GLASS	CERAMIC KOVAR
3	CERAMIC-KOVAR SLUG -KOVAR SEAL RING	KOVAR	SAME AS NO. 1	CERAMIC GLAZE	CERAMIC KOVAR
4	CERAMIC-KOVAR SLUG	CERAMIC	SOLDER-METALIZED SEAL RING	CERAMIC GLAZE	CERAMIC KOVAR
5	CERAMIC-KOVAR TAPE SEAL RING	KOVAR	SAME AS NO. 1	CERAMIC TAPE	CERAMIC KOVAR
6	CERAMIC-TAPE	CERAMIC	SOLDER-METALIZED SEAL RING	CERAMIC TAPE	CERAMIC KOVAR
7	CERAMIC-KOVAR DRY PRESS SEAL RING	KOVAR	SAME AS NO. 1	CERAMIC GLAZE	CERAMIC KOVAR
8	CERAMIC-DRY PRESS	CERAMIC	SOLDER-METALIZED SEAL RING	CERAMIC GLAZE	CERAMIC KOVAR

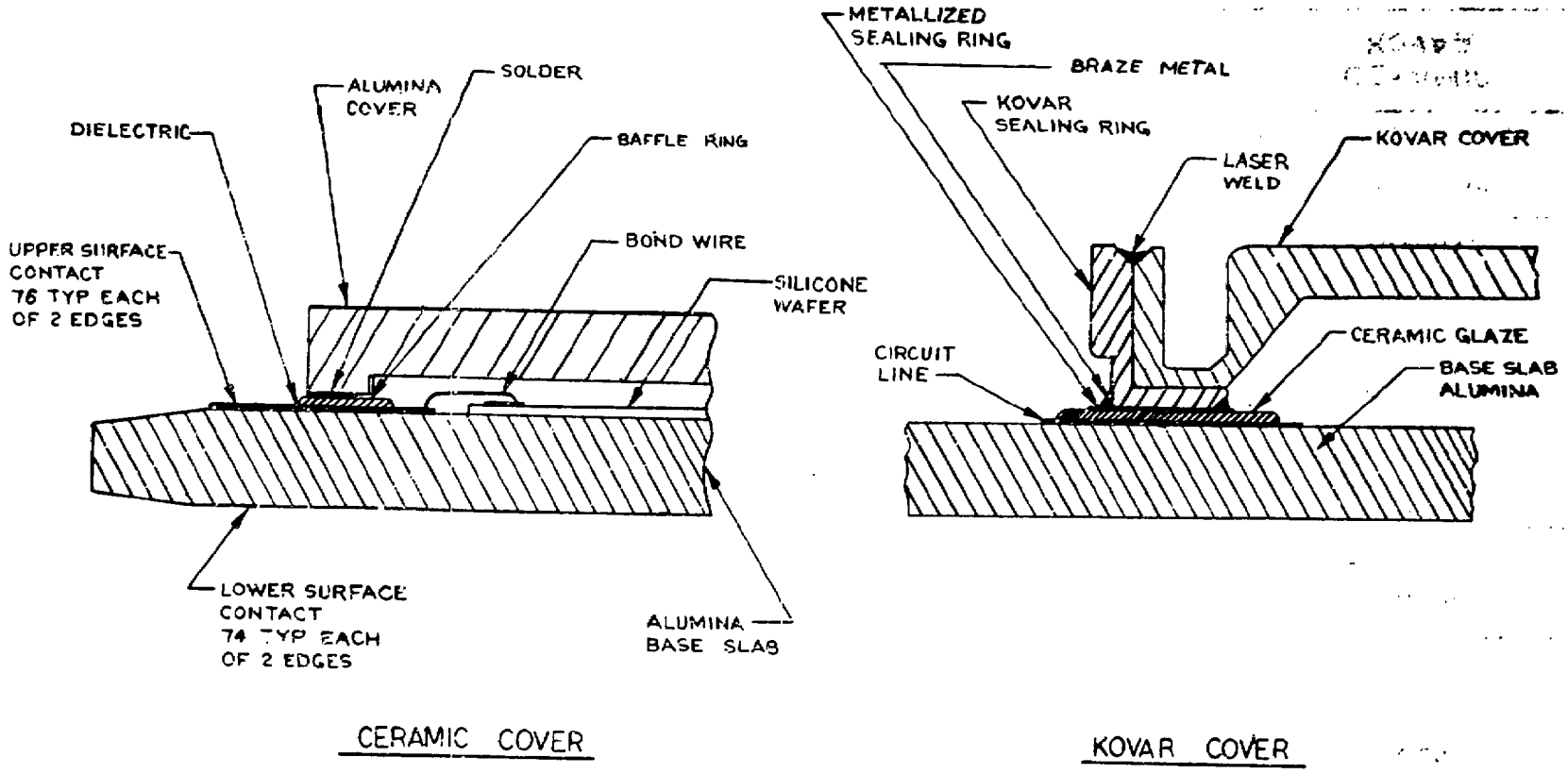


FIGURE 6 CROSS SECTION SEAL AREA

FIGURE 7 KOVAR COVER MODULE

Insertion Force Connector. The connector provides interconnection between the Building Block Module and the backboard wiring system of the Higher Level Package.

The connector's unique features are:

- Zero insertion force
- Five to ten-ounce contact pressure
- Less than 0.002 ohm contact resistance
- Interlock mechanism that precludes operation if the module is not properly seated, and precludes module removal prior to contact release
- Cam loading during contact closure

The connector is illustrated in Figure 2 in the closed position. A design trade-off study was conducted which considered tolerance effects, single cam designs and alternate contact arrangements (see Figure 8). The final design which preserves wiping action is illustrated in Figure 9 along with the contact arrangement and interlock mechanism. Note that the contacts are on .05 centers and the envelope dimensions are 4.75 inches long x 0.60 inches high x 0.50 inches wide.

HIGHER LEVEL PACKAGE - DESIGN APPROACH

The Higher Level Package with its modular approach is illustrated in Figure 3. A set of Cam Operated Connectors service each module. A series of through bolts clamp the stacked connectors between the front and rear panel to form a rigid frame for the overall package. Spacers can be used to accommodate various module widths while compensating for tolerance accumulations.

GUIDING, KEYING AND INTERLOCK

Guiding of the Building Block Module into the Higher Level Package is provided by guide slots in the connector block. Keying pins and bushings preclude improper location. There are 128 possible combinations available.

Mislocation or partial seating of the module prevents operation of the connector cam. Similarly, the system cover cannot be seated unless all cams are in the closed position.

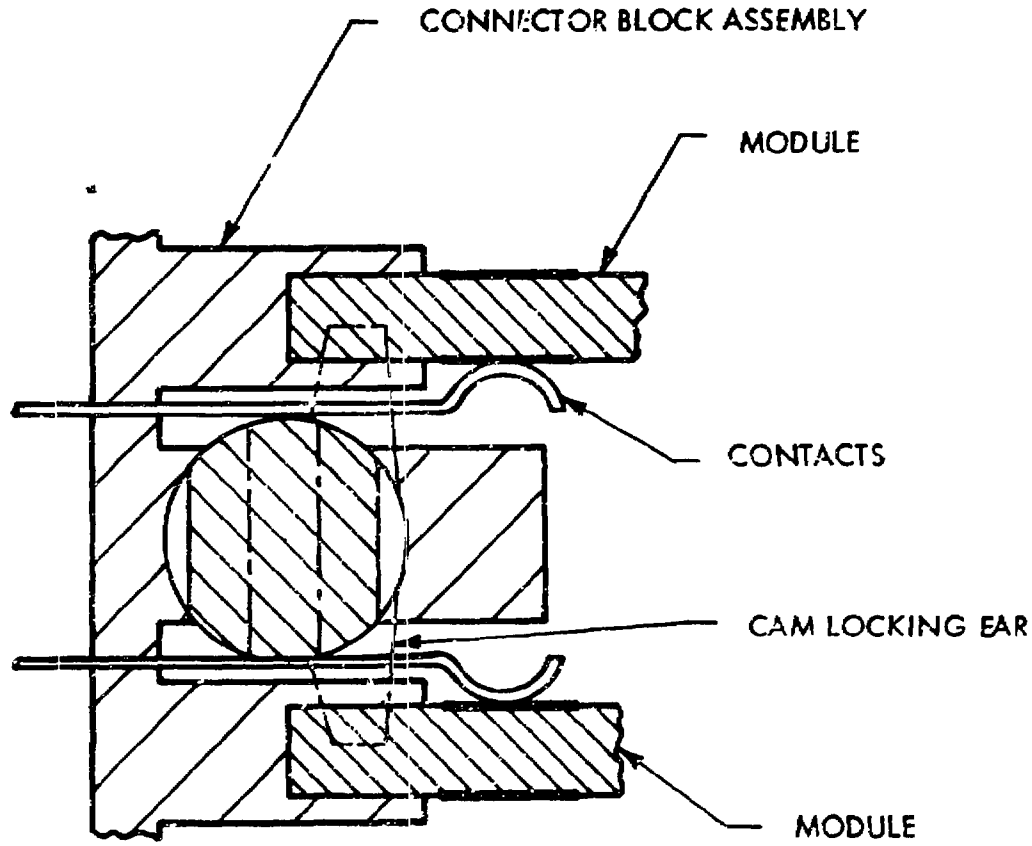


FIGURE 8 SINGLE CAM CONNECTOR

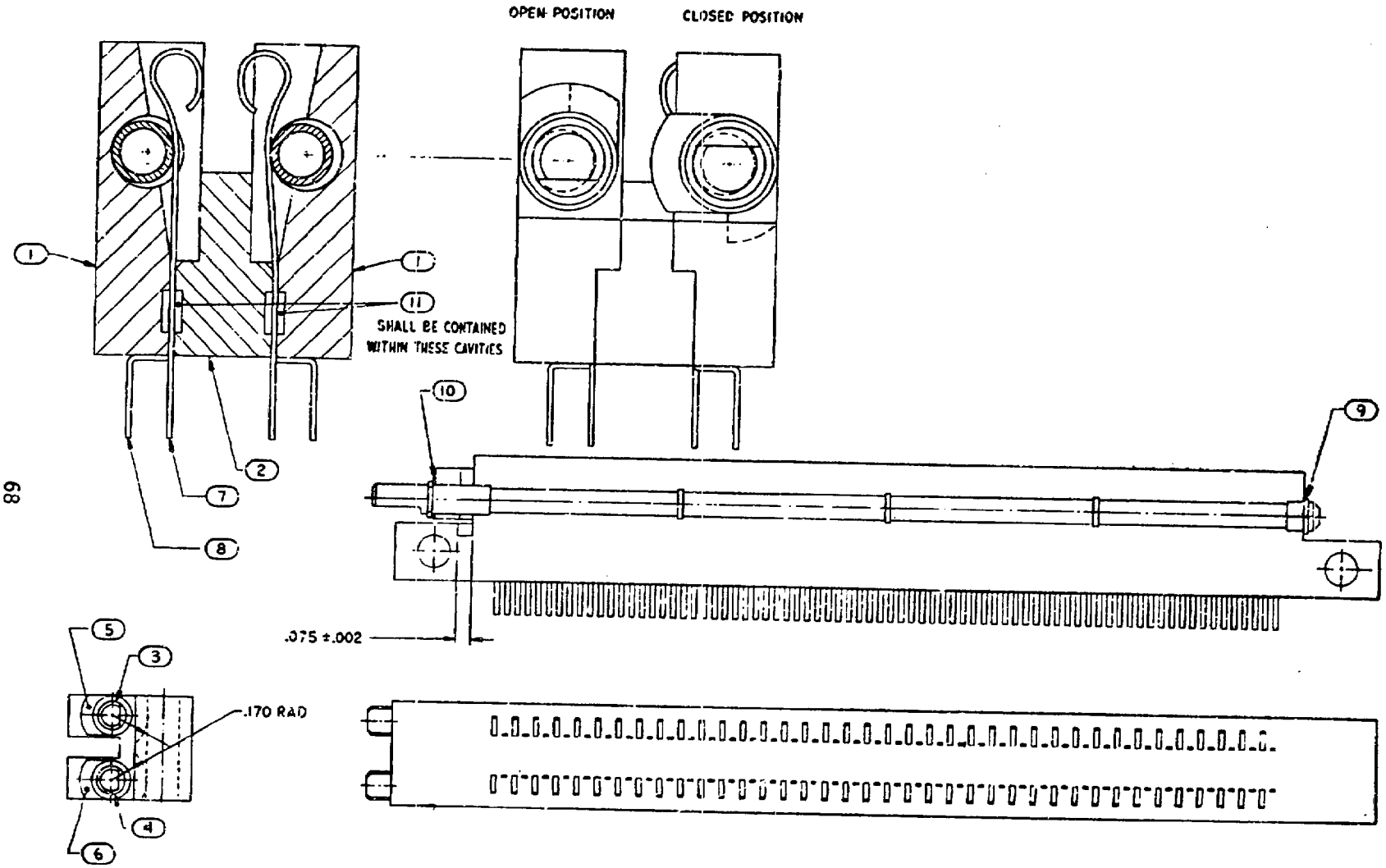


FIGURE 9 CAM OPERATED CONNECTOR ASSEMBLY

COOLING AIR FLOW

Cooling air is circulated through the modules using a parallel air distribution method, wherein each module receives inlet air having the same temperature. Air enters at the front panel of the Higher Level Package (Figure 3), passes through the modules via the lower air distribution plenum, and exits via the upper air plenum. Molded gaskets prevent cooling air leakage at the module/plenum interfaces.

The Higher Level Package design, in combination with the Building Block Module, can be optimized to meet various cooling air pressure drop and flow rate requirements. Maximum permissible component operating temperatures, to a large extent, determine the cooling air flow rate and temperature. Pressure drop characteristics are determined by the module heat exchanger area, fin design, cooling air velocity, and the ratio of the Higher Level Package duct area to the module heat exchanger cross section. A series of design curves has been generated to show the interrelation of these parameters. Curves of this type are used to optimize the duct size of the Higher Level Package and to establish the type and optimum size of the heat exchanger to be used for the Building Block Module in a particular application.

Figure 10 illustrates the component temperature rise above the inlet air temperature as a function of cooling air flow for a 20 watt module having BeO and Al_2O_3 heat exchangers with .065 inch and .130 inch high fins. Figure 11 indicates anticipated pressure drops for Higher Level Packages for various distribution plenum sizes and module fin heights.

INTERCONNECT

Connections from the connector block assembly to the front connector panel can be made via a multilayer motherboard and flexprint as illustrated in Figure 3. A motherboard is located in the back of each connector block. Communication between the motherboards can be made at the front panel or by a circuit board located between a series of modules. If desired, the motherboard interface card can have an orientation and contact arrangement analogous to a Building Block Module and if desired can be permanently installed. The motherboards can incorporate a micro-strip design.

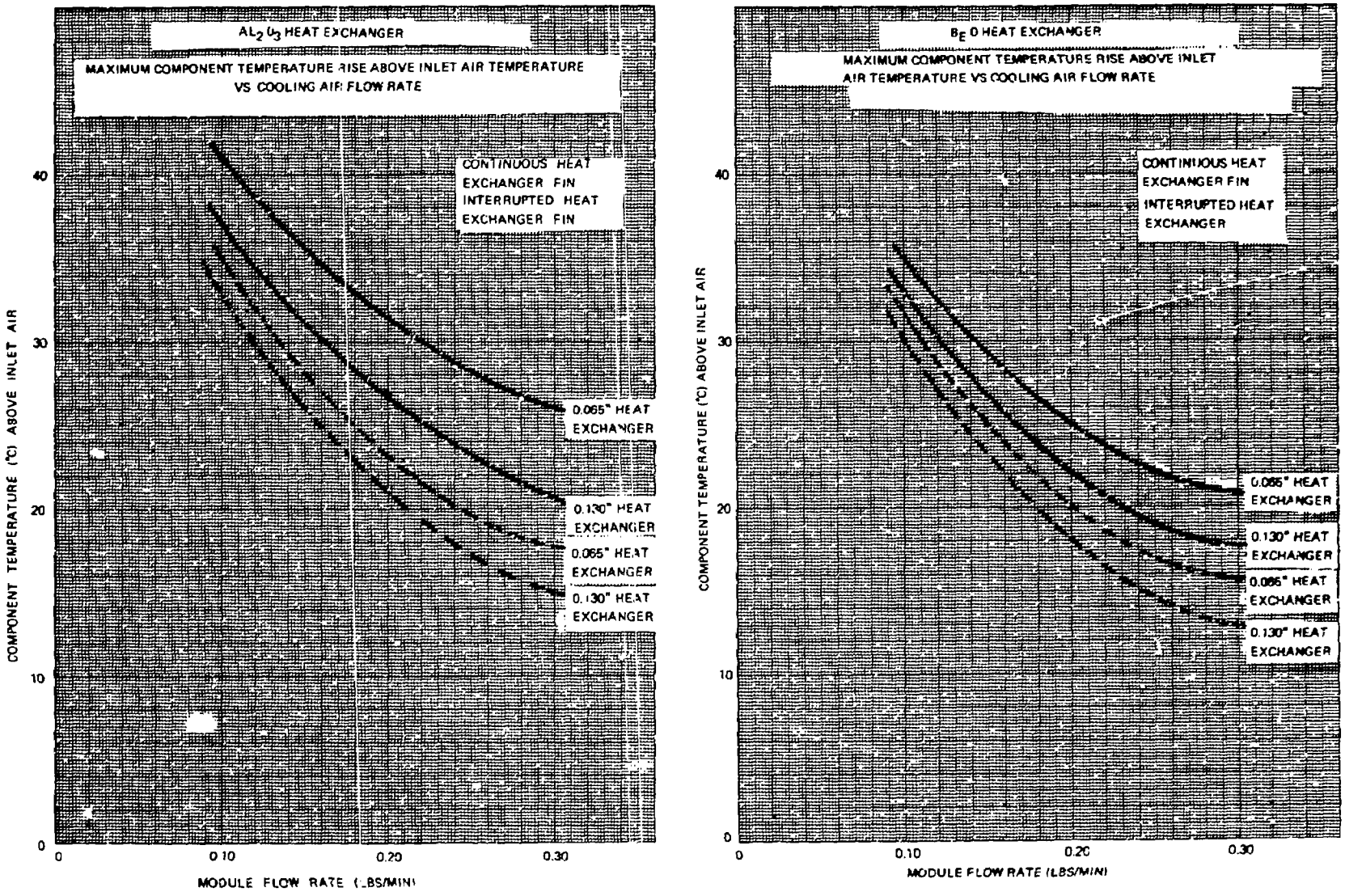


FIGURE 10 COOLING AIR FLOW RATE VS TEMPERATURE RISE

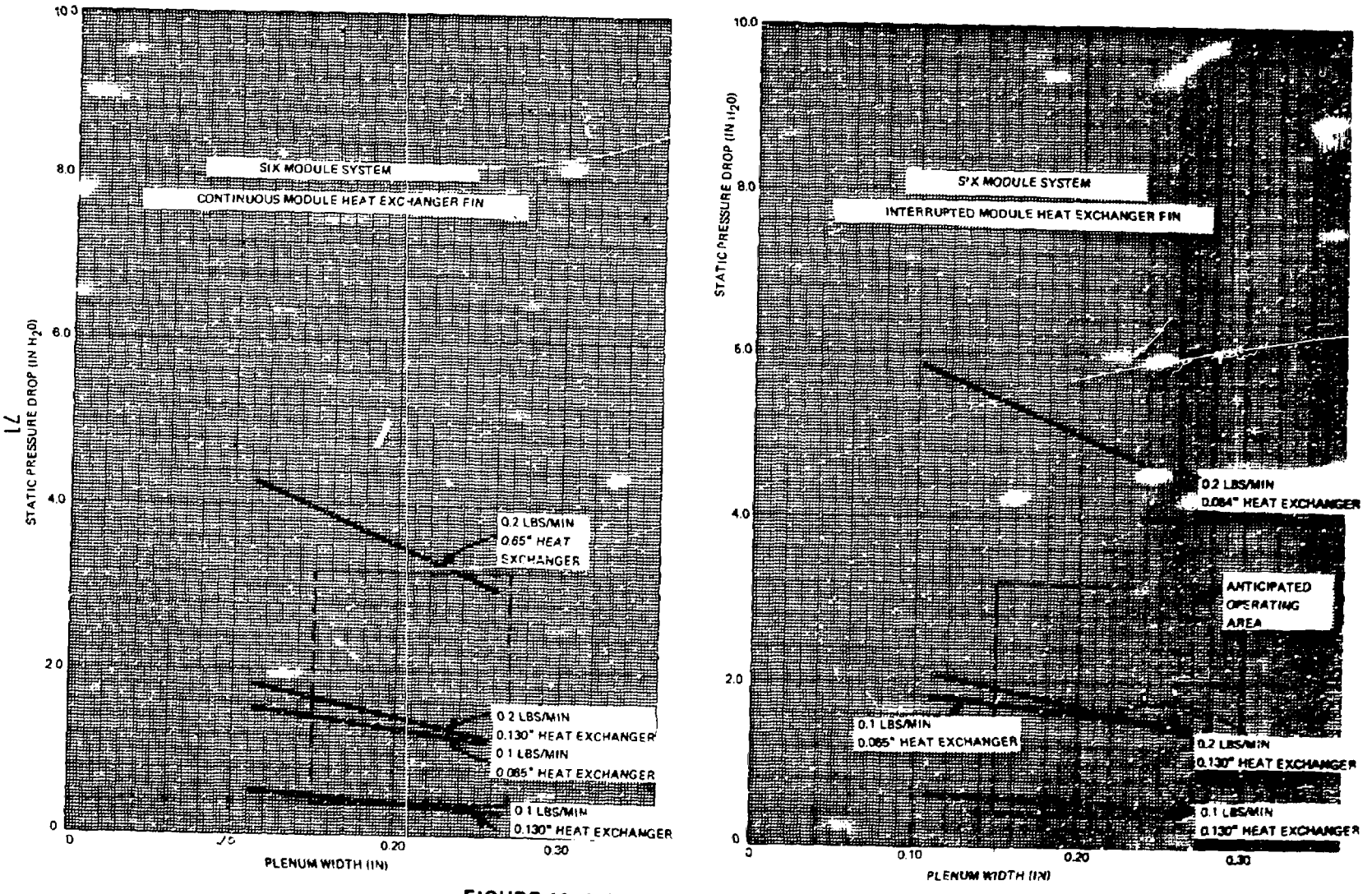


FIGURE 11 MODULE SYSTEM PRESSURE DROP

TV RESOLUTION SOLID-STATE ARRAY CAMERA

by

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Abstract

Using a 200,000 element silicon phototransistor matrix, a recently developed solid-state array camera provides TV compatible video and resolution. This paper describes the design and implementation of the system's hybrid bare chip circuitry, and its overall operational characteristics.

Introduction

Over the past decade, working under NASA, Huntsville contract NAS 8-5112, Westinghouse has pursued an evolutionary development program directed toward production of an all solid-state image converter having resolution capabilities equivalent to those provided by commercial television. This effort has led most recently to the successful fabrication of high density row-column organized sensor matrices containing nearly a quarter million individual phototransistors, and to the deployment of one of these arrays in the engineering model camera system shown in Figure 1.

As configured this novel solid-state array camera is completely self-contained needing only a source of 110 volt ac power, is totally molecular in design using state-of-the-art silicon technology devices throughout, and is output interface compatible with conventional TV studio type display monitors. Functionally and physically it is

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divided into two distinct sections: the image converter mainframe, which is 10" x 10" x 2" and contains the 400 x 500 element photosensor array and its LSHI (large scale hybrid integration) bare chip packaged scanning and control electronics: and the detachable supply/processor subunit, which is 10" x 3" x 2" and contains the multiple-voltage power converters and EIA format video processor.

SENSOR ARRAY

The photodetector employed in this system is a monolithic array of 200,000 phototransistor elements organized in an x-y access matrix of 400 rows and 500 columns. It is fabricated using standard planar epitaxial and diffusion processing techniques on a specially prepared high quality 2-½ inch diameter single crystal silicon wafer. A photograph of a finished array is presented in Figure 2. Surface dimensions of the mosaic consist of 2.0-by-2.5 mil center-to-center spacings of emitters and collectors, respectively, for a total functional detector area of one square inch. The effective area coverage aspect ratio of the sensor matrix is 1:1 and leads to a 100% modulated bar chart limiting resolution of 200 line pairs per picture height in the vertical direction and 250 line pairs per picture height in the horizontal direction.

Individual elements in the array are pulse biased for operation in the charge-storage (integration) mode by cross-coincident activation in row/column access line pairs. The output signal charge available from respective phototransistors follows the integration mode relationship

$$Q_{signal} = (1 + g)\,[Q_{io} + Q_a\,(\tau_L/\tau_i)]\,(1 - e^{-\tau_i/\tau_L})$$

total output charge	output transistor gain	initial stored charge	photon generated factor	recombination loss factor	exponential accumulation factor

where τ_i is the integration period and τ_L is the junction leakage time constant. Conversion of input irradiance on any element basis is intrinsically linear over greater than three decades, but the usable dynamic range of the aggregate array is typically limited to about two decades by interelement non-uniformities.

CAMERA SYSTEM

To divorce the primary functions of image sensing and scan conversion from the sub-functions of power conversion and signal format-

ting, the PICTURE 45* camera system is divided into two distinct units. The supply/processor sub-unit module, which interfaces with the image converter through a 15 pin connector, serves as an electrical buffer to the outside world for both raw input power and final output signal video. The camera mainfram, which is designed to have a basically planar architecture, houses the readout electronics in the jig-saw puzzle interrelated layout of compartmentalized LSHI substrates shown in Figure 3. Optical coupling to the centrally located photosensor monolith is provided by a 50mm f/1.2 lens. Rear surfaces of the mechanical frame are made flat and projection free to facilitate mounting on a domicile wall or vehicle bulkhead like a picture frame.

Electrical outputs from the camera mainframe are in the form of raw, scan-coverted serial image video and separate blank and sync pulses. The signals may be used independently if desired, or they can be passed along to the remotely programmable sub-unit where the processor combines them into a 1 volt peak amplitude EIA format composite TV video signal which is then output in both positive and negative polarity push-pull form. Scan synchronization for the system is provided by an Apollo moon camera type digital sync generator while master clocking is selectable from either an internal 9.45 MHz crystal controlled source, which produces the U. S. standard 525 line 60 interlaced fields-per-second TV scanning format, or an externally variable source, which permits tailoring the system frame rate to meet particular application requirements.

Distinctive, eighth order time-shared signal acquisition followed by high speed parallel-to-serial analog multiplexing is employed in the 45 camera to allow sufficient per-element sampling dwell time while successive data bits are processed from the detector mosaic. Extensive use is made of low power TTL devices in the timing circuitry to assure adequate sequencing speed capabilities with a moderation of power requirements. Sectional compartmentallization of the system electronics is established on the basis of functional independance and circuit modularity. Counter/decoder sequencing logic designs are employed in preference to shift register schemes due to their greater reliability and the availability of IC logic chip functions.

Implementation of the sub-sectional electronics follows hybrid bare chip fabrication principals. Individual substrates are formed from electronic grade alumina having an 8 micro inch surface finish and bimetal chrome-gold conductors. Interconnections between adjacent substrates, between the sensor mosaic and its peripheral interface circuitry, and between IC logic chips and their substrate conductor runs are made by thermo-compression ball-and-stitch bonded flying wire gold leads. Opposing side circuit design redundancy and layout mirroring are employed to eliminate crossover lines and simplify substrate processing, construction, and testing. Two circuitry sections are retained in discrete p.c. board

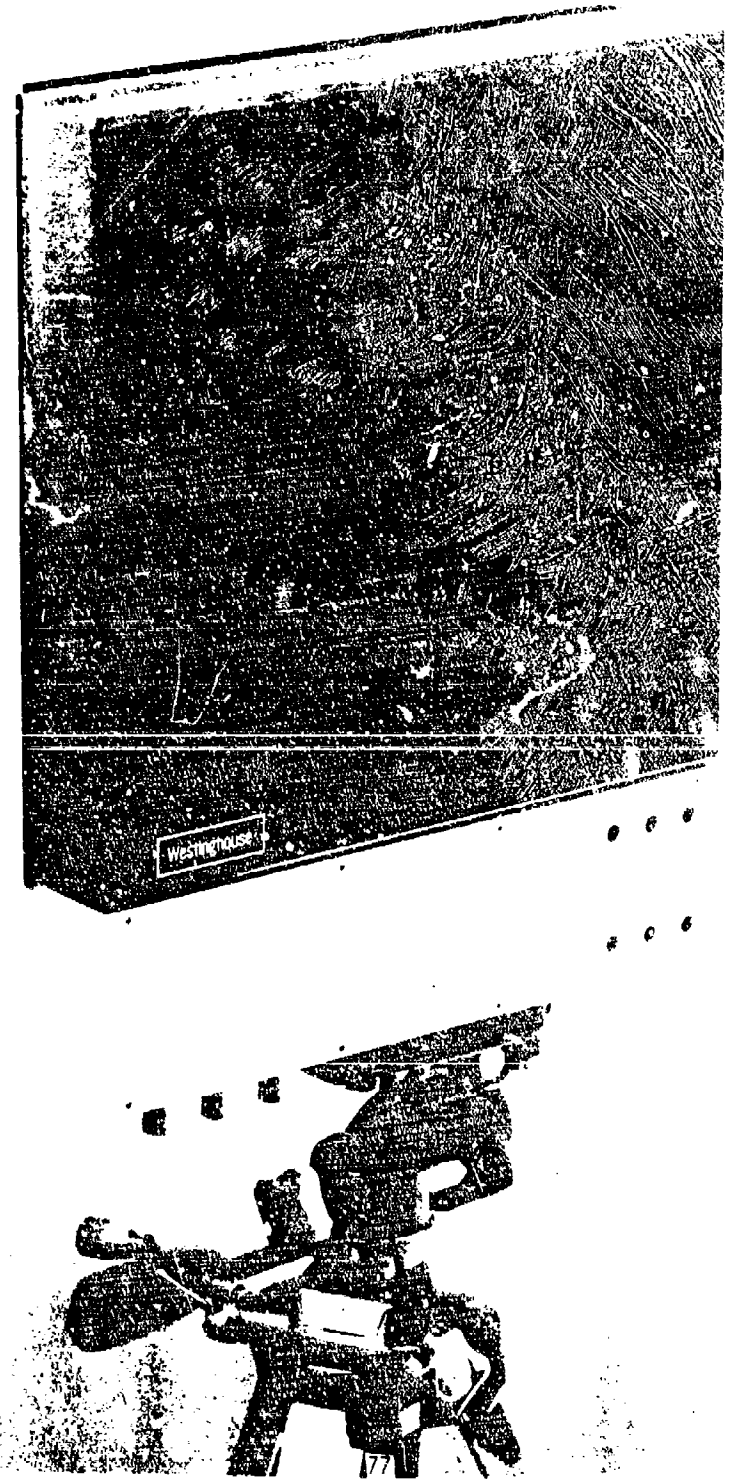
*PICTURE 45 is the abbreviated name applied to the engineering model 400 x 500 element solid-state array camera. It is derived as a contraction of Photon Image Converter w/Television Universal REsolution using a 400-by-500 element sensor mosaic.

packaged form due to tye type of components they contain.

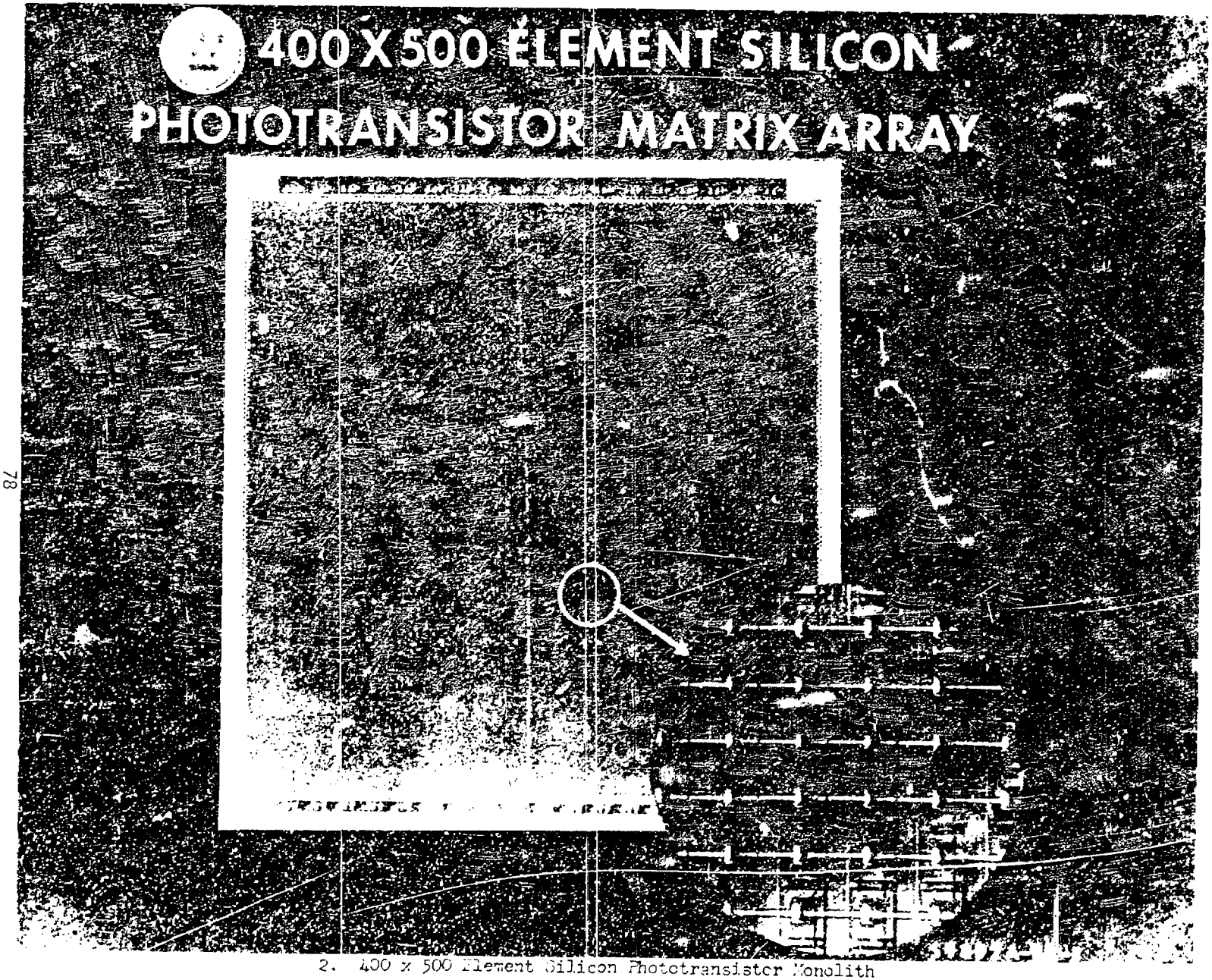
The non-enhanced conversion transfer range typically realized by the camera for irradiance in the range of 400 to 1000 nanometers (10% spectral response points) is seven shades of grey, with the minimum usable irradiance level of approximately 0.2 $\mu W/cm^2$ at 30 Hz frame rates being limited primarily by scan conversion uniformities. Signal information bandwidth, with internally controlled scanning, is 4.5 MHz — identical to that for commercial television and resulting in the same qualitative resolution in line-pairs.

SUMMARY

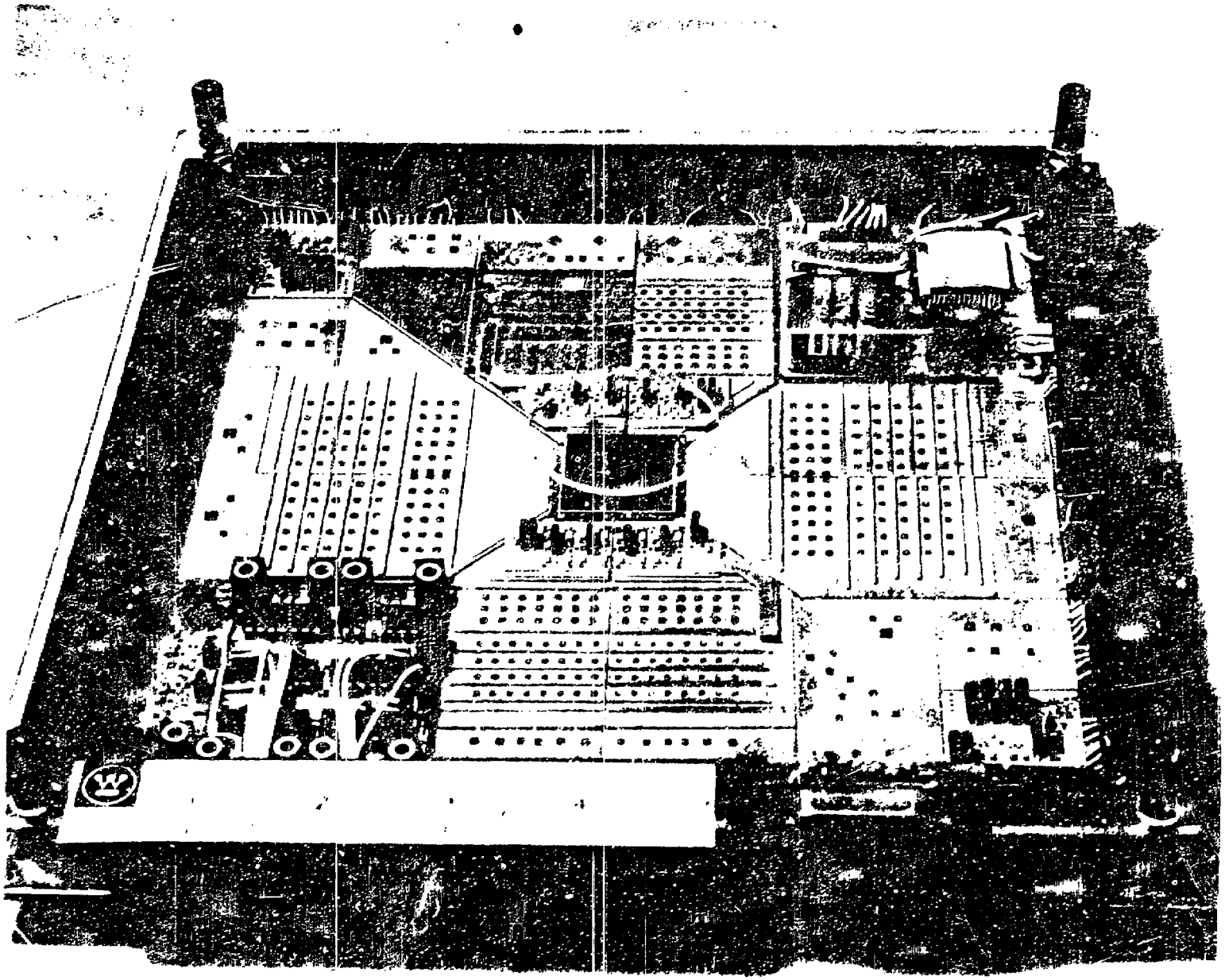
With the level of resolution attainable by integrated half-tone images now being on a par with broadcast television, totally solid-state imaging is seen to have come-of-age. While input power and composite weight of the present engineering model system are moderately high -- on the order of 12 Watts and 5 pounds — both factors are readily reducible to levels of about 1 Watt and 1 pound, or less, in next generation molecular cameras by capitalizing on recent MOS technology improvements. Over the next decade refined versions of solid-state array cameras are therefore expected to supplant conventional high vacuum systems in many critical military, industrial, and aerospace applications. Following consociate technology advances in the human sciences, they should also see greatly expanded usage in the biomedical field; particularly in the area of ambulatory aids for the blind.



1. Engineering Model TV Resolution Solid-State Array Camera



2. 400 x 500 Element Silicon Phototransistor Monolith



3. Large Scale Hybrid Integration (LSHI) Camera Packaging

AN APPLICATION OF MICROELECTRONICS TO THE REMOTE LENS OF THE SKYLAB COLOR TELEVISION CAMERA

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ABSTRACT

A remotely controlled adjustable lens assembly for the Skylab color television camera was developed using multichip hybrid packaging techniques. Three thick film packages were used to contain over 150 discrete chip components which performed all of the circuit functions. The entire lens assembly is mounted on the Skylab field sequential color television camera.

INTRODUCTION

The remote lens of the Skylab color television camera is attached to the camera when the camera is being prepared for placement on an extendible observation boom. The adjustable lens functions of the camera, when extended over 20 feet from the exterior surface of the Skylab station, will allow the astronauts to remotely observe outside portions of the space station. Coded control signals are sent up the boom by a four conductor cable and all lens functions consisting of adjustable focus, zoom, and iris are decoded by the circuitry in the three multichip hybrid packages located in the lens assembly. Reversible stepper motors, driven at the vertical sync rate in order to eliminate picture interference, are used to drive the lens functions. All of the circuitry has been placed into multichip hybrid packages since there is no space for discrete component wiring. The following sections of the paper will discuss the system design of the remote lens along with the microelectronic design of the circuitry.

SYSTEM DESIGN

The Skylab remote control lens system consists of four parts as shown in Figure 1, the encoder, the receiver, the decoder, and the lens function motor drivers. The encoder which is located within the Skylab space station converts a mechanical switch input (e.g. iris-close) to a binary coded signal suitable for a high (28V) two level, four wire transmission system. The receiver located on the remote lens then converts the signal to T^2L signal levels since standard T^2L ICs are used in the decoder. Decoding circuitry using the camera's vertical sync as a clock, stores four bits of switch information, updating the storage registers at the vertical sync rate of 60 Hz. The four bits are then decoded and the commanded switch function executed in the lens unit. (e.g. the iris closes)

The system requires 7 commands for motors (iris open, iris close, focus in, focus out, zoom in, zoom out, neutral) and four commands for Automatic Light Control (ALC). One of the design rules was that only one motor command may be given at any one time, and ALC information can not be disturbed by the application of a motor command. There are 28 different commands that may be given by the switches with only four signal lines and 16 possible states for the command lines. Hence a capability to remember commands is required. The system operates in two modes (1) motor command, (2) ALC command. When a motor command is given the last ALC information received is retained in memory. This prevents the ALC from being changed whenever a lens motor is being operated. When ALC information is being transmitted the ALC memory is continuously updated (at the vertical sync rate) and the motors are inhibited from operation.

The coding follows directly from the description. One signal line is used for mode definition; it indicates either an ALC command or a motor command. Two lines are used as address lines indicating which motor has been commanded or which ALC position has been commanded. The remaining line is used only as a direction indicator for the motors.

The transmission of the data is done at a high logic level in order to improve the system noise margin. Line drivers in the encoder are transistor switches presenting either a low impedance thru the return line (0) or a 20KΩ collector load (1) to the 28V supply line. Direct coupled line receivers in the remote lens, filter the input signal and compare the filtered signal to a reference that is equivalent to approximately one half of the 28V supply voltage. If the signal is greater than the reference, a "one" is received; if it is less a "zero" is received. The outputs of the line receiver comparators are at T^2L levels and are compatible with the decode circuitry. The line receiver for the vertical sync pulse is a transformer-coupled comparator with hysteresis in order to maintain isolated ground for the T.V. system. Vertical sync pulses are used in the remote lens assembly to clock all information into registers and also to provide a 60 Hz clock to generate the 4 phases for the motor drive.

Switch position information bits are clocked into the decoder with the vertical drive pulse. If an ALC command is received the two address lines are clocked into holding registers and the motors are inhibited. If a motor command is present the ALC information remains unchanged and the address lines are decoded to determine which motor has been commanded. The direction bit controls an up-down counter whose outputs are decoded to give the phase drive pulses for the motors.

The lens motors are stepper motors requiring 2 alternating current square waves 90° out of phase, either leading or lagging depending on rotation direction. By using four drivers which can source or sink current the proper drive currents can be applied from a single positive supply.

MICROELECTRONIC DESIGN

Packaging requirements of the skylab color camera remote lens system placed severe limitations upon the quantity of electronic circuitry. Since the remote lens would be attached to the front of the camera, all electronics would have to be within the lens housing. All of the components in the breadboard design were discrete and because of the quantity of parts it was obvious that a discrete assembly would not be feasible. A microelectronic hybrid packaging technique, incorporating a specially designed monolithic ceramic package was used to relieve the packaging problem.

After finalization of the breadboard design, there followed a functional breakdown of the circuits into probable packages. Further refinement of this was for minimization of both inter and intra package connections, elimination of circuit interactions and duplicities, equalization of chip densities, and restriction of power dissipation to within package limits. Each multichip package substrate was then laid out according to existing techniques for manufacturability and reliability. Three multichip hybrid packages were the resultant of this effort.

The circuit layouts incorporated an initial ground plane construction for the elimination of ground loops and incorporation of low resistance ground paths. The ground plane was cut away from critical loads to prohibit capacitive coupling. One or more layers of conductors were then deposited intersperced with dielectric insulators. Bonding of chips, which included thick and thin film resistors, capacitors, diodes, transistors, and various integrated circuits, commenced and wirebonding of components terminated the manufacturing process.

After passing numerous functional circuit tests, the substrates where soldered into a special! designed package featuring a monolithic sandwich construction with a hermetically sealed lid, and subjected to more testing, thermal cycling, and power aging. Figure 2 depicts the layout of the receiver package which is composed of LM111 comparators, thick film chip bias resistors and chip bypass capacitors on a three layered thick film substrate. In this package the iris, focus, and zoom switch control functions from the encoder are converted into digital information.

These signals then reach the decoder package shown in Figure 3 where the information is converted into clocked pulses coded for the different motor functions and for the ALC information. This package consists of almost all digital integrated circuits on a five layer thick film substrate.

The motor drive package is the third package. As seen in Figure 4. It is composed of thin film resistors, chip ceramic capacitors, and chip transistors on a three layer thick film substrate. The currents and voltages necessary for driving the three motors are generated in this package.

Function isolation in each package is evident in that the low level commands are transformed into digital information before interfacing with another package. This information, once it leaves the receiver is stored immediately upon entering the decoder. Then the digital command and inhibit pulses are formed before leaving the package. Lastly, the motor control circuitry with its noisy switching and driving circuitry is kept isolated from the decoded signals.

Power dissipation is minimal in both the encoder and decoder packages, but the motor drive dissipates nearly a watt having close to one hundred chips for its implementation.

SYSTEM IMPLEMENTATION

The remote lens assembly is illustrated in breadboard form in Figure 5. All of the receiver decoder and motor driver circuitry as illustrated fits into the lens assembly when packaged in microelectronic form. Figure 6 shows the final assembly of the multichip hybrid packages for the remote lens assembly. The two large packages are 1" X 2" and contain all of the decoding circuitry and motor drive circuitry. Also shown is a smaller 1" X 1" package which contains the line receiver comparators. These packages are mounted on multilayer printed circuit boards and are contained within the lens assembly housing. Extensive temperature evaluation has been performed on the MHPS and full circuit operation

has been verified over -55°C to +125°C. Figure 7 is the complete Skylab Remote TV Camera Assembly.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the contribution of L. L. Niemyer, S. M. Engle, and L. A. Thomas for their help and technical assistance. This design and development was supported by the National Aeronautics and Space Administration, Manned Spacecraft Center contract number NA59-12429.

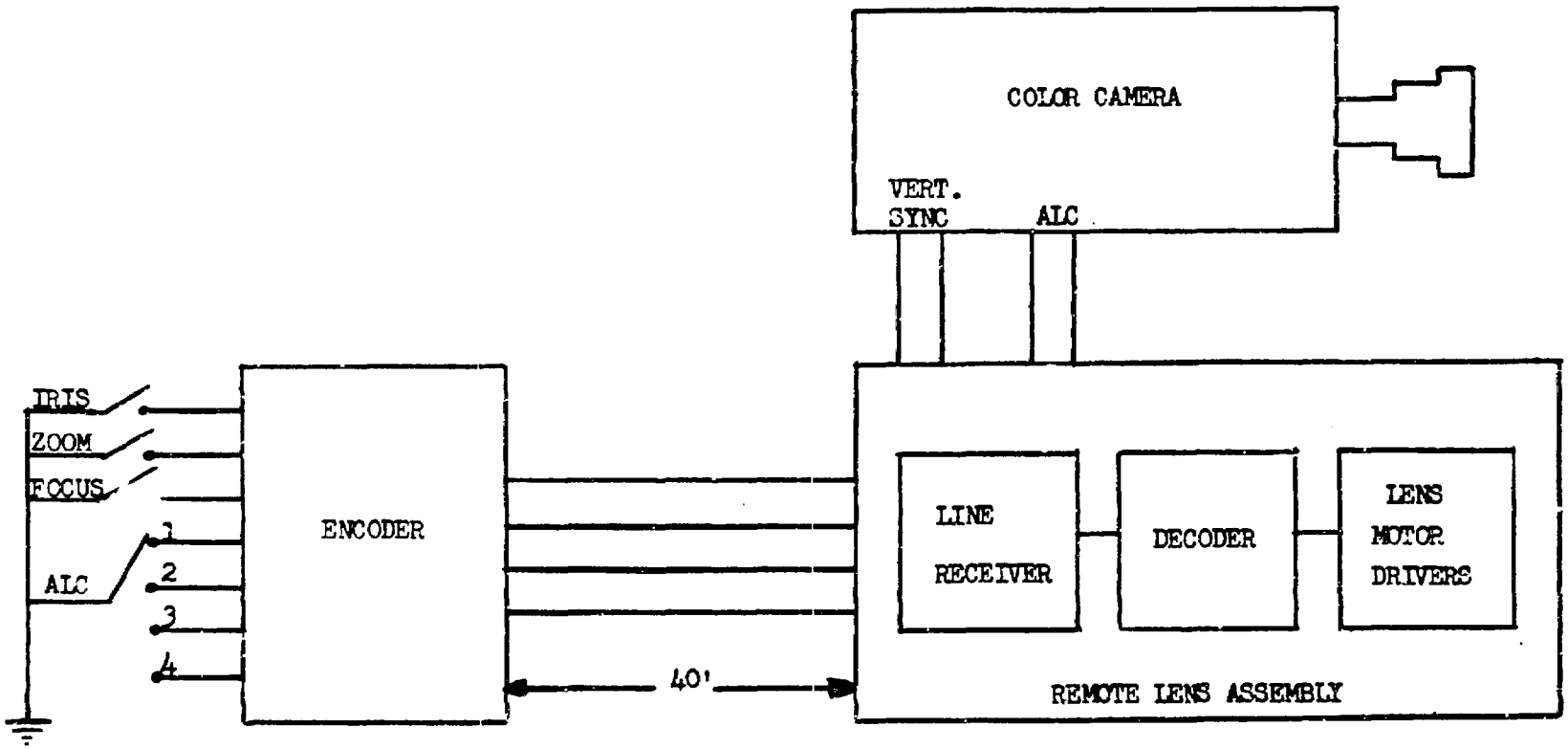

Figure 1. Skylab Remote Lens Block Diagram

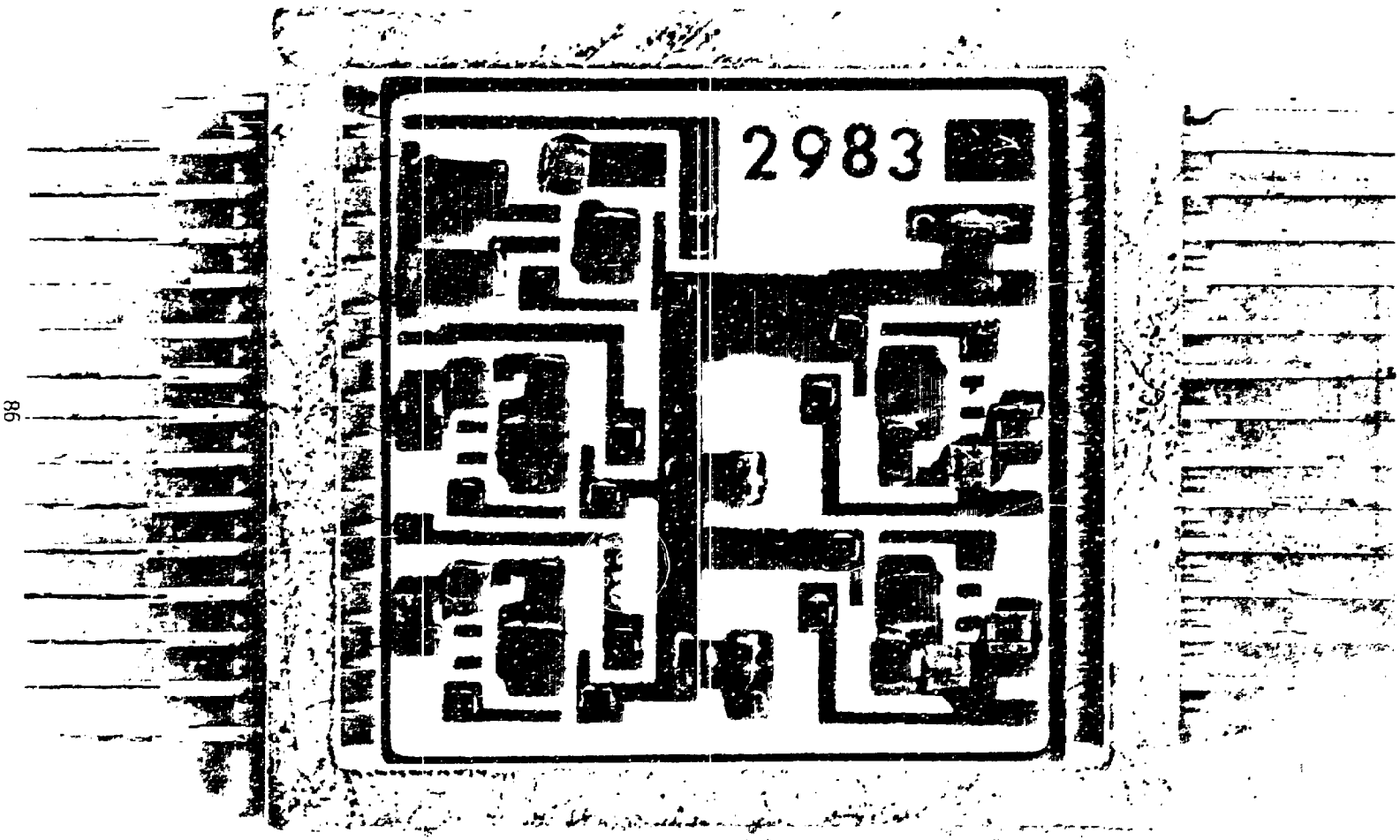

Figure 2. Receiver Multichip Hybrid Package

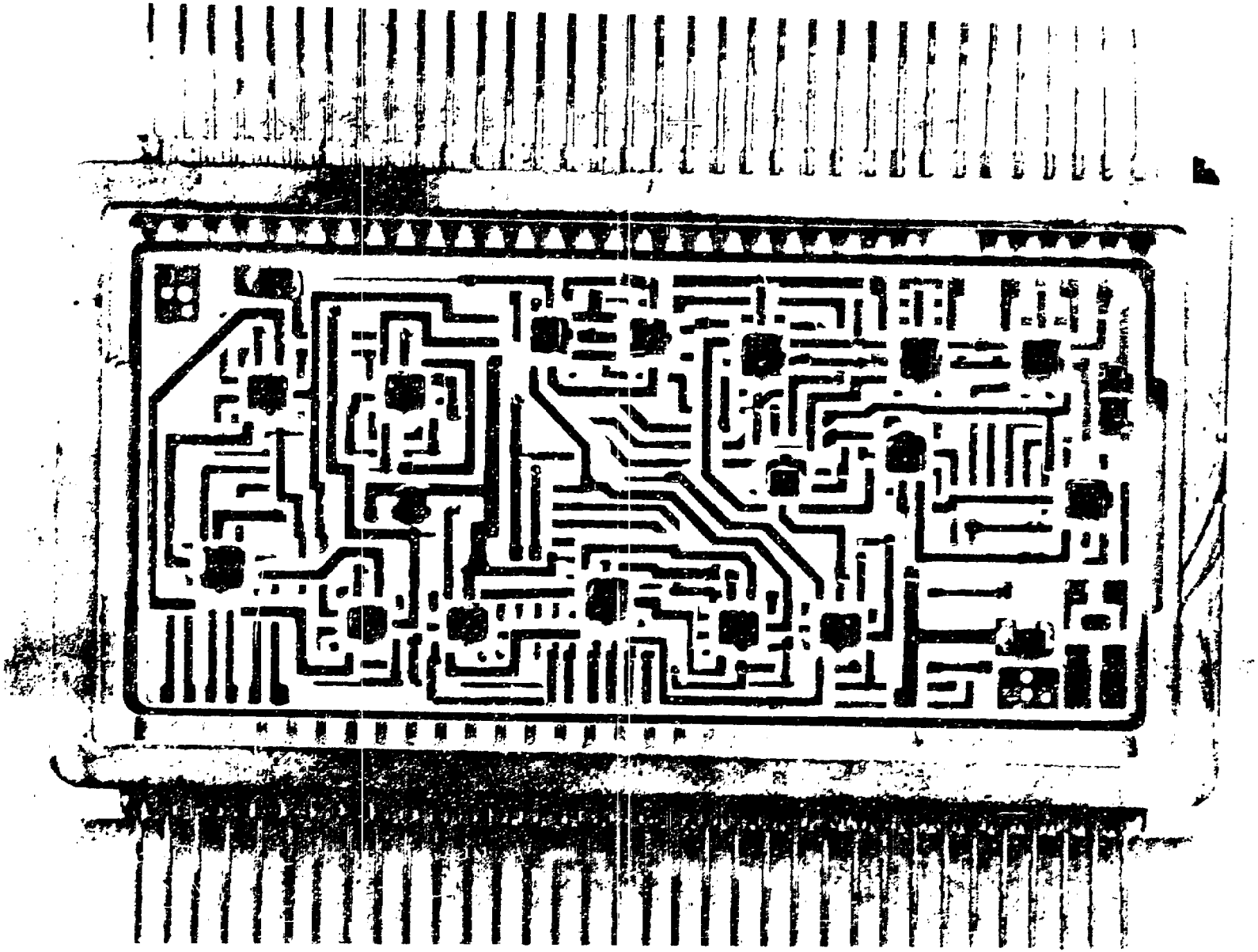

Figure 3. Decoder Multichip Hybrid Package

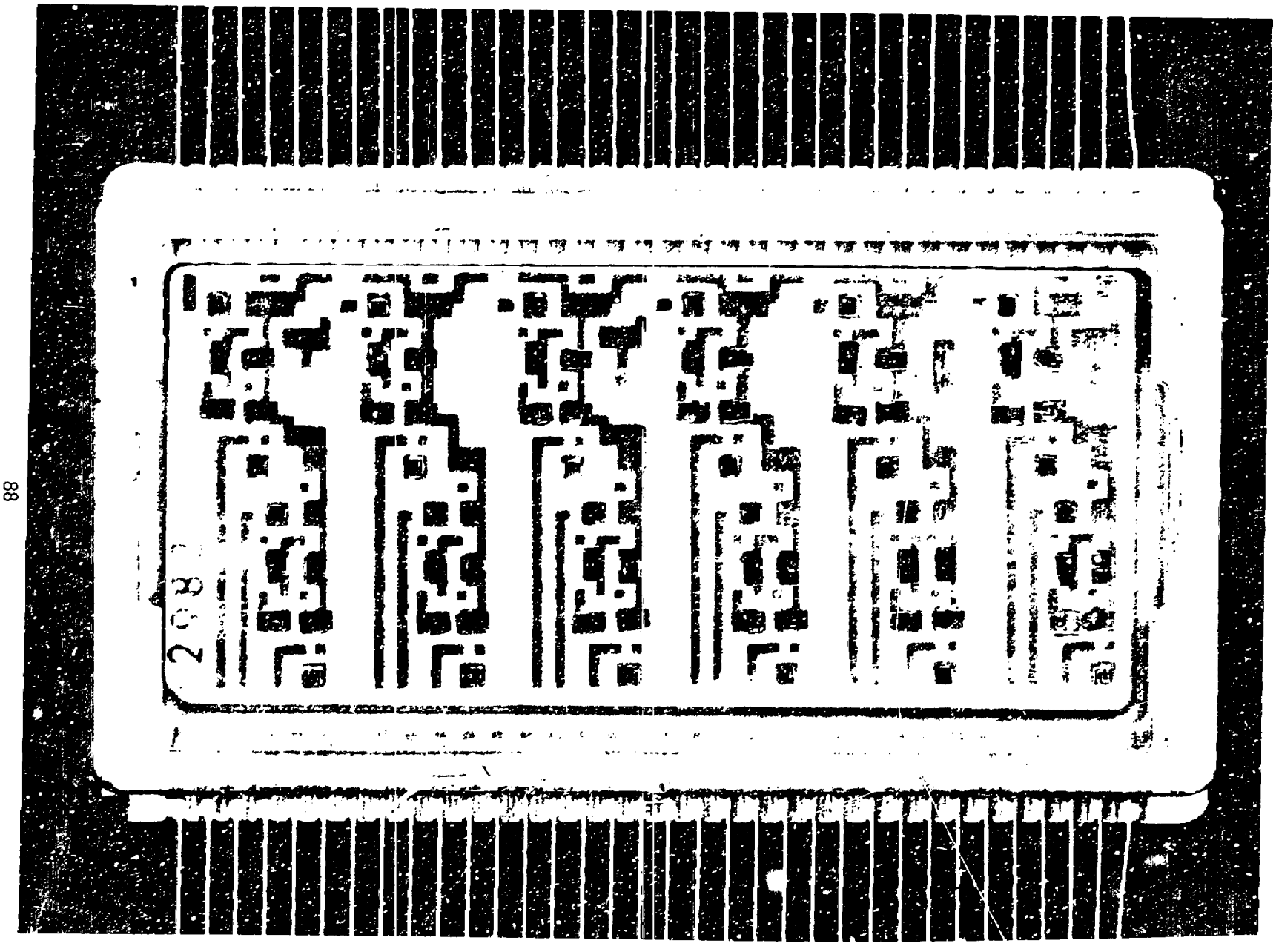

Figure 4. Motordriver Multichip Hybrid Packag

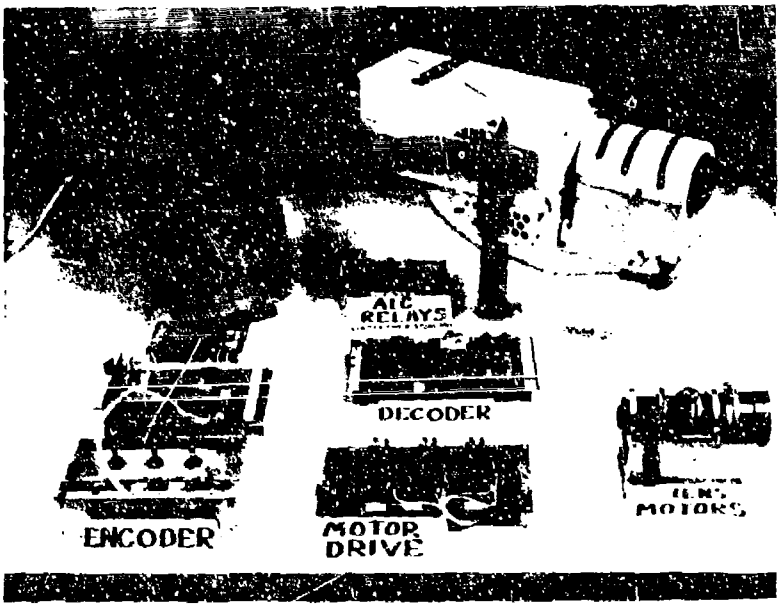

Figure 5. Skylab Remote Lens Breadboard

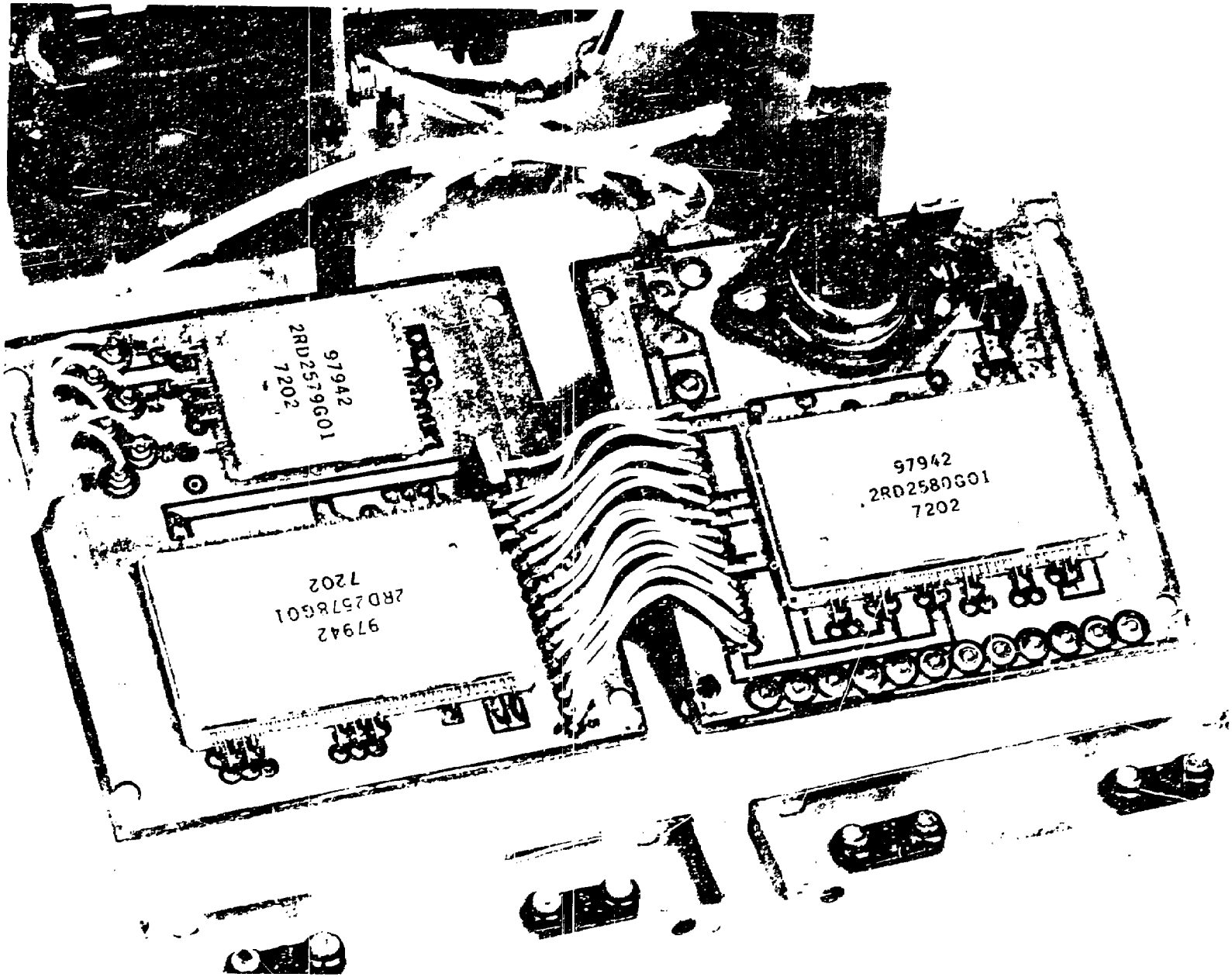

Figure 6. Remote Lens Multichip Hybrid Package Assembly

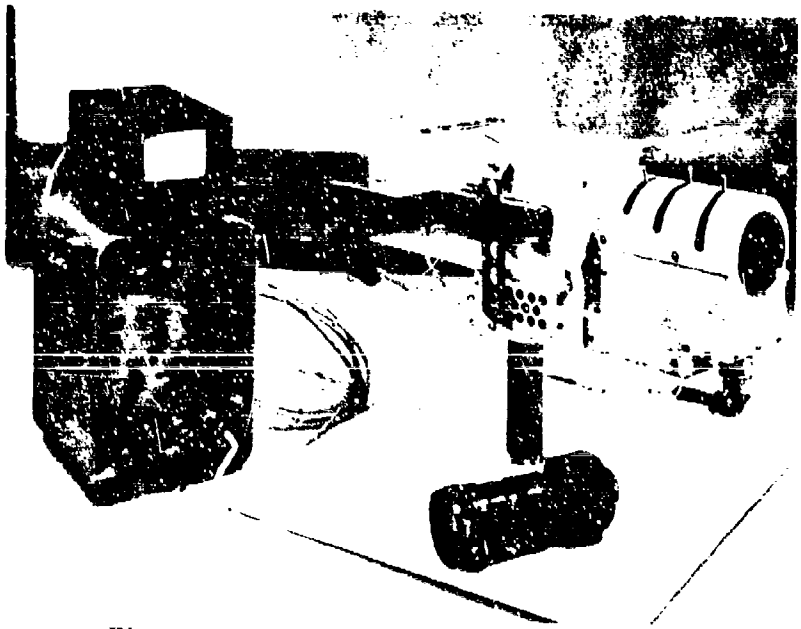

Figure 7. Skylab Remote TV Camera System

SELF-SCANNED PHOTODIODE SENSOR FOR POSTAL BAR CODE READING

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P. O. Box 22307
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ABSTRACT (UNCLASSIFIED)

Experimental results are presented for the application of LSI self-scanned photodiode arrays in low-cost electro-optical sensing for bar/half-bar recognition of bar code patterns for postal mail sorting.

1.0 INTRODUCTION

An extraction code imprinted on the front surface of a letter-size mail piece provides a means for lower cost machine sorting of mail than optical character recognition and context analysis of the address. For mail sorting applications, an inexpensive means of sensing and recognition of pre-printed bar codes is essential. Examples of cases where bar code patterns may be pre-printed are; return address envelopes of major mailers, and line printer generated address blocks that contain bar sorting codes. (See Figures 1 and 2.) Scanned photodiode sensors offer a means for low-cost electro-optical sensing since a single LSI chip may contain 64 to 256 photodiodes and on-chip scanning circuitry for serial sampling of the columnar photodiode sensing elements. (See Figure 3.)

2.0 FUNCTION

Mail imprinted with a bar pattern is transported past the Code Reader at 100 to 250 inches per second. The Code Reader is to electro-optically sense and recognize tall and short bars with an accuracy sufficient to yield an error rate less than 1 in 10^5. In general two bar code field regions contain bars of 0.110 $\pm$.010 and 0.050 $\pm$.010 inch height and of 32 bars-per-inch pitch. For the cited mail transport velocity and bar pitch, the recognition rate is 6,000 bars per second.

3.0 SPECIFICATIONS

Size: Read Optics Unit (ROU) 9 inches by 10 inches by 12 inches
Signal Processor Unit (SPU) 21 inches by 19 inches by 17 in.
Transport Speed: 100-250 inches per second
Bar Code Characteristics:

Bits per inch	32 $\pm$2
Tall bar height	0.110 $\pm$ 0.010 inch
Short bar height	0.050 $\pm$ 0.010 inch
Bar width	.010 to .019 inch
Void area	25 percent maximum of bar envelope
Minimum reflectivity of ink with respect to background	50 percent
Bit skew	$\pm$ 6 degrees maximum
Bit pattern skew	$\pm$ 2 degrees maximum
Viewing area of optics on mail piece	Field = .5 inch
Depth of Field at Mail piece	.25 inch

Maximum Read Error Rate:	1 per 100,000
MTBF: (Objective)	2,000 hours minimum
MTTR: (Objective)	30 minutes maximum

4.0 TECHNICAL APPROACH

Bar code reading systems completed under United States Postal Service contract (RER 70-72) use digital recognition logic and differ primarily in optical sensors. A discrete assembly of silicon phototransistors was employed in the first of the unit delivered to the USPS. (See Figure 4.) The second unit, completed in early 1972, uses a self-scanned photodiode array in the read head (Figure 5). The LSI chip comprises a row of N photodiode elements, a corresponding N stage shift register, with each stage connected to the gate of a MOS switch that couples the adjacent photodiode to a common recharge line. In response to a TTL clock input, a bit is loaded into the first shift register stage, and clocked through the register successively opening and closing the MOS switches, thereby connecting each photodiode in turn to the recharge line. As each photodiode is accessed, it is brought to the recharge line potential and then left open-circuited until sampled again. During the scan period the diode depletion layer capacitance is discharged by the instantaneous photocurrent integrated over the line scan time. When sampled again the integrated charge is replaced through the recharge line. Amplification of the signal (Figure 2) is via an integrating operational amplifier to yield a signal representative of envelope or bar reflectance. Amplifier output is sampled with an analog/digital converter of 4-bits to provide sixteen gray level resolution of envelope reflectance. An automatic gain control circuit (Figure 5) is employed to set the A/D converter white reference at a level corresponding to the envelope "white" in order to compensate for envelopes of varying color or reflectance. An area correlation unit is employed to provide dynamic thresholding of the gray-level-data to a binary quantized black/white decision. In the threshold unit local reflectance data is employed to set threshold level based on local samples immediately around a particular cell. For recognition, a 5 by 16 matrix (Figure 5), is employed on which digital feature combination logic operates to perform recognition of bar/half-bar classes.

5.0 EXPERIMENTAL RESULTS - SCANNED ARRAY BAR READER

Figure 6a illustrates a line printer generated bar coded address block, which it may be noted, is of substantially lower quality than a pre-printed code (Figure 1). This code field, sampled at 0.012 inch vertical intervals, 0.008 inch horizontal intervals, and thresholded; yields the video data shown by the lower trace of Figure 6b. Also shown (Figure 6b, upper trace), are the output signals from bar code

recognition unit, that show accurate recognition despite the poor quality of the bar code sample. Of primary concern, in determination of the usefulness of scanned array photodiode sensors, is obtaining an accurate rendition of envelope/data-field reflectance at high scan rates. Our results to date indicate that a dynamic range of at least 16.1 may be obtained at sampling rates of 2 Megahertz, by use of reset mode integrating operational amplifier circuit to cancel out clock transients present in the array output. Two factors limit the highest sampling rate: 1) array recharge RC time interval of 100-200 nanoseconds, and 2) amplifier reset and settling interval of 80-120 nanoseconds. In this application, the sampling of 40 cells in the time interval (32 microseconds) corresponding to envelope displacement of 0.008 inch at a 250 inch/second mail transport velocity yields a per cell interval of 800 nanoseconds, that is well within the rate limit factors. Primary rationale for employment of scanned array technology in lieu of discrete phototransistor arrays is cost savings by reduction from forty to one amplifier channels. This advantage is somewhat offset by the necessity for a more sophisticated and costly amplifier for the scanned array; however, additional and significant advantages accrue as follows: elimination if fiber-optic assemblies, reduced illumination level requirement, and compact overall optical path.

6.0 POSTAL APPLICATIONS

Experimental results described in paragraph 5.0 are for a 64-photodiode scanned array of which only 40 elements were employed for a 0.5 inch field of view with 0.1025 inch vertical sampling interval. Bar code reader described herein, with a limited 0.5 inch field of view is termed "Fixed Position Bar Code Reader", where the location of code field is known. For an extended coverage envelope width read band of several inches, more elements are required, for example, 256 cells with 0.010 inch vertical sampling interval for a 2.56 inch overall field of view. An extended capability unit "Variable Position Bar Code Reader" with a 2.56 inch envelope width field of view is currently under development by Recognition Equipment Incorporated for the United States Postal Service. This unit is to be capable of distinguishing between code fields and alphanumeric address information interference. For this application, a 256 photodiode array with a 10 Megahertz sampling rate is required. A custom LSI sensor chip with four video channels, each operating at 2.5 Megahertz, is to be employed to attain the net sampling rate of 10 Megahertz. It may also be noted, that consistent with device and amplifier scanning rate limitations, sufficient resolution may be obtained with 512 element arrays for optical character recognition of address blocks on un-coded mail.

Figure 1 Envelope with Pre-Printed Mail Sorting Bar Code Fields

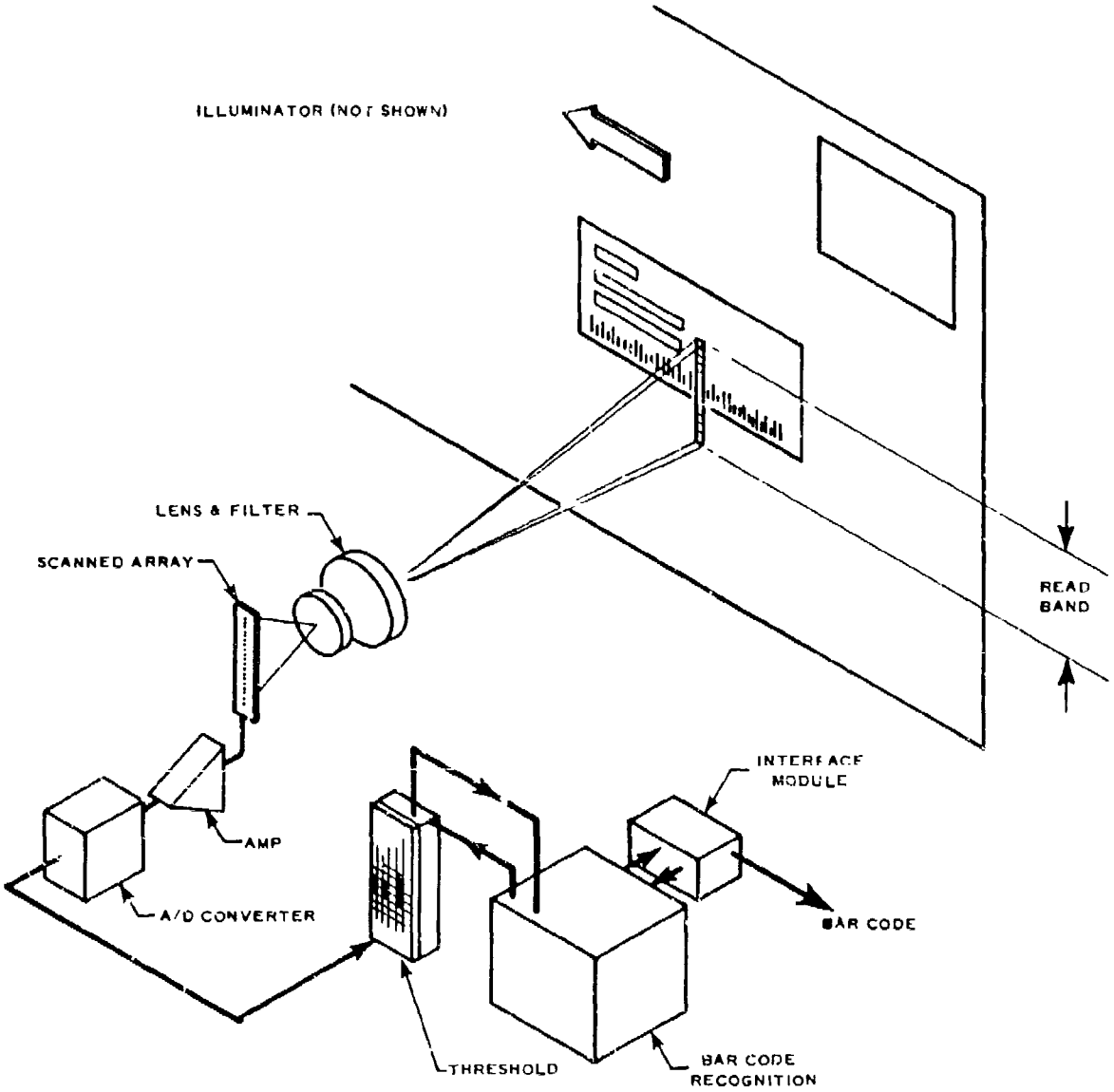


Figure 2 Application of LSI Self-Scanned Photodiode Array to Electro-Optical Sensing of Bar Coded Letter Mail

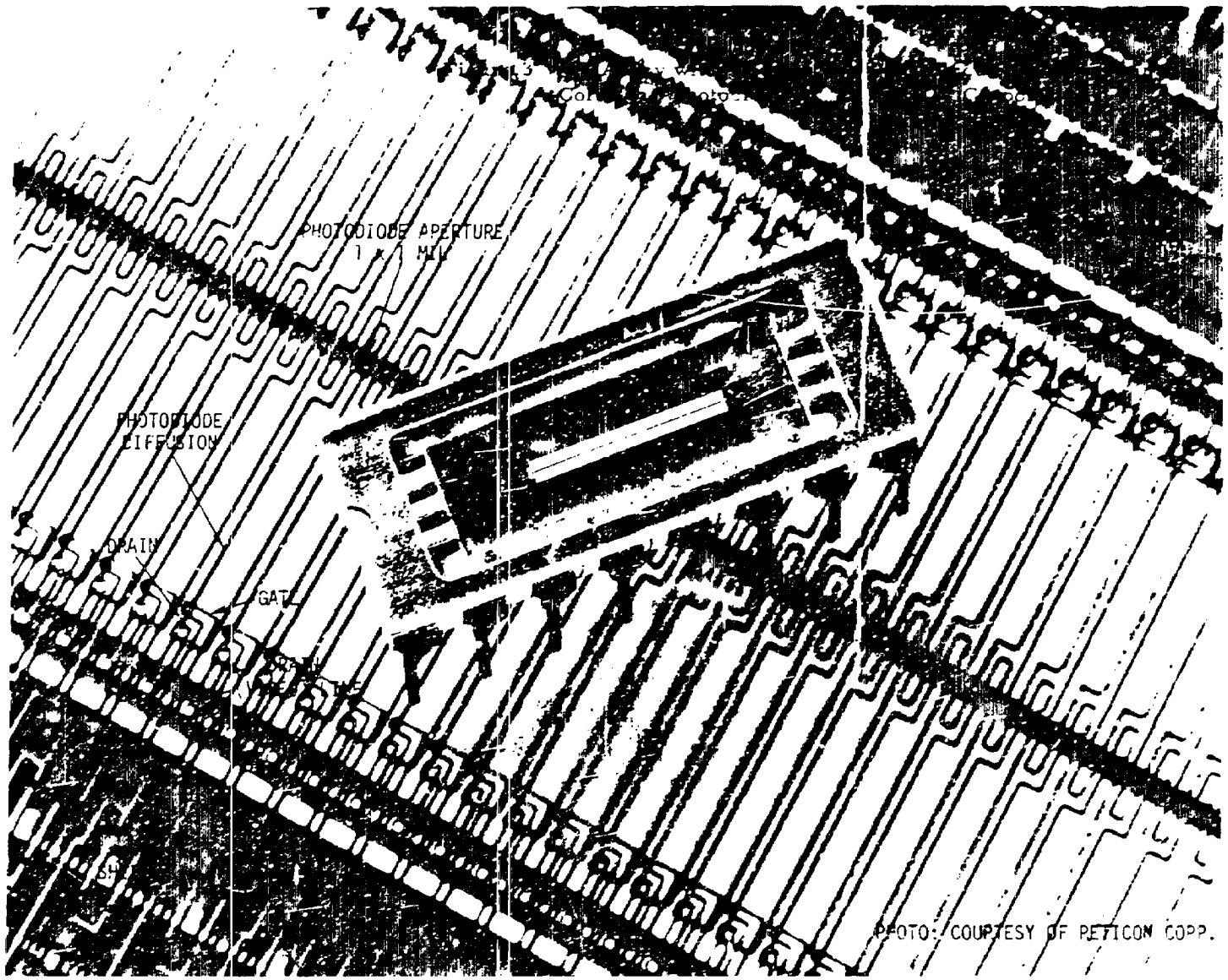


PHOTO: COURTESY OF PETICON CORP.

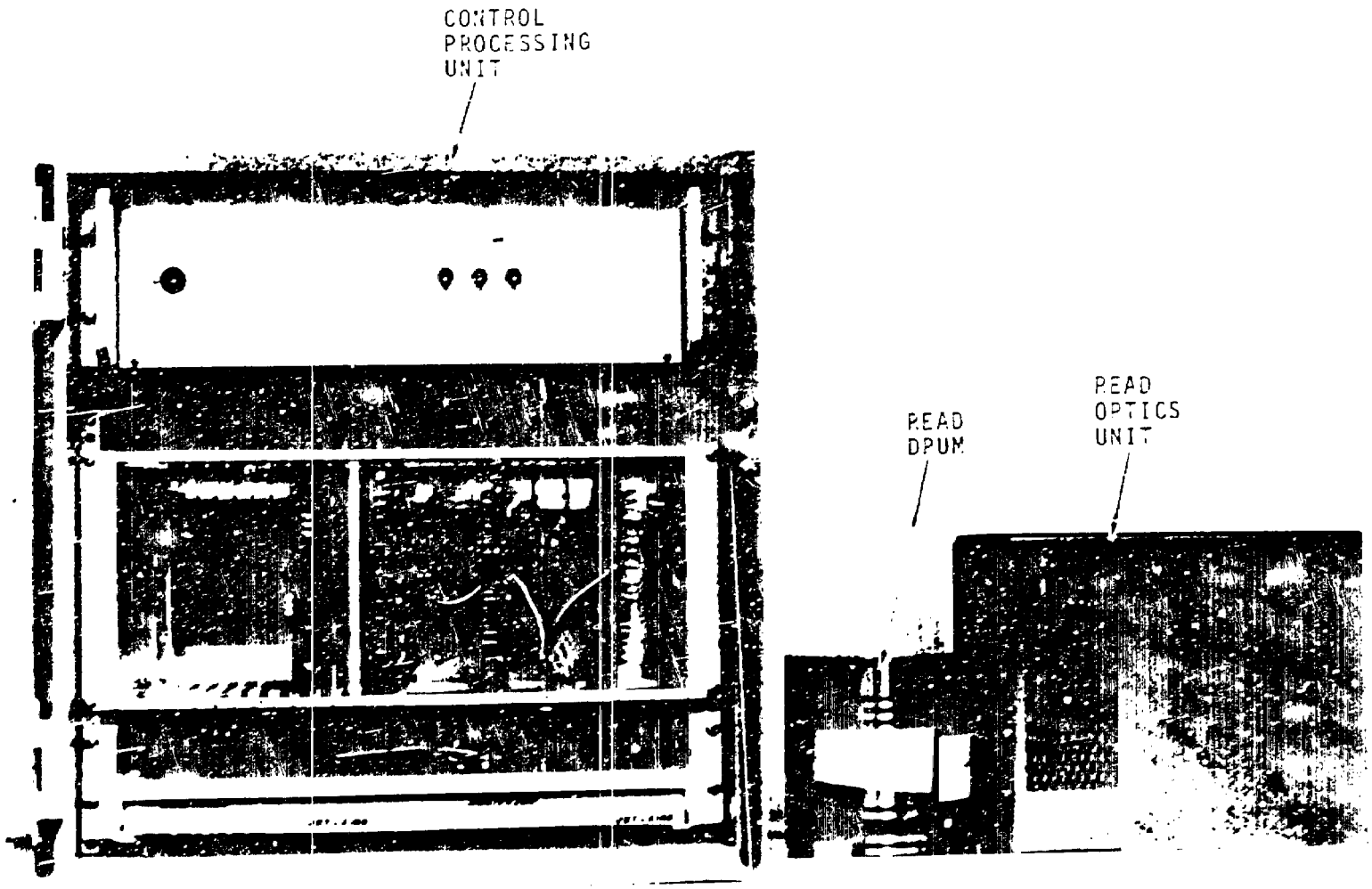


Figure 4 Bar Code Reader Comprising Read Optics Unit and Control Processor Unit

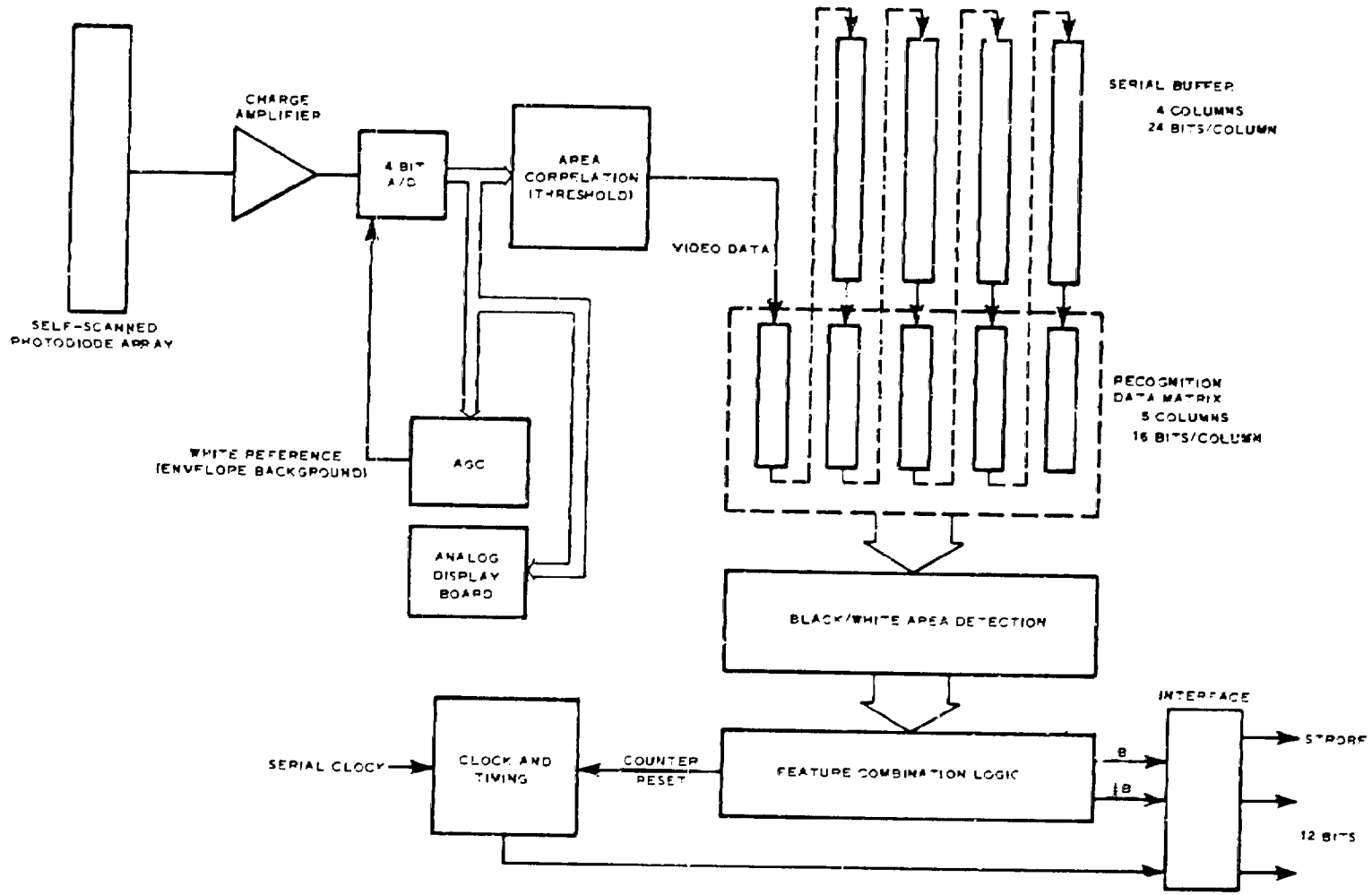
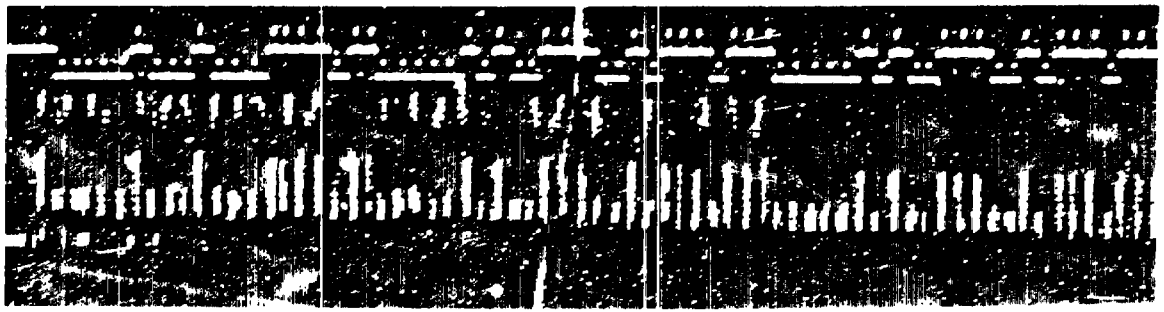


Figure 5 Bar Code Reader Block Diagram

BASF COMPANY
BEDORD MA 01730

(a) LINE PRINTER GENERATED ADDRESS SAMPLE



(b) CORRELATED & DIGITALLY FILTERED VIDEO DATA, AND OUTPUT SIGNALS FROM BAR, HALF-BAR RECOGNITION ELECTRONICS

Figure : Recognized Bar Pattern From Fixed Position Bar Code Reader

EFFECTS OF HIGH ENERGY PULSES ON HYBRID CIRCUIT MATERIALS

J. F. Burgess, C. A. Neugebauer, R. A. Sigsbee

Abstract

The thermal and mechanical behavior of Au, Cu, Al and Ni-Cr films and Al-30% Ge solder on BeO and Al_2O_3 substrates when exposed to a short high intensity energy pulse is examined. A range of energies is considered.

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EFFECTS OF HIGH ENERGY PULSES ON HYBRID CIRCUIT MATERIALS

J F. Burgess, C. A. Neugebauer, R. A. Sigsbee

In high energy pulse environments, hybrid circuits containing Au conductors are unsatisfactory because of absorption-induced failures. In this case, the Au conductors fail due to heating caused by the high absorption. To avoid this problem, hybrid systems which utilize Al conductors and Al-Ge chip-bonding solders have been proposed. This study analyses the high energy pulse behavior of materials likely to be considered for hybrid circuit conductors, resistors and substrates.

In this study, the primary conductor materials considered are Au, Al, Cu and NiCr in combination with Al_2O_3, BeO and SiO_2 substrates. The temperature rises due to absorbed energy were calculated using the appropriate absorptions, heat capacities, and thermal conductivities. Results were interpreted in terms of the attendant failure mechanism, such as melting, vaporization, thermal expansion induced stresses, and irreversible structural changes. The maximum transient temperature achieved by the films or bonded chips on a ceramic substrate included heat losses to the substrate. Principal attention was devoted to the region where the differences in absorption are large. The maximum transient temperatures are plotted in Fig. 1 for various film materials of several thicknesses on BeO, Al_2O_3 or SiO_2 substrates as a function of the incident fluence level in cal/cm^2, assuming an initial temperature of 25°C. The induced thermal stresses in the film which can lead to failure directly or through the excitation of acoustic vibrational modes in the hybrid structure were then calculated for films thin relative to the substrate and are plotted in Fig. 2.

The principal conclusions for various energy ranges in order of decreasing energy are:

Range A

Here the absorption coefficients of all materials are the same within a factor of 2 or 3. Failure may then occur when the temperature rises to the melting point of the lowest melting material present, such as the chip attachment solder.

Range B

Here the difference in absorption between various materials is very great and low absorption are superior. The principal conclusions in this energy region are:

1. Al, Be, Si, Al_2O_3, BeO and SiO_2 all experience similar temperature increases. Also the temperature rise in Al films will not depend on the film thickness.

2. The transient temperature rise for Cu films on Al_2O_3 or BeO substrates is less than 1/50 that of Au films.

3. The transient temperature rise for a Cu film depends strongly on its thickness and the thermal conductivity of the substrate, in addition to the pulse duration. The thinnest Cu film on the highest conductivity substrate is optimum. Nevertheless, even 1000A of Cu on BeO experiences twice the temperature rise of Al films.

4. If a solder containing appreciable quantities of medium absorption elements is used, a fluence level of 160 cal/cm^2 may not be exceeded for practical solder thicknesses or melting will occur.

5. If an Al conductor system, or a thin (<5000A) Cu system is to be used to its full advantage, only Al or lower absorption materials may be used in the die attachment. However, there are no thickness limitations on these materials. Similarly, NiCr resistors on the chip must be replaced with lower absorption materials, or have a better heat sink than SiO_2.

6. Stress induced failures may be caused by shear stresses generated during heating making the interfacial bond strength critical. Film thicknesses and temperature increases should always be minimized to reduce interfacial shear stresses, even if yielding occurs.

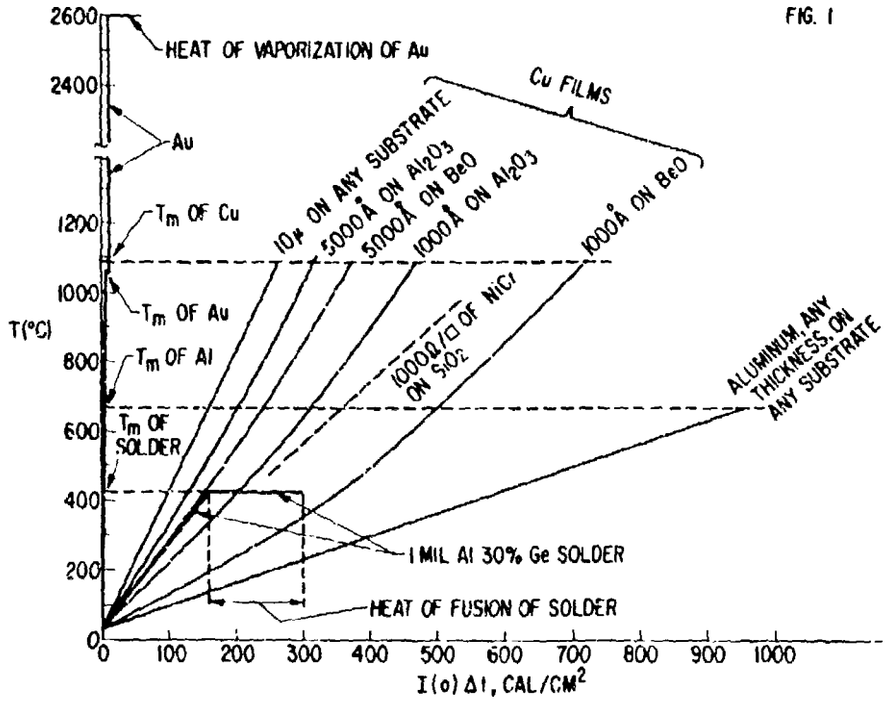
Range C

Here the energy absorption of Al and Si is $\sim$1/30 that of Au, compared to Cu and Ni-Cr which absorb $\sim$1/5 that of Au. The transient temperature rises, relative to Al, for medium absorption materials are greater than for Range A but may be acceptable for medium energy density environments.

Range D

The absorption by Al and Si is $\sim$1/10 that of Au and Cu is $\sim$1/4 that of Au. The absorption by Be and BeO is significantly lower than for Al or Al_2O_3. BeO substrates are therefore better heat sinks in this energy range. This may be particularly important when the pulse is repetitive.

FIG. 1



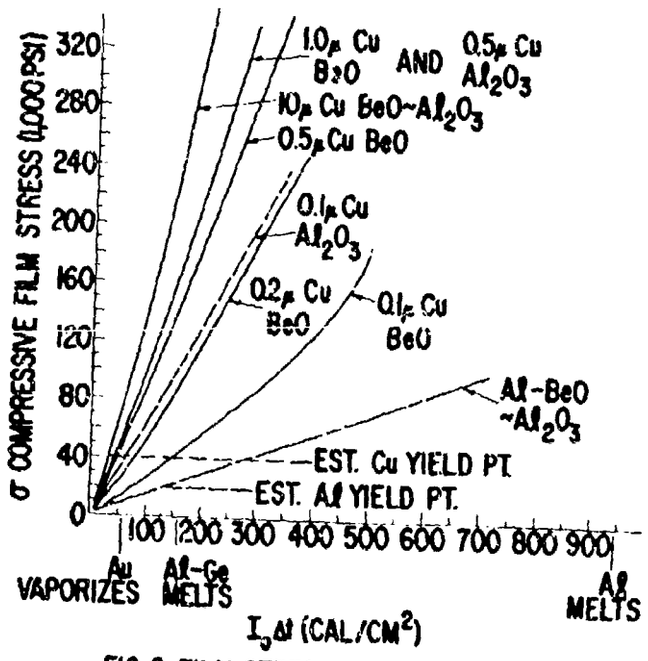


FIG. 2 FILM STRESS vs INTEGRATED FLUX

NEUTRON RADIATION HARDENED GaAs JUNCTION FIELD-EFFECT TRANSISTORS OPERATING IN THE HOT ELECTRON RANGE*

R. Zuleeg

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5301 Bolsa Ave., Huntington Beach, California 92647

ABSTRACT

Fast neutron induced degradation characteristics of short channel GaAs junction field-effect transistors operating in the hot electron range are presented. The neutron degradation improvement factor is theoretically predicted and is experimentally verified to correlate with the predictions. Degradation of GaAs J-FET transconductances up to a neutron fluence of 1.2×10^{16} n/cm^2 (E>10 keV) are reported.

1) INTRODUCTION

Short channel GaAs junction field-effect transistors operate in the hot electron range. An extended unipolar transistor theory by Lehovec and Zuleeg[1] describes the voltage-current characteristics in explicit mathematical relations and includes the effects of scattering limited velocity saturation. An application of these theoretical results, together with known carrier removal rates and degradation of N-type GaAs material, predicts improved neutron degradation characteristics of GaAs J-FET's. The theoretical analysis and preliminary data for the effects of fast neutron irradiation on the electrical parameters of N-channel, GaAs J-FET's operating under hot electron conditions was published by McNichols and Zuleeg[2]. This paper presents extensive measurements of degradation characteristics of GaAs J-FET's which were exposed to a fast

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* This work was sponsored in part by the Air Force Cambridge Research Laboratory and the McDonnell Douglas Astronautics Company Independent Research and Development Program.

neutron fluence up to 1.2×10^{16} n/cm^2 (E>10 keV).

2) EXPERIMENT

The GaAs J-FET's, Fig. 1, used in this study were fabricated on N-type layers 1-2 μm thick with carrier concentrations in the range of 10^{15} cm^{-3} to 10^{17} cm^{-3} epitaxially grown on chromium doped, semi-insulating substrates. The gate, with a length of 5 μm, is zinc diffused across a mesa formed by etching through the epitaxial layer. Source, drain and gate contacts are alloyed AuGe. The maximum frequency of oscillations for the devices is about 6 GHz.

The data for the normalized transconductance degradation of the J-FET's as a function of channel doping for a neutron fluence of 2×10^{15} n/cm^2 are presented in Fig. 2 for all transistor lots tested under the study program. Each lot was composed of a minimum of ten devices. It is evident that the average value, and the standard deviation range, of normalized transconductance degradation of device lots doped with 2×10^{15}, 2×10^{16}, 5×10^{16} and 1×10^{17} cm^{-3} are predicted by the theory for z >> 1, where by definition[1]

$$z = \frac{\mu V_o}{v_m L} \tag{1}$$

and where μ is the low field drift mobility, V_o is the device pinch-off voltage, v_m is the carrier drift saturation velocity and L is the gate length of the device. From theory[2] one obtains for $V_o >> V_b$, where V_b is the junction built-in voltage, the relations

$$g_m/g_{mo} = (\mu N/\mu_o N_o) \text{ for } z = 0 \tag{2}$$

$$g_m/g_{mo} = (\mu N/\mu_o N_o)^{1/3} \text{ for } z >> 1 \tag{3}$$

When z >> 1 the devices operate in the hot electron range. For devices operating in the Shockley mode, i.e. z = 0, the degradation would be more severe and comply with theoretical predictions given as the dashed line. The agreement of the results with the theory for z >> 1 establishes the improvement factor which is inherent to GaAs field-effect transistors operating in the hot electron range. According to Eq. 3 the low field mobility degradation and the carrier concentration

reduction enter in the hot electron range case with a power of 1/3, whereas in the Shockley case the degradation of g_m is proportional to the product of μN (Eq. 2).

The small degradation of g_m and almost unnoticeable change of drain saturation current, I_{DS}, of two GaAs J-FET's with a channel doping of 1×10^{17} cm^{-3}, exposed to a neutron fluence of 1×10^{15} n/cm^2 (E>10 keV), is demonstrated in Fig. 3. Drain saturation current in the hot electron range is determined by a velocity limited current component, I_o, through the relation[1]

$$I_{DS} = I_o \ (1 - u_m) \qquad (4)$$

where $I_o = qNv_m aW$ and u_m^2 is a normalized drain voltage and related to Z. Since u_m and v_m are assumed constant, the degradation of I_{DS} is only related to the change in N, which is less than 5% for this fluence. For the Shockley case I_{DS} is proportional to μN^2 and larger changes would be expected due to degradation of μ. Fig. 4 presents the predicted degradation of normalized transconductance vs. neutron fluence for three different channel doping concentrations of GaAs J-FET's operating in the hot electron range according to Eq. 3. Experimental points are shown which present the average value of 18 GaAs J-FET's fabricated on material with a channel doping of approximately 1×10^{17} cm^{-3} and exposed to successively higher fluence levels. The uncircled data point at $\Phi = 8 \times 10^{15}$ n/cm^2 was obtained by annealing the devices at 250° C for 10 minutes. As received, the devices experienced an abrupt degradation to values of 0.5 to 0.6 in contrast to the theoretical predictions. Since the annealing is of the stage I characteristic, as observed by Aukerman et al,[3] the speculation is that this component of the damage may be due to the appreciable gamma flux present during neutron irradiation at the higher fluences. Isochronal annealing studies on devices exposed to a fluence of 1.2×10^{16} n/cm^2 are in progress to clarify the degradation mechanism.

3) CONCLUSION

Operation of GaAs J-FET's in the hot electron range yields a neutron degradation improvement factor, which was experimentally verified.

Devices with a channel donor concentration of 1×10^{17} cm^{-3} or greater are capable of operating at a fluence level of 1×10^{16} n/cm^2 in a variety of circuit applications with tolerable degradation and with negligible degradation of electrical parameters at a fluence of 1×10^{15} n/cm^2.

4) ACKNOWLEDGEMENTS

The author credits A. F. Behle, D. T. Dion and S. H. Watanabe for the fabrication and evaluation of the devices and thanks S. A. Roosild of AFCRL for providing the neutron irradiations.

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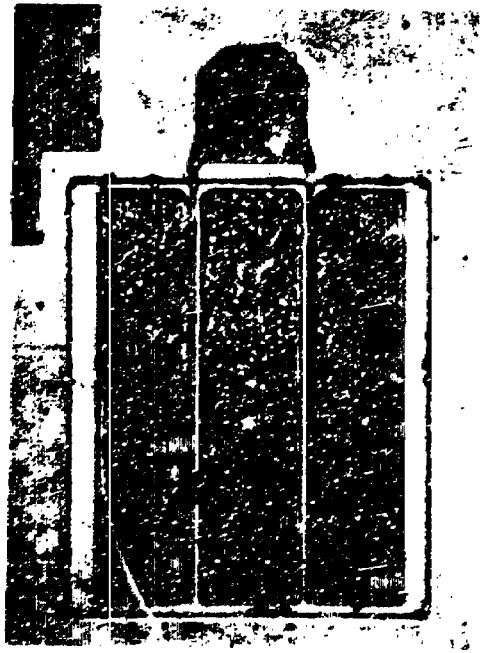
1. K. Lehovec and R. Zuleeg, "Voltage-Current Characteristics of GaAs J-FET's in the Hot Electron Range," Solid State Electronics, 13, Oct. 1970, pp. 1415-1426.

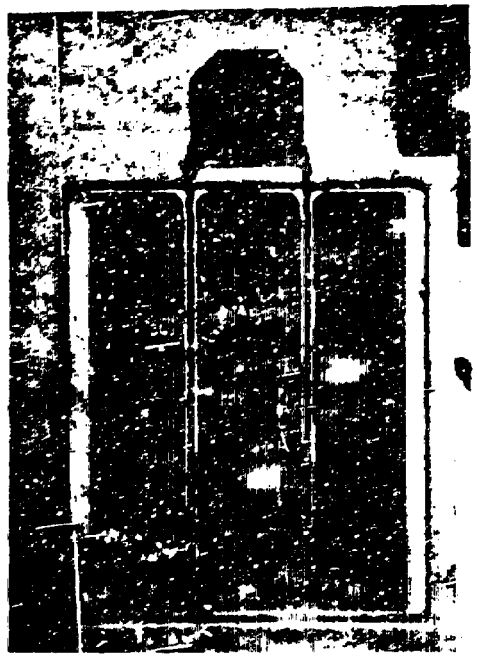
2. J. L. McNichols and R. Zuleeg, "Improved Fast Neutron Tolerance of GaAs J-FET's Operating in the Hot Electron Range," IEEE Trans. Nuclear Science, NS-18, April 1971, pp. 110-113.

3. L. W. Aukerman, P. W. Davis, R. D. Graft and T. S. Schilliday, "Radiation Effects in GaAs," Journal of Applied Physics, 34, Dec. 1963, pp. 3590-3599.

Ga As JUNCTION FET GEOMETRY



W = 700 μm (= 28 mil)
L = 5 μm
L_S = 2.5 μm
L_D = 5 μm

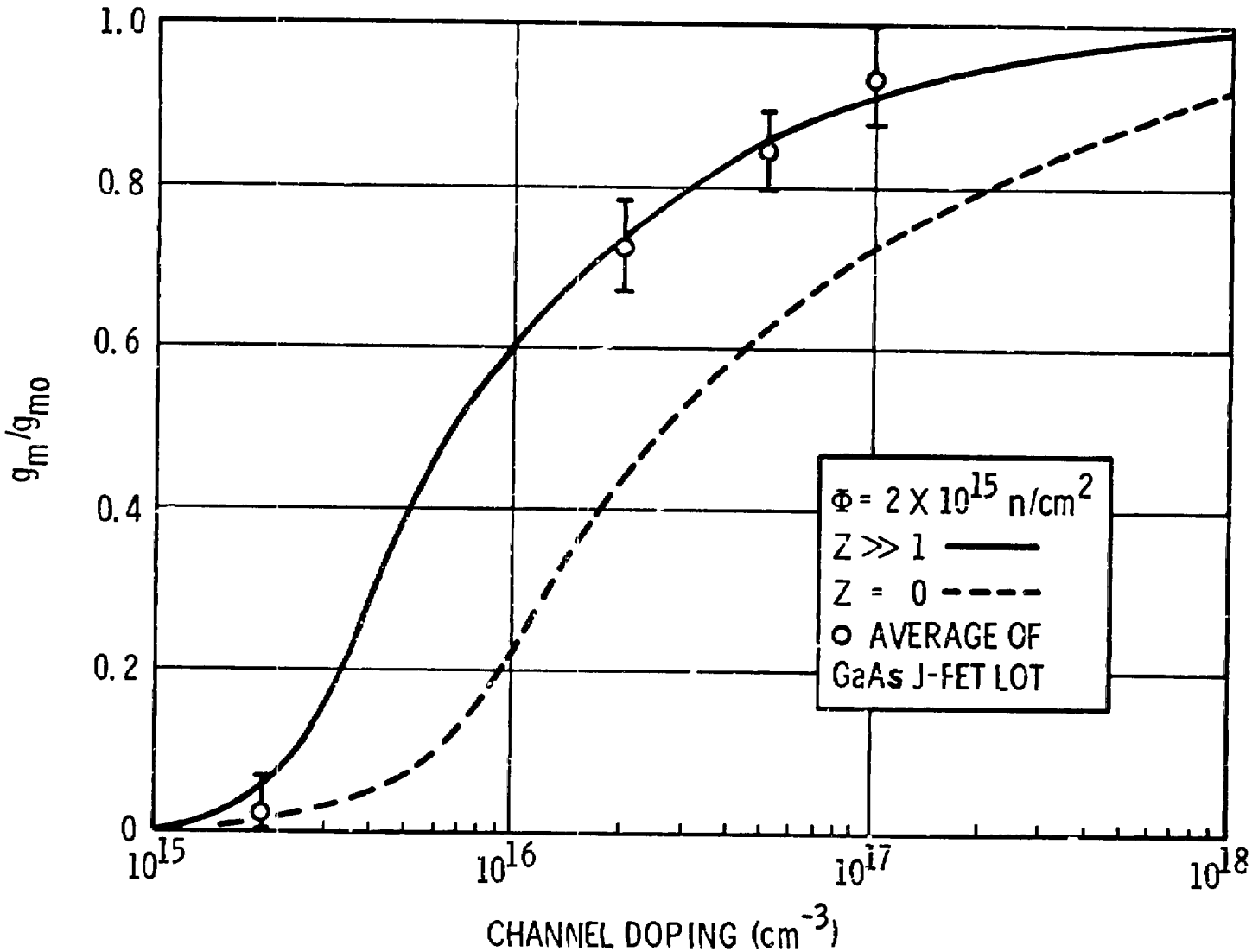


W = 700 μm
L = 5 μm
L_S = 5 μm
L_D = 5 μm

SCALE:
100 μm

Figure 1 Photograph of GaAs Junction FET Geometry on Wafer. Channel Width, 700 um; Channel Length 5 um; Separation Gate to Source 2.5 um.

Figure 2 Normalized Transconductance Degradation vs. Channel Doping for a Fluence of 2×10^{15} Neutrons/cm^2 (E>10 keV) for the case z = 0 and z >> 1. Experimental Results of GaAs J-FET's with Various Channel Doping Concentrations are Indicated by Circles.

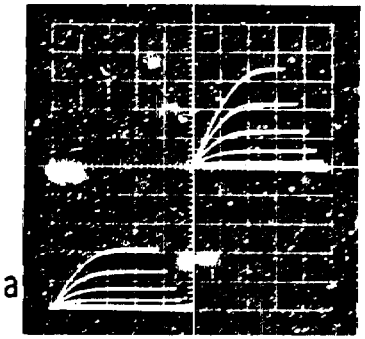


GaAs J-FET VOLTAGE-CURRENT CHARACTERISTICS

TWO DEVICES FROM LOT IN-90-B
WITH A CHANNEL DOPING OF 1×10^{17} cm^{-3}

Figure 3 Voltage-current Characteristics of Two GaAs Junction Field-effect Transistors with a Channel Doping of 1×10^{17} cm^{-3} before and after Exposure to a Neutron Fluence of 1×10^{15} n/cm^2 (E>10 keV).

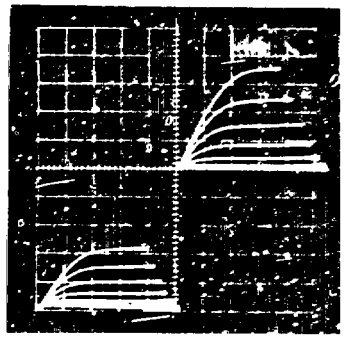
DEVICE 9a



9b

BEFORE EXPOSURE TO NEUTRONS (E > 10keV)

DEVICE 9a



9b

AFTER EXPOSURE TO 1×10^{15} NEUTRONS / CM^2

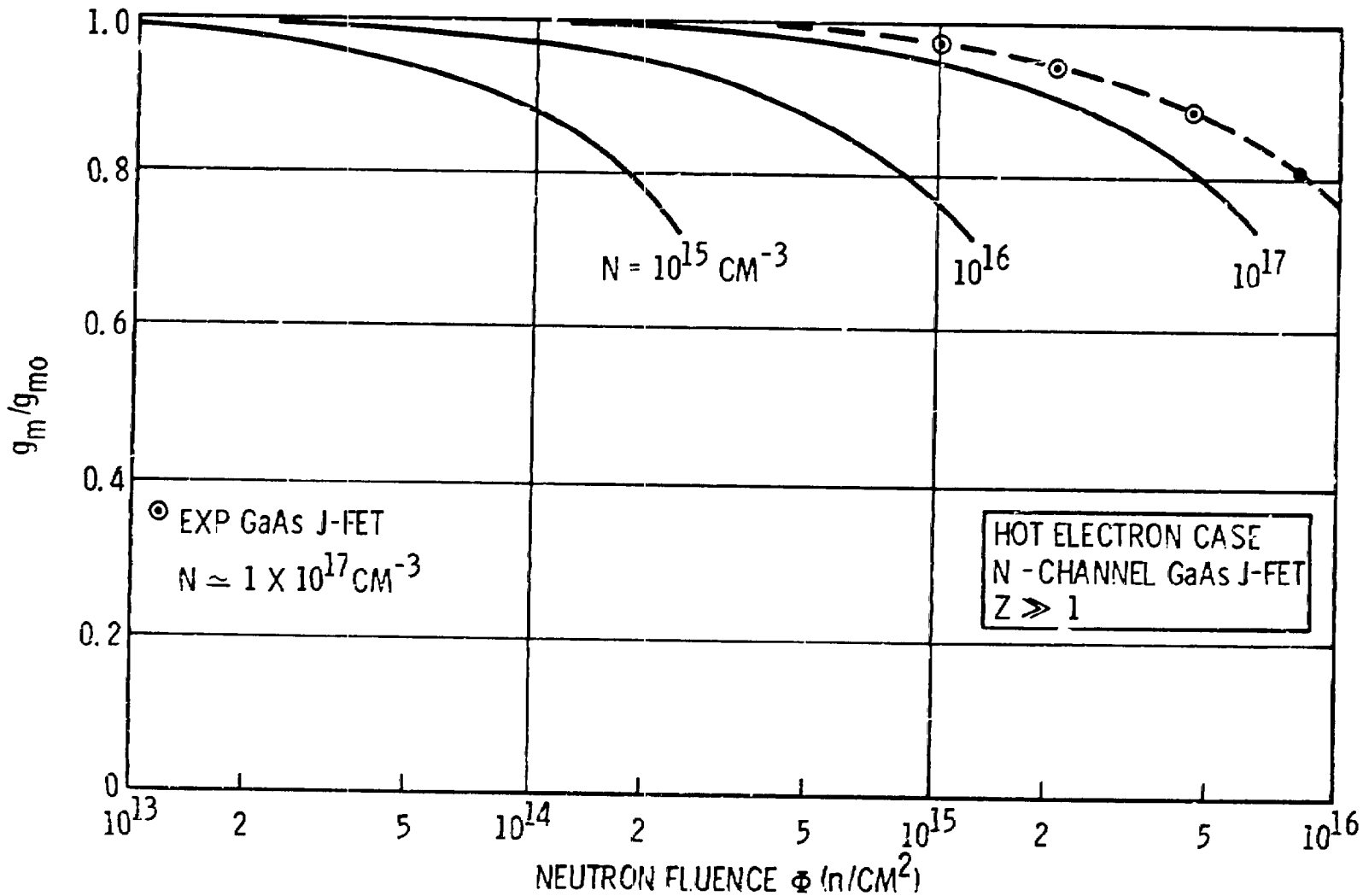
IDENTICAL SCALES:

VERT I_D IN 10 mA/DIV

HORIZ V_D IN 1 VOLT/DIV

NEG V_G IN 0.5 VOLTS / STEP

Figure 4 Normalized Transconductance vs. Neutron Fluence (E>10 keV) of GaAs J-FET's operating in the Hot Electron Range for Three Different Channel Doping Concentrations. Experimental Results of GaAs J-FET's with a Channel Doping of approximately 1^{17} cm^{-3} are shown.



Abstract

POWER TRANSISTORS RESPONSE TO
HIGH PROMPT GAMMA DOSE RATE LEVELS

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(201) 256-4000

Experimental data is presented on the transient response of power transistors to prompt dose rate levels of between 10^8 - 10^{12} rads(Si)/sec. For the higher dose rate levels where catastrophic failure was encountered, design circumvention techniques are presented.

POWER TRANSISTORS RESPONSE TO HIGH PROMPT GAMMA DOSE RATE LEVELS

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In most electronic systems exposed to a nuclear radiation burst, the most susceptible part of the system to both transients and permanent damage is the power supply section. This problem becomes even more acute at high dose rate levels where primary photocurrents of as much as hundreds of amperes have been measured. In order to effectively solve the problem of power supply survivability, a thorough understanding of the response of power transistor to prompt gamma dose rates levels is required. It is the purpose of this paper to present the results of an effort designed to yield sufficient experimental data on power transistors in a nuclear environment. These results attempt to both advance the understanding of the behavior of power components at high levels and present the power supply design engineer with helpful transient components data.

EXPERIMENTAL PROCEDURE

Three standard transistor types and one hardened (Solitron) transistor type were exposed to a prompt gamma dose rate environment ranging from 10^8 to 10^{12} rads (Si)/sec. Five units of each type were irradiated. These were:

(1) BR100B Solitron Devices Hardened Transistors (5 Amp)
(2) W1714-1405 - Westinghouse Power Transistor (5 Amp)
(3) 2N5805 - RCA Power Transistor (10 Amp)
(4) 2N2219 - Motorola Transistor (0.8 Amp)

The Solitron devices were chosen due to their wide availability in a variety of case styles, and have a number of similar types available, thus making them applicable in a number of hardened power supply applications. The other devices were chosen due to their general usefulness in systems which do not have a severe neutron environment.

The units were irradiated in three different facilities:

(1) Gulf Radiation Technology LINAC (10^8 - 10^{10} rads (Si)/sec).

(2) Physics International's 1140 Pulserad (10^8 - 10^{11} rads/sec).
(3) Air Force Weapons Lab's PI-1590 Pulserad (10^{11} - 10^{12} rads/sec).
Transient primary photocurrents were measured by utilizing the test circuits shown in Figure 1a and b.

Test circuit 1a was utilized at lower level LINAC testing where electrical noise problems were not severe. At high dose rate levels (Flash X-Rays) a novel technique was used to record I_{pp} through a charge storage phenomena.

The data obtained is presented in graphical form. The plot which appears in Figure 5 shows I_{pp} vs gamma dot level for each transistor.

A representative set of raw data is now presented. Figure 2 shows the primary photocurrent of the 2N5805 power transistor as obtained from the circuit of Figure 1a. The primary photocurrent for this device is 900 ma and could cause significant damage in a circuit if not compensated properly. Figure 3 shows a primary photocurrent of 200 ma for the W1714-1405 power transistor, Figure 4 illustrates the response of the BR100B using the circuit of Figure 1b. A current of approximately 120 amps was obtained. This current caused catastrophic failure in the device through burnout.

DISCUSSION OF RESULTS

The results obtained in this effort clearly indicate that most power transistors including hardened devices cannot withstand a transient gamma burst exceeding about 5×10^{10} rads/sec without a serious possibility for catastrophic failure. The graph illustrates a qualitative relationship that can be used as a good rule of thumb to determine primary photocurrents. The higher the f_T of the transistor the lower the photocurrent at any given radiation level. This is due to the fact that the f_T is dependent on the collector-base capacitance, which is directly related to the collector base area. This area, in turn, weighs heavily in the photocurrent generation. Since conventional junction compensation techniques would be completely ineffective at levels exceeding 10^{10} rads/sec, the power supply designer is forced to seek design circumvention techniques. The method of junction photocurrent compensation becomes ineffective at high dose rates (above 10^{10} rads/sec) due to two factors: (1) A mismatch between the primary junction photocurrent and the compensating junction photocurrent develops thus rendering compensation totally ineffective, (2) At severe dose rates and large junction areas burnout becomes very probable. Hence, other techniques must be sought which when combined with prudent design solves the problem at these higher levels.

Collector circuitry should include a resistor, so that the collector-base photocurrent is limited. The value of this resistor should be the maximum resistance that does not affect normal circuit operation. In power supply circuits such as pulse width modulators, the high amount of inductance already in the circuit might be enough to prevent any damage. The maximum current change can be calculated from a knowledge of the circuit and the width of the radiation pulse (maximum change in the inductor, not the transistor junction). If the current is too large, it can be reduced by increasing the inductance of the inductors. If necessary additional

inductors can be placed in the collector circuitry.

Care should also be taken when using capacitors, since they can supply large amounts of current over short periods of time. The circuit should be checked for large equivalent capacitances appearing across the collector base. An example of this appears in Figure 6. Again, a base resistor can be inserted.

CONCLUSION

Using the above techniques and data, the power supply engineer has some useful tools to use when designing power supplies to the higher levels of prompt gamma radiation.

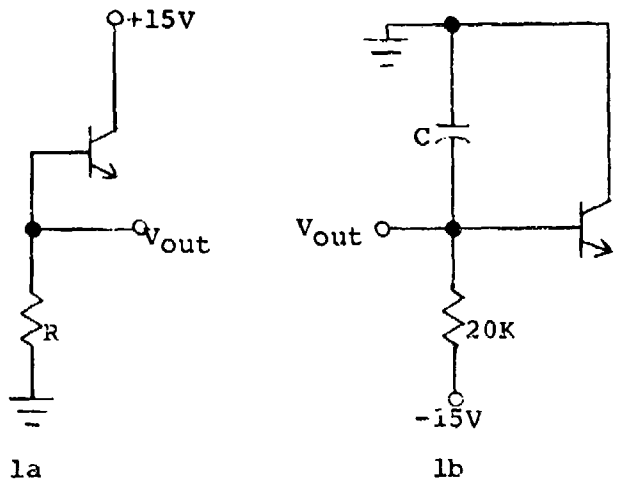

FIGURE 1

TEST CIRCUITS FOR PRIMARY PHOTOCURRENT MEASUREMENTS

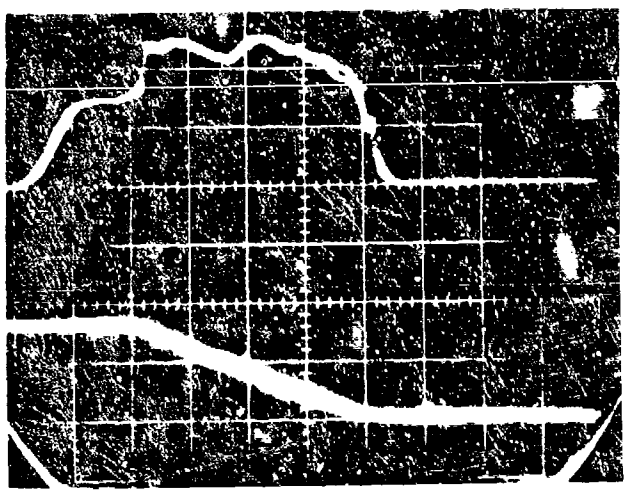

Figure 2 - TRANSIENT RESPONSE OF 2N5805 AT 10^8 r/S
TOP TRACE - V_{out}, in Fig. 1a
R = 10
VERT - 4 V/cm
HORIZ - 1 uS/cm
BOTTOM TRACE - ACCUMULATED DOSE

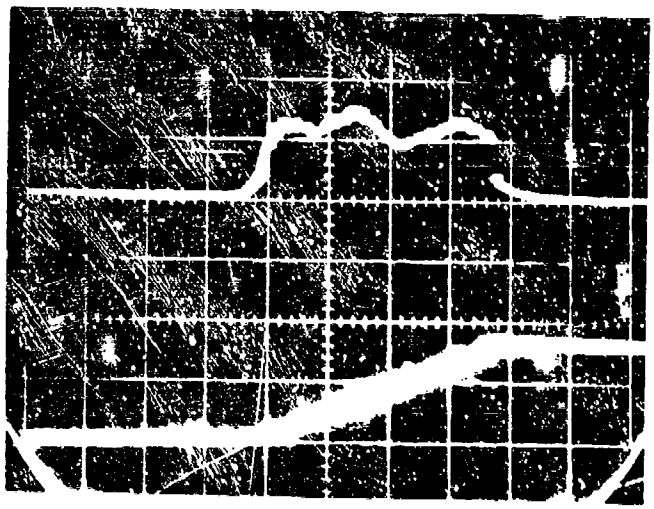

Figure 3 - TRANSIENT RESPONSE OF W1714-1405 AT 10^8 r/s
TOP TRACE - V_{out}, in Fig. 1A, R=10
VERT - 2 V/cm
HORIZ - 1 uS/cm
BOTTOM TRACE - ACCUMULATED DOSE

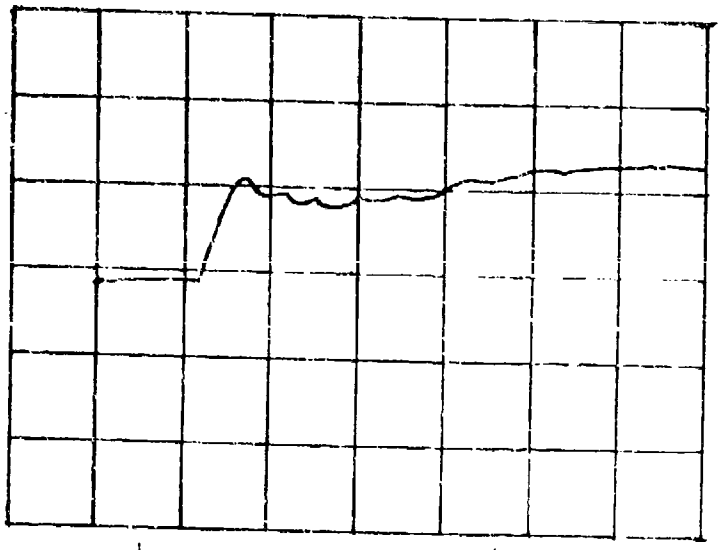

Figure 4 - TRANSIENT RESPONSE OF BR100B AT 10^{12} r/s
V_{out} IS SHOWN, in Fig. 1b,
C = .1 uF
VERT - 5 v/cm
HORIZ - .1 us/cm

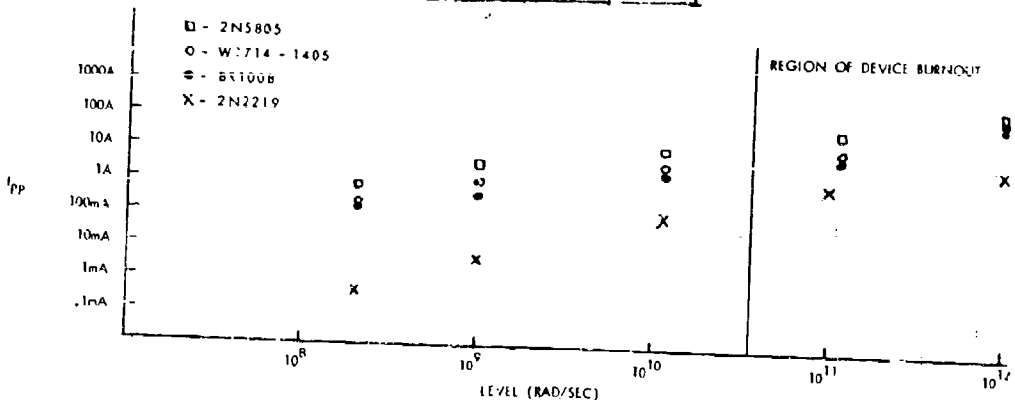

FIGURE 5 - I_{PP} vs GAMMA-DOT LEVEL

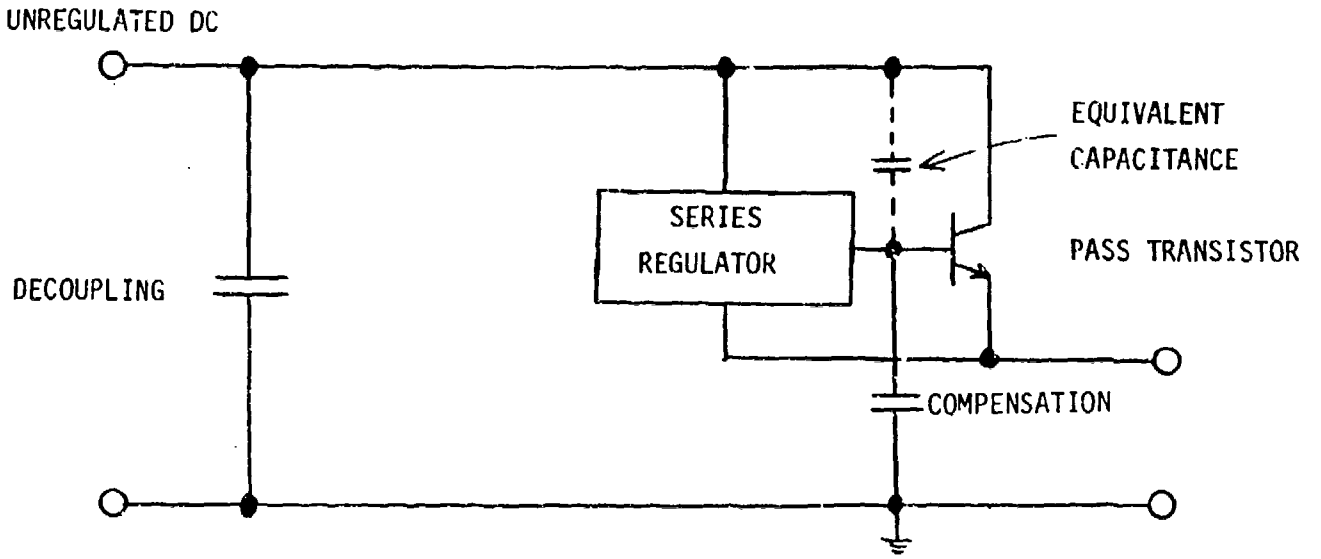

FIGURE 6 EXAMPLE OF EQUIVALENT COLLECTOR-BASE CAPACITANCE

TRANSIENT IONIZATION TESTING OF PULSED MICROWAVE TRANSCEIVER MODULES DESIGNED FOR PHASED-ARRAY RADAR APPLICATIONS*

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ABSTRACT

The importance of radiation-hard microwave T/R modules in phased radar systems necessitates well-planned and well-executed radiation testing of such circuits.

This paper describes the test equipment and techniques required for transient ionization data acquisition and the representative data that may be obtained from a typical module.

INTRODUCTION

The importance of the phased-array transceiver module is embodied in the combination of low-noise signal reception and high-power transmission capability in an independent operating entity. Array versatitlity and long-term useful life are the designer's aim. Each is achievable by realizing a high MTBF module and graceful degradation of the array associated with a large number of array elements. Reliable integrated circuits (logic and microwave) provide a compact combination to achieve the system aims and associated nuclear hardness.

Irradiation of solid-state circuits by an ionizing source results in the generation of transient anomalous currents. Most prominent are photocurrents caused by carrier generation within the depletion volume of a reverse-biased PN junction. Transistor action may produce a pulse of current many times the primary photocurrent generated in the collector base junction.

Additionally, high-ionization dose rates result in electron displacement currents in materials and between adjacent conductors, possibly causing device failure due to burnout.

MODULE DESCRIPTION

The L-band transceiver, shown in block-diagram form in Figure 1, is realized in three sections: receiver, transmitter, and common circuitry. The receiver is composed of a three-stage, class A amplifier characterized by 34 dB of gain, a 3.5-dB noise figure, and a limiter providing incident power protection for levels up to 40 watts. The transmitter, a series connection of class A and class C power stages, is designed to achieve 40 to 60 watts output power at long-term duty cycles exceeding 30 percent.

*This work supported by the U.S. Army ECOM under Contract DAAB07-71-C-0202.

Common to both transmit and receive functions are the four-bit line-length phase shifter, logic, channel T/R switch, and circulator. These circuits are centrally located to optimize both modes of operation.

Thin-film substrates, beam-lead components, chip ICs, and discrete microwave transistors are integrated to fabricate each module. Two exceptions are the Kapton d-c interconnect and the antenna port circulator. Finally, the electrical functions are enclosed in a hermetically sealed nickel-plated aluminum housing.

IONIZATION TEST DESCRIPTION

A block diagram of the test box used for transient ionization tests is shown in Figure 2. A 90-volt battery is used to bias two PIN diodes which are a-c coupled across a 50 Ω load into an oscilloscope. The outputs of the diodes, placed at critical points on the module, are used to monitor ionization dose rate and the shape of the ionizing pulse. Transient monitoring of all bias supplies is accomplished through the use of current transformers and capacitor noise suppression, as described in the TREE handbook.

Figure 3 shows the method used to profile the radiation dose rate received by the module. Strategically placed TLD discs are employed to determine dose-rate uniformity and the intensity of the radiation pulse as seen by various module circuits, e.g., receiver, power final, and logic. Experimental results showed that the dose rate at dosimeter A1 was ≅ 7.2 times that at either B1 or B2; hence, the latter were used for radiation monitoring during the actual tests so that the dose rate received by the module is not altered by the presence of a dosimeter between it and the X-ray beam. Peak dose rate is taken as this 7.2 multiplication factor times the average dose rate received by TLDs B1 and B2.

The logic switching circuit serves as a parallel-to-serial converter, simulating the module logic requirements of two 4-bit parallel-phase words, a 4-bit clock, and transfer pulse.

All biases, transmit-receive switching, and phase-shifting logic connections are made with a shielded, multiconductor cable between the test box and the module. In addition, the test box is shielded against EMP and RFI to minimize noise pickup on the bias lines and PIN monitor cables. Connections from the box to bias supplies and oscilloscopes are made with appropriately loaded 50 Ω cables to prevent mismatch-induced transients.

Figure 4 shows the technique used for r-f pulsing the module during testing in the transmit mode. The r-f source is voltage tunable and set for operation at midband frequency. Bias for the r-f source is supplied by a remotely triggered pulse generator with the trigger signal derived from the control panel of the ionization source. Bias pulse width and amplitude are chosen to produce the required module output power and pulse length. Delay may be introduced between the trigger and output of the pulse generator so that the ionization pulse can occur at an arbitrary point during the transmit pulse. Use of the circulator and 3-dB pad reduces mismatch at the input of the module.

Ionization pulses for these tests were obtained from the 2-MeV Flash X-ray (Febetron 705) at Kirtland Air Force Base. Because of the short penetration depth of electrons in aluminum and other module materials, a sheet of tantalum was used as a Bremsstrahlung converter and tests were run under X-ray irradiation. The generated ionization pulses have an effective pulse width of 25 to 30 ns (half-power points) and the delay between the control panel trigger pulse and onset of the X-ray beam is continuously variable up to 100 ms.

TYPICAL RESULTS

Figures 5 through 8 show typical transients observed on the bias lines when a module is subjected to an ionization dose rate of greater than 10^{11} rads (Si)/s. The r-f pulse produced during transmit has a width of 500 μs. The 5-volt line (Channel A) biases the module's logic circuitry, the −15 volt line (Channel B) powers the receiver and power preamplifiers, and the 28-volt line (Channel C) is used as the power amplifier final bias supply.

Figures 5 and 6 show the response of the module to an ionizing pulse while in the transmit mode. A delay of 12 μs was introduced between the beginning of the scope traces (as triggered by the Flash X-ray control panel) and the onset of the radiation pulse. The same delay is used for radiation pulsing while the module is in a receive mode; its response under these conditions is indicated in the photographs of Figures 7 and 8. Saturation effects of the current transformer monitoring Channel C result in the waveform exhibited by the bottom trace of Figure 5.

Figure 9 shows the outputs of the PIN diodes during a typical ionization pulse. Effective pulse width is taken as 25 ns and previous calibration of the diodes show an output of $\cong 6.5 \times 10^{-10}$ V/rads(Si)/s (across 50 Ω) at the ionization dose rates to which the modules were subjected.

Table 1 indicates the circuitry of the module biased by Channels A through C and the quiescent current level of each channel. The last two columns show the amplitudes and recovery times of the transients shown in Figures 5 through 8.

A sufficient and intelligent choice of network parameters must be evaluated to detect any permanent effects due to irradiation. NF, gain, phase shift and linearity, and logic switching effectively summarize receiver operation. Power output, efficiency, pulse droop, and phase settling are recorded as basic transmitter parameters. Table 2 typifies parametric effects on the T/R modules due to ionizing radiation.

CONCLUSIONS

Concurrent ionization testing and electrical evaluation of the modules revealed several critical points. The unavailability of proper r-f equipment for module evaluation at the radiation site makes necessary the use of indirect factors for determining survivability to an ionizing pulse. Both quiescent bias current levels and the presence of a power pulse on the transmitter bias line can be recorded to indicate parameter degradation or catastrophic failure of the transmitter section.

Proper test design and shielding are required to reduce EMP and noise generation because they may be sufficiently high to cause component failure due to overvoltage stress. Noise voltages as high as 60 volts have been observed on module bias lines during improperly designed ionization tests. An example of this is shown in Figure 10, a photograph of open-circuit noise levels on the −15 volt and 5-volt lines taken during an X-ray pulse with the employment of inadequate shielding around the module and bias lines.

The stability of any r-f equipment used to test the module before and after ionization pulsing is a critical parameter. Long-term stability is a necessity to prevent misread parameter changes as being attributable to ionization-induced degradation.

Indications of susceptibility to transient ionization pulses are expressed in r-f parameter degradation or catastrophic failure. Results based on failure analysis indicate that high-level, ionization-induced currents temporarily overstress circuitry (e.g., power stages operated near maximum limits) that is normally under electrical stress, but may not generate immediately detectable failures. Proper current limitation and circuit design will help alleviate this condition.

Channel	Voltage (V)	Circuitry Biased	Operation Mode	Quiescent Current (mA)	ΔI (mA)	T_r (μs)
A	5	Logic	T	350	90	10
			R	350	60	20
B	−15	Power Preamp, Receiver	T	25	35	10
			R	50	15	7
C	28	Power Output Stage, Power Preamp	$T(RF_{in} = 0)$	15	–	–
			$T(RF_{in} = 0.1\ W)$	6000	–	–
			R	15	100	8

Table 1. Typical Quiescent and Transient Current Levels During an Ionization Pulse

Parameter	Pre-Ionization	Post-Ionization	Δ
	RECEIVER		
NF	4.15 dB	4.0 dB	–0.15 dB
Gain	26.4 dB	27.0 dB	+0.6 dB
ϕ Shift Accuracy	4.4°	4.2°	–0.2°
ϕ Linearity	–1.1°	+1.8°	+2.9°
Logic Operation	OK	OK	OK
	TRANSMITTER		
Power Output	45.5 W	47 W	+1.5 W
Efficiency	28.6%	29.8%	+1.2%
Pulse Droop	0.15 dB	0.3 dB	+0.15 dB
ϕ Settling	24.0°	20.8°	–3.2°

Table 2. Typical Ionization-Induced Changes

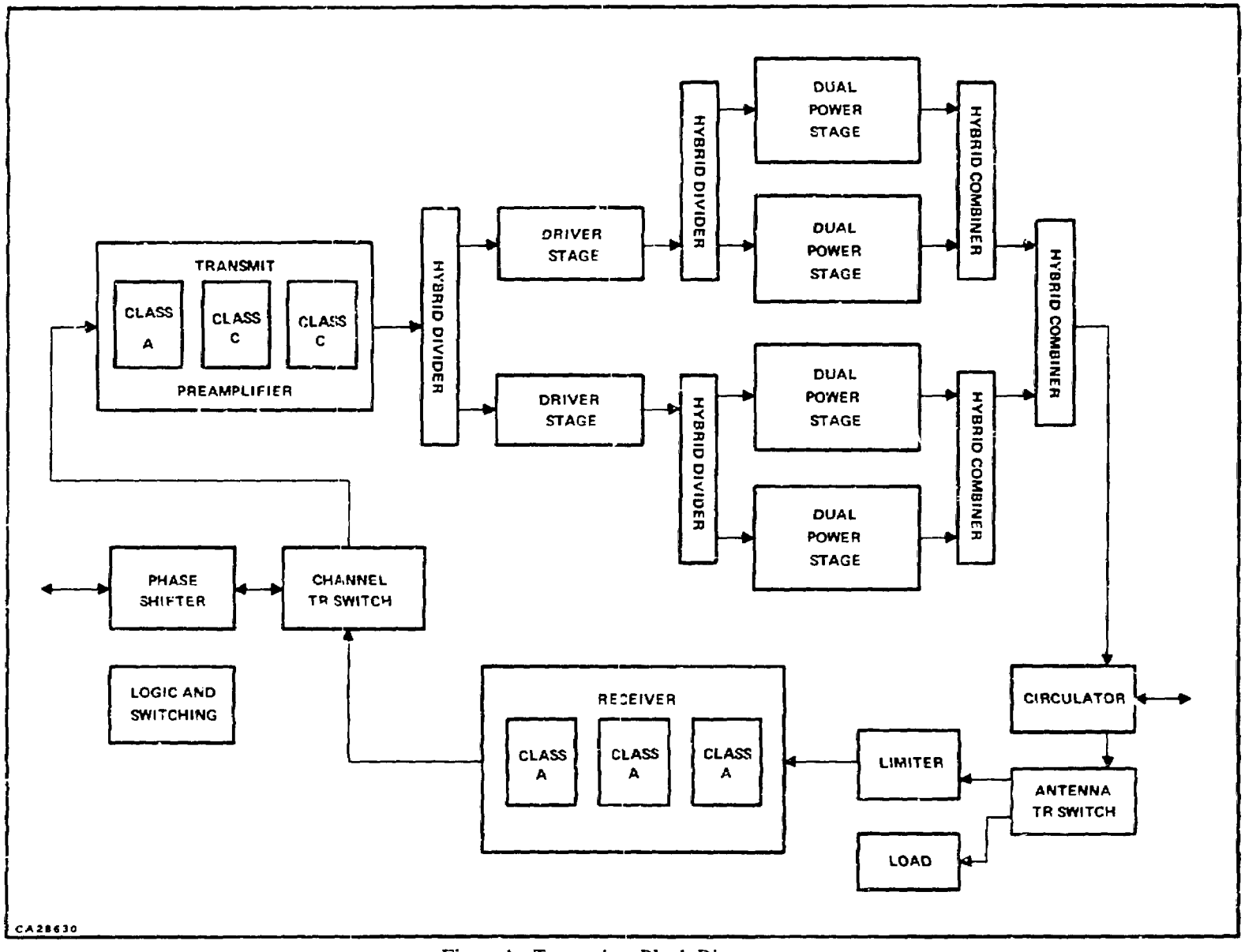

Figure 1. Transceiver Block Diagram

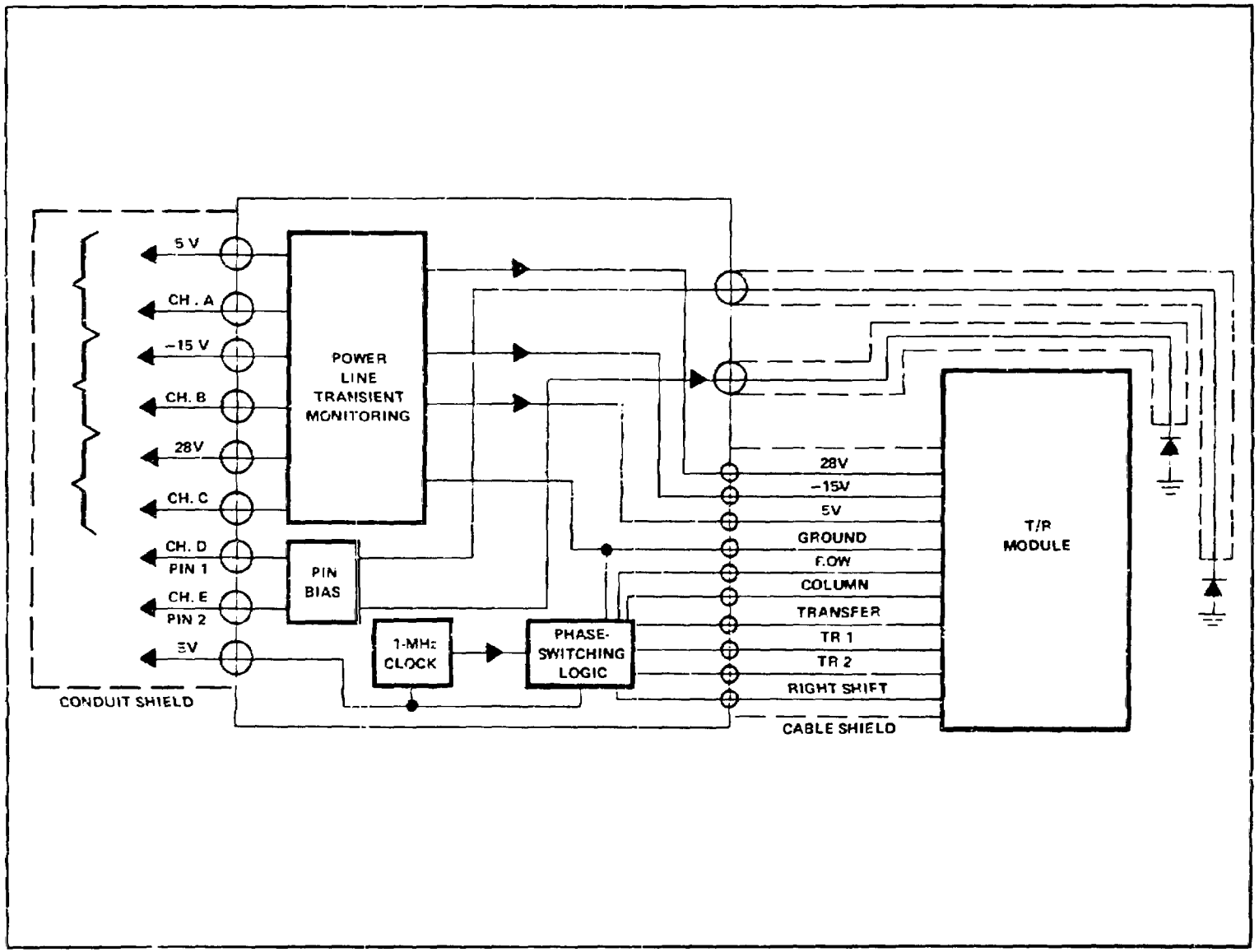

Figure 2. Test Box for Ionization Tests on Phased-Array T/R Modules

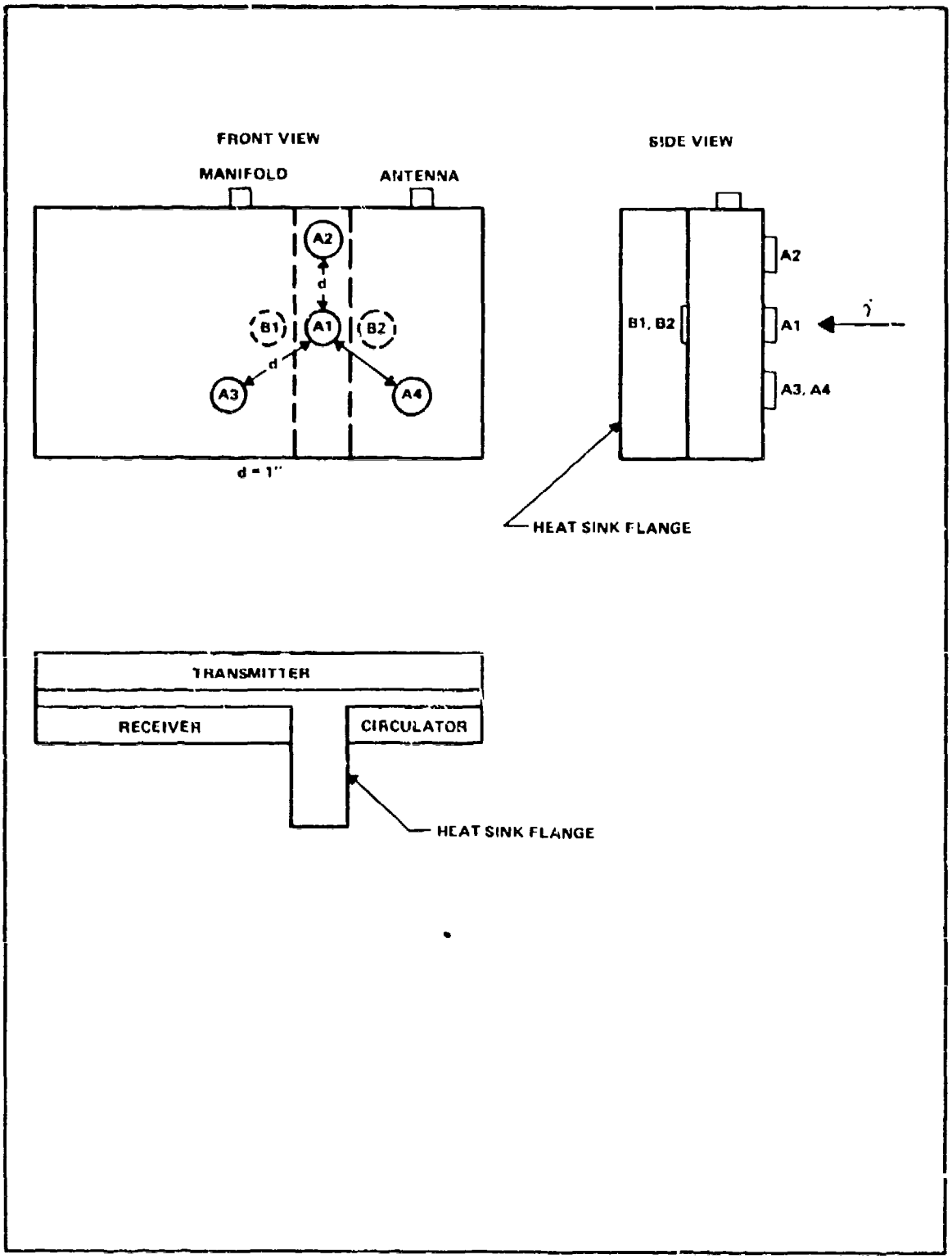

Figure 3. Dose Rate Profiling

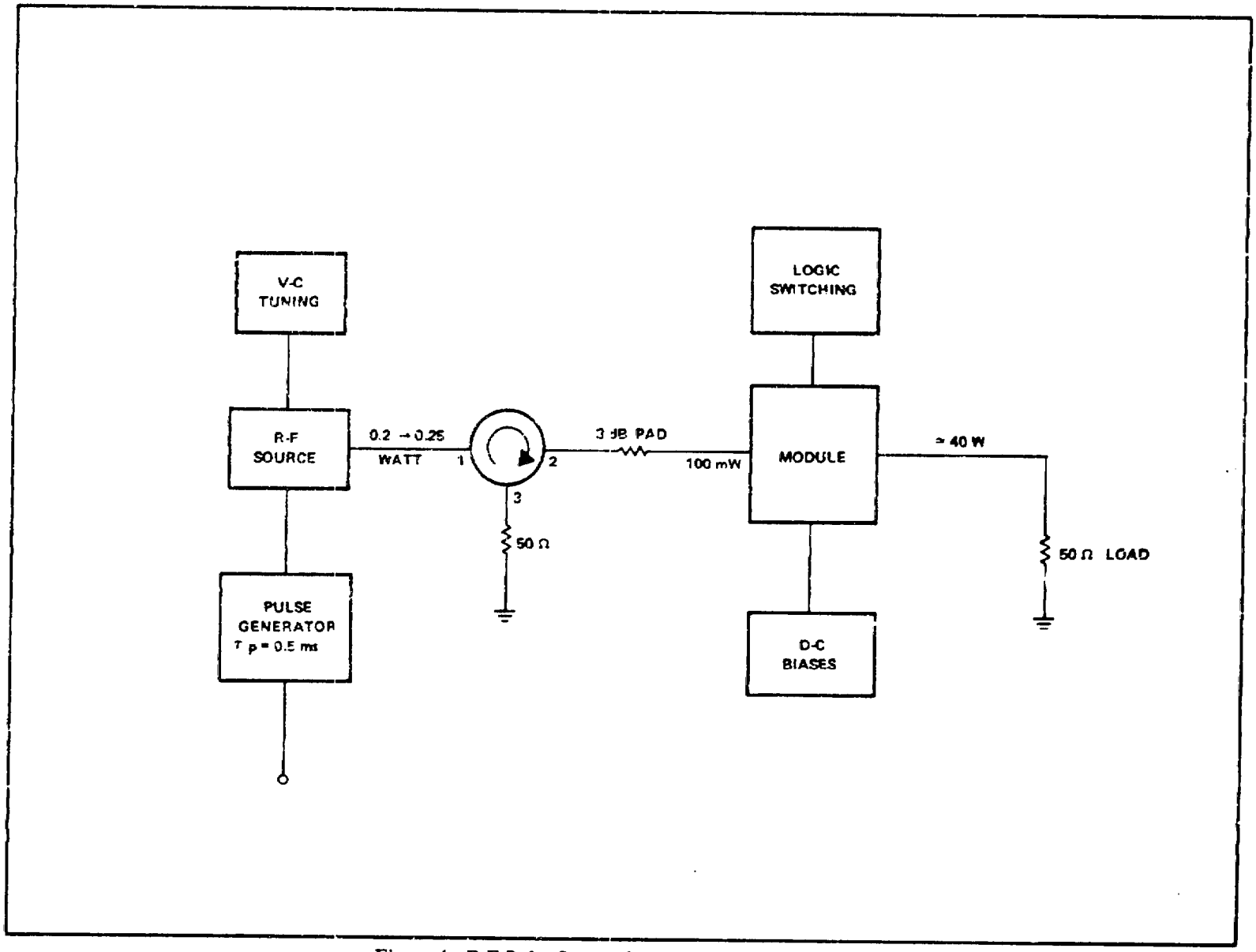

Figure 4. R-F Pulse Source for Transmit-Mode Testing

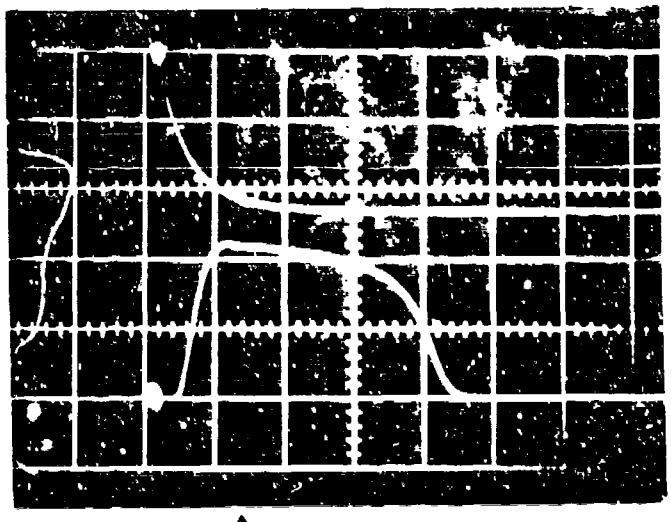

Figure 5. Ionization Pulse, Module in Transmit Mode
Top: Bias Pulse for R-F Source, 10 V/Div.
Bottom: Channel C, 2 A/Div. 10 μs/Div. Horizontal

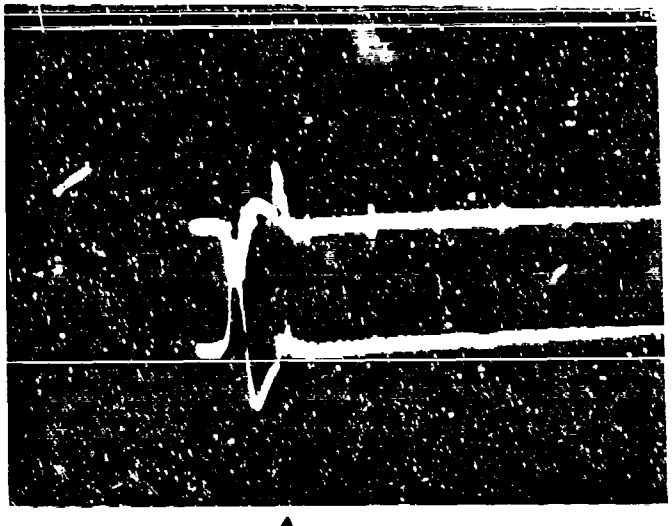

Figure 6. Ionization Pulse, Module in Transmit Mode
Top: Channel A, 0.1 A/Div.
Bottom: Channel B, 40 mA/Div. 10 μs/Div. Horizontal

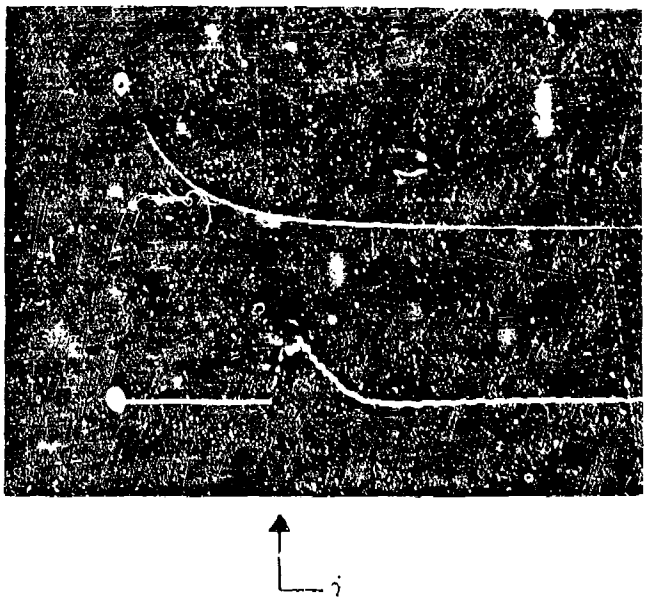

Figure 7. Ionization Pulse, Module in Receive Mode
Top: Bias Pulse for R-F Source, 10 V/Div.
Bottom: Channel C, 0.1 A/Div. 5 μs/Div. Horizontal

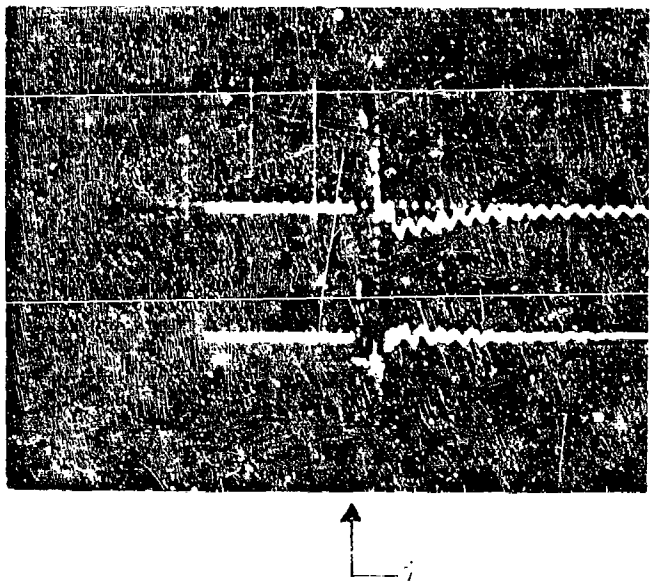

Figure 8. Ionization Pulse, Module in Receive Mode
Top: Channel A, 40 mA/Div.
Bottom: Channel B, 20 mA/Div. 5 μs/Div. Horizontal

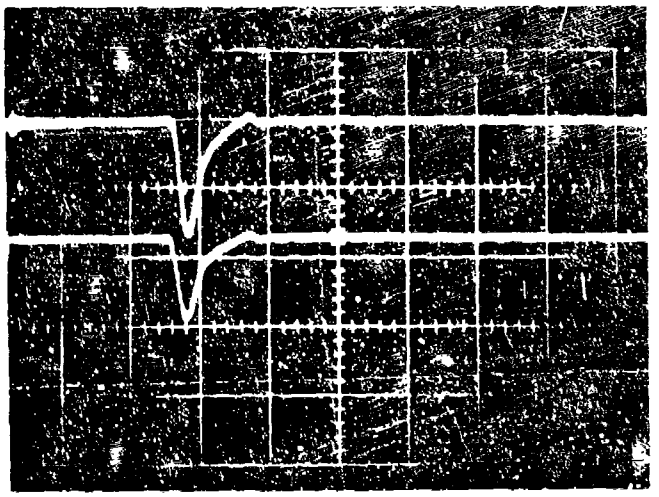

Figure 9. Monitoring of Ionization Pulse by PIN Diodes
10 V/Div. Vertical, 100 ns/Div. Horizontal

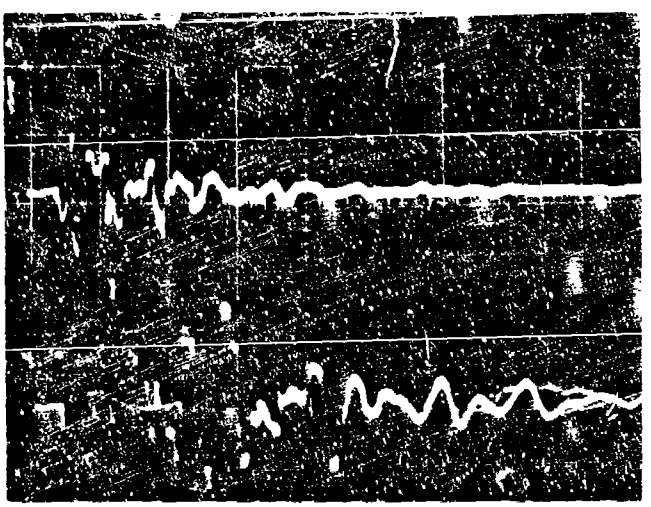

Figure 10. Ionization-Induced Transients on Open-Circuit Bias Lines
Top: Channel A, 20 V/Div.
Bottom: Channel B, 20 V/Div. 0.2 μs/Div. Horizontal

MINIMUM DELAY/HARDWARE ECL OR/NOR 4-VARIABLE FUNCTION SYNTHESIS CATALOG*

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Hughes Aircraft Company
Culver City, California 90230

ABSTRACT

A minimum delay, minimum hardware ECL OR/NOR Gate Synthesis Catalog has been generated for implementation of every four variable logic function together with its complement. The computer program used to generate the catalog is discussed. Use of the catalog in the synthesis of an arbitrary logic function is illustrated.

1.0 INTRODUCTION

As a prelude to ongoing integrated logic circuit development work, a fairly comprehensive study was undertaken to determine the capabilities of existing ECL for high performance digital communication and signal processing applications. As a part of our preliminary work, a special computer program was written and used to find the minimum delay, then minimum hardware, 4 input ECL OR/NOR gate networks for generation of each 4 variable logic function together with its complement. The computer program and the derived catalog are discussed in this paper. Statistics on delay and hardware costs are presented; use of the catalog in finding the minimal synthesis of an arbitrary 4-variable logic function is illustrated.

Attention is restricted in the catalog to interconnections of 4-input OR/NOR (Current Switch Emitter Follower) gates which have an (Emitter) output OR-wired logic-capability; wired logic fan-in of at most 4 is assumed though this does not meaningfully restrict derived syntheses. Results derived will not be immediately applicable to emerging medium performance ECL MSI/LSI in which both collector and emitter wired-logic can be used. Currently very high performance (e.g., 200ps T_{pd}) ECL is being produced only as single gate SSI chips, however, and results derived can be used directly for these circuits.[1]

*The work reported was sponsored by the Air Force Avionics Laboratory in the context of work on the Maximum Speed Multiplier Organization Program (Contract No. FY1175-71-00865-TE). These efforts have been guided by Lutz J. Micheel, Air Force Project Engineer under the direction of Robert D. Larson, Chief AFAL/TEA Branch.

Although there are 2^{16} distinct four input logic functions, these are subdivided among only 222 different (hardware) equivalence classes. Functions within each equivalence class differ only in the way that input and output connections are made to/from a fixed interconnected gate network. All functions within a given class are implemented with one circuit by interchanging (permuting) input connections and/or connecting complemented input variables (instead of uncomplemented variables) and/or using the complemented (instead of uncomplemented) circuit output. For ECL synthesis, complement input variables are produced simultaneously by the driving ECL gates; similarly, each 4-variable logic circuit produces the complemented and uncomplemented functions. In view of the above, this study was restricted to finding the minimal synthesis for the one required circuit for each of the 222 equivalence classes. Consideration was further restricted to networks in which both the function and its complement were generated simultaneously. *

2.0 COMPUTER PROGRAM REQUIREMENTS

Four-input ECL Current Switch Emitter Follower OR/NOR gates with an output wired-logic OR capability (with wired-OR fan-in of 4 or fewer) were used as the gate building blocks. Since available ECL can support fan-out loads of usually greater than 10, no limit was placed on the number of inputs to each four-variable circuit. Driving circuits were assumed to supply either the input variable x_i or its complement $\bar{x}_i$ or both. The program was designed to find the minimum circuit that produces (at the same time) both the function and its complement.

The minimization criteria used are listed below in order of decreasing importance; i.e., each criterion was satisfied subject to the constraint that all previous criteria were satisfied first:

1. Minimum number of levels of gating
2. Minimum number of total gates
3. Minimum number of first level gates (gates all of whose connected inputs are connected directly to the input variables)
4. Minimum number of leads to which input variables are connected (Corresponding to minimum number of literals in Boolean expression for f)

5a. Minimum number of wired logic nodes.

5b. Maximum number of wired logic nodes.

Criteria 2 and 3 are equivalent, as is shown shortly.

---

*A somewhat similar study was most recently reported by Muroga,[2] et al., but was restricted to the much smaller set of (22) equivalence classes of three variable functions. In this work, delay was NOT considered, and attention was focused on gate count and numbers of input connections only.

3.0 PROGRAM DESCRIPTION

The program used hinges on several simplifying logic circuit properties which follow when ECL with wired-logic is used. (Exhaustive search techniques such as those used by Hellerman[3] were not required.) These properties may be stated concisely as two theorems and a definition;* the second theorem outlines the steps performed by the program.

Theorem 1

Any minimal "NOR" synthesis of a 4-variable logic function requires at most two levels of gating. If two levels of gating are needed for a particular function, then only one second level (output) gate is used. Each first level gate has at least two input variables. Furthermore, the "OR" (uncomplemented) output of each first level gate is never used as an input to the second level gate.

From these results, it follows that a minimal synthesis can be derived straightforwardly from the minimal sum of products Boolean expression for a representative logic function for each equivalence class. The minimal Boolean expression is defined as follows.

Definition (Minimal Boolean Expression). A sum of products (e.g., $x_0\bar{x}_1x_2 + x_0x_1\bar{x}_2\bar{x}_3 + x_3$) is minimum if it satisfies the following criteria in order of decreasing importance (i.e., if each criterion is satisfied subject to the constraint that all above are satisfied first).

1. The number of operation types (e.g., AND, OR, etc.) in the expression is minimum (there can be at most two).

2. The number of terms is minimum.

3. The number of literals is minimum.

The algorithm used by the computer synthesis (in terms of this definition) is given in the second theorem.

Theorem 2

The following procedure will yield a minimal synthesis for a logic function f:

> First obtain minimal expressions for f and for $\bar{f}$ and select the smaller. (If both are equal, select either one.) Let g equal the function corresponding to the selected minimal expression (i.e., g with be either f or $\bar{f}$).

---

*Proofs will be offered in the conference presentation. While straightforward, they involve treatment of several special cases.

Case 0. If the selected expression has no literals, g is degenerate. In this case both g and $\bar{g}$, hence f and $\bar{f}$, are simultaneously synthesizable with no gates. (This case applies to only one equivalence class.)

Case 1. If the selected expression has exactly one literal, then g, and hence f, is of the form x_i^{δ} ($i = 0, 1, 2, 3$; $\delta = \pm 1$; $\delta = +1$ for x_i and $\delta = -1$ for $\bar{x}_i$).

In this case f and $\bar{f}$ are simultaneously synthesizable with no gates. (This case also applies to one equivalence class.)

Case 2. If the selected expression has one term and that term is the product of more than one literal, then the minimal simultaneous synthesis of f and $\bar{f}$ uses one "NOR" gate. The inputs to the gate are the complements of the factors in the single term of the selected expression, and g, $\bar{g}$ appear at the "NOR" and "OR" outputs of the gate, respectively. Hence f appears at one of these outputs and $\bar{f}$ at the other, depending upon whether $f = g$ or $\bar{f} = g$. (This case applies to three classes.)

Case 3. (All other equivalence classes). If the selected expression has more than one term, the minimal simultaneous synthesis of f and $\bar{f}$ will have two levels. Each term with more than one literal will correspond to a first level gate, and the inputs to that gate are the complements of the factors in the term. Thus the number of first level gates is equal to the number of terms in the selected expression that have more than one literal. The inputs to the second level gate will be the "NOR" outputs of the first level gates (using wired "OR"ing of these outputs, as necessary) and the variables that appear as terms of the selected expression having a single literal. If $f = g$, then f and $\bar{f}$ appear at the "OR" and "NOR" outputs of the second level gates, respectively; otherwise the outputs are reversed.

4.0 ECL SYNTHESIS CATALOG

The computer program embodying the above algorithm was used to generate a 222 page catalog. Typical pages are shown in Figures 1, 2, and 3. Each is headed by its class number and class identifier (discussed in Section 5). Also included are a Karnaugh Map of the function synthesized, a hardware data summary, and the gate circuit configuration.*

Some of the more useful statistics governing minimal ECL synthesis of 4-variable logic functions are shown in Figure 4. It was found that simultaneous synthesis of each output and its complement for 4-variable functions require an average delay of about 1.97 stages and that an average network requires about 4.35 gates. Statistics related to the loading of the ECL circuits driving the four variable networks are presented in Figures 5 through 7.

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*The complete catalog will be available in the near future as a Hughes special report.

Figure 5 shows the distributions for the maximum and minimum input loading by displaying the largest and smallest numbers of gates in a network synthesizing a 4-variable function which are driven by any one network input signal. Figure 6 shows a distribution for the number of input variables (from the eight possible)* used in the 4-variable function syntheses and Figure 7 presents the equivalence class distribution versus the number of inputs to all gates in the 4-variable networks that are driven from the network inputs. One useful interpretation of these data is as follows. The mean from Figure 6 indicates that on the average, 6.97 of the eight possible inputs are used to synthesize 4-variable functions and their complements. Then dividing the number of used internal gate inputs by this average permits interpretation of Figure 7 (lower abscissa scale) as a distribution of the equivalence classes versus the number of internal gates driven by each exterior input. In this case, the mean value in Figure 7 indicates that for the "average network" each of its 6.97 inputs is used to drive 11.6/6.97 = 1.66 gates inside the network. On the other hand as indicated in Figure 5, there are eight function classes in which at least one input signal must drive four gate inputs (from the "maximum curve"), and there are 108 function classes in which one of the input signals isn't used at all (see "minimum curve").

Figure 8 shows the statistics related to the utilization of wired logic within the four variable function networks. The "maximum curve" displays the number of equivalence classes versus the largest possible wired logic fan-in, and the "minimum curve" presents the minimum number of gate outputs wired together. For example, there are 52 of the 222 classes in which two gate outputs must be wired together to permit the two stage realization of both the functions and their complements.

5.0 SYNTHESIS OF AN ARBITRARY 4-VARIABLE LOGIC FUNCTION USING THE CATALOG

The catalog, which now exists, is used primarily to find the minimum delay/hardware ECL OR/NOR synthesis of any given 4-variable function. Before the catalog can be used, the equivalence class** of the given function first must be identified through classification. During the search for the function's equivalence class, one also generates all necessary permutations and complementations of the input variables and/or the output. When these permutations and/or complementations are applied to the inputs and/or the outputs of the

---

*These are x_0, x_1, x_2, x_3, $\bar{x}_0$, $\bar{x}_1$, $\bar{x}_2$, $\bar{x}_3$.

**Function classification is discussed by Harrison[4] who catalogs function syntheses for relay circuit mechanization and for DTL gate mechanizations. Unfortunately, his classification system, in our opinion, is unduly complicated and much less easy to describe than one given earlier by Golomb[5]. The classification procedure outlined in this paper is based on Golomb's work. The classification numbers given in the catalog, however, conform with Harrison's system. The conversion after completion of classification is accomplished easily, as will be shown shortly.

canonical gate network (shown on the catalog page listing the equivalence class), then that network realizes the minimum delay/hardware synthesis of that function and its complement.

Given an arbitrary 4-variable logic function, a procedure for finding its minimal synthesis via catalog look-up is as follows.

1. Compute the Walsh Transform of the (truth-table-like) function corresponding to the given function.

2. Manipulate the Walsh Transform (an array of 16 coefficients) to maximize its lexicographic order. The three kinds of rearrangements used correspond exactly to permuting input variables, complementing input variables, and complementing the output function.

3. Convert this sequence of coefficients to an equivalent Harrison sequence that will be a class identifier for one of the tabulated (cataloged) functions.

4. Construct the minimal function by connecting the catalog listed network but with variables permuted, and/or complemented, and/or with the output complemented precisely as was necessary to convert the Walsh Transform Array (in Step 2)

These steps are accomplished at Hughes by a simple computer program. For purposes of illustration, they are carried out in detail for the function depicted on the Karnaugh Map in Figure 9a.

Step 1

The function shown is converted to an equivalent truth-table like function shown in Figure 10 as follows. The interval from 0 to 1 is subdivided forming 16 sub-intervals. The first corresponds to the input state 0000, the second to 0001, etc., with the interval number in general following a standard binary sequence on the variables $x_3x_2x_1x_0$. The value of the converted function, $\hat{g}$ on each sub-interval is given by $1-2g$ (i.e., if $g = 0$, $\hat{g} = 1$ and if $g = 1$, $\hat{g} = -1$).

The Walsh Transform of the given function then is easily computed in terms of the converted function $\hat{g}$. This transform is a coefficient array (exactly analogous to Fourier Series) listed as

$$g_c, g_3, g_2, g_1, g_0, g_{32}, g_{31}, g_{30}, g_{21}, g_{20}, g_{10}, g_{321}, g_{320}, g_{310}, g_{210}, g_{3210}.$$

Each coefficient is the weighting term that could be multiplied by the corresponding Walsh function shown in Figure 11 to represent the

original function. Each coefficient $g_{i_1, i_2, \ldots, i_k}$ is computed (again like Fourier coefficients) by an inner product:

$$g_{i_1, i_2, \ldots, i_k} = 16 \int_0^1 \hat{g}(x)\, W_{i_1, i_2, \ldots, i_k}(x)dx \quad .$$

For example for the function of interest here,

$$g_{321} = 16 \int_0^1 \hat{g}(x)\, W_{321}(x)dx = -6,$$

where W_{321} is shown in Figure 11 and $\hat{g}(x)$ is as given in Figure 10. Actually the coefficient calculation involves a simple set of pairwise ±1 multiplications and a summation. The 16 Walsh coefficients for the given function g(x) are

$$-2, 6, -2, -6, -2, -2, -6, -2, 2, 6, 2, -6, -2, -6, 2, 2.$$

Step 2

Maximize the Lexicographic Order of the Walsh Transform array as follows. Invert the signs of all array coefficients. This inversion corresponds to complementation of the original function. The complemented function is depicted on the Karnaugh Map of Figure 9b and its Walsh coefficients are

$$2, -6, 2, 6, 2, 2, 6, 2, -2, -6, -2, 6, 2, 6, -2, -2 \ .$$

Change the sign of every Walsh coefficient whose subscript contains a "3" (e.g., g_{321} changes sign but g_{21} does not). This change corresponds to complementing the input variable x_3. A Karnaugh Map displaying the function after both the change of step 2a and this step, 2b, is shown in Figure 9c. The corresponding Walsh coefficient array is now given by

$$2, 6, 2, 6, 2, -2, -6, -2, -2, -6, -2, -6, -2, -6, -2, 2.$$

The final step in maximizing the Lexicographic order of the Walsh coefficient array involves interchanging variables. Here only an interchange of the variables x_1 and x_2 serves this purpose. When interchanged, the corresponding coefficients are interchanged in the Walsh array as follows. Each coefficient including a "1" is exchanged

with its counterpart which includes a "2" in its subscript (e.g., g_{31} and g_{32} are interchanged; note that g_{321} is not changed). The new Walsh array is now given by

$$2, 6, 6, 2, 2, -6, -2, -2, -2, -2, -6, -6, -6, -2, -2, 2.$$

and the corresponding function "1" is shown in Figure 9d.

Each of the above operations has increased the Lexicographic size of the Walsh Array; no further operations of the above type will permit further increase. Hence, the function f, having the last set of Walsh coefficients is the cataloged canonical function for the equivalence class to which g belongs.

Step 3

Although a Walsh coefficient array would most adequately represent each class, our catalog uses Harrison's identifier sequences to permit easy correlation with his previously published results. Conversion of a Walsh sequence to its equivalent Harrison sequence is accomplished by the simple formula:

$$H_{i_1, i_2, \ldots, i_k} = (1/2)(2^4 - W_{i_1, i_2, \ldots, i_k}).$$

For example, $H_3 = (1/2)(16 - W_3) = 5$. Using this formula for all coefficients results in

$$7, 5, 5, 7, 7, 11, 9, 9, 9, 9, 11, 11, 11, 9, 9, 7$$

as the Harrison class identifier of g (and also of f).

Step 4 (Catalog look-up and synthesis)

The above class identifier is located at the top of page 152 of the catalog (reproduced here as Figure 3). The minimal delay/hardware network shown for the (canonical) function f is also minimal for the function g; the input/output connections only are different, corresponding to the changes made in Step 2. To use the circuit, one performs the three operations used to convert the Walsh array but in reverse order. Specifically, first permute input variables x_1 and x_2, then complement input variable x_3, and then use the complement output. This sequence of operations is indicated schematically across the bottom of Figure 9 (right to left).

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4. M. A. Harrison, Introduction to Switching and Automata Theory, McGraw-Hill Book Company, New York City, New York, pps 123-167 and pp. 396-471, 1965.

5. S. W. Golomb, IRE Trans. on Circuit Theory, CT-6, Special Supplement, pp. 176-186, May 1959.

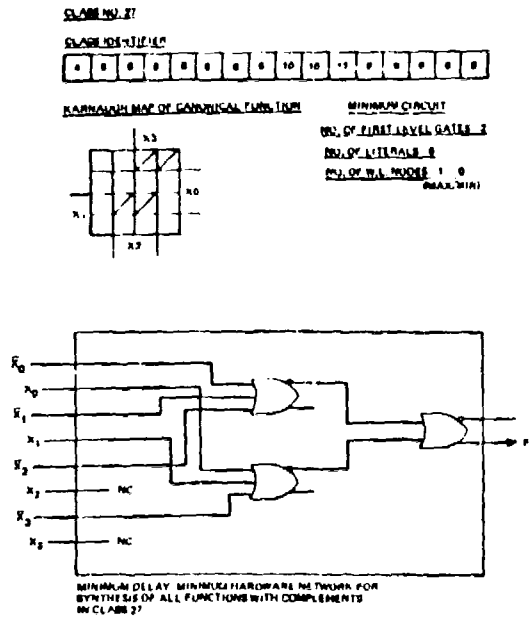

Figure 1. Page 27 of catalog showing minimum synthesis of "small" function

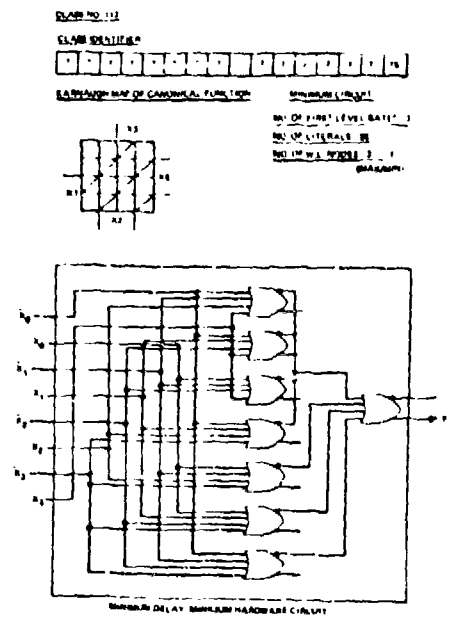

Figure 2. Page 112 of catalog showing minimum synthesis of "large" function

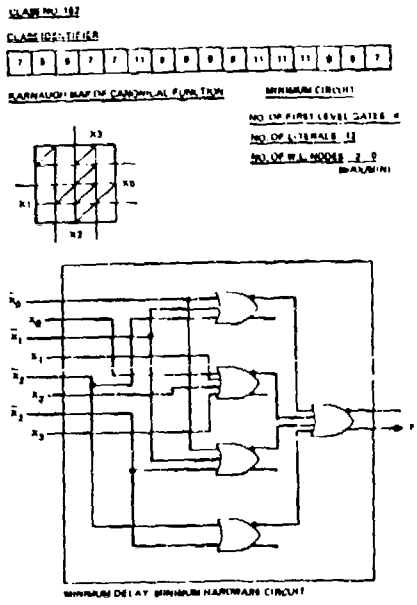

Figure 3. Page 142 of catalog showing minimum synthesis of "average" function

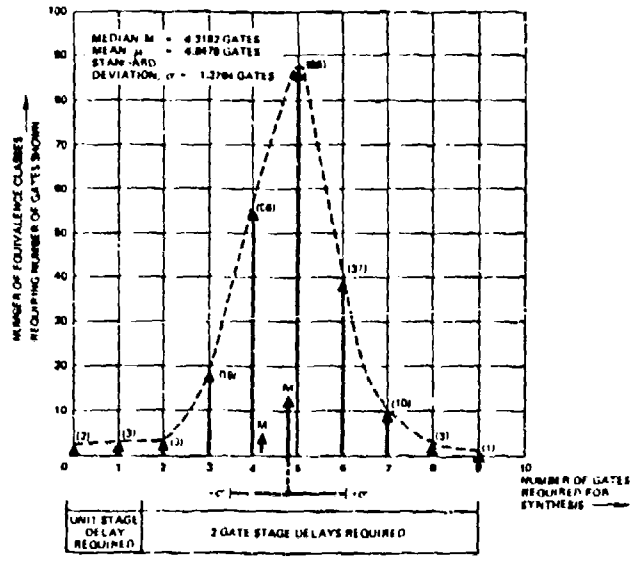

Figure 4. Statistical summary for minimum delay ECL OR/NOR gate synthesis of all 222 classes of 4-variable logic functions and complements

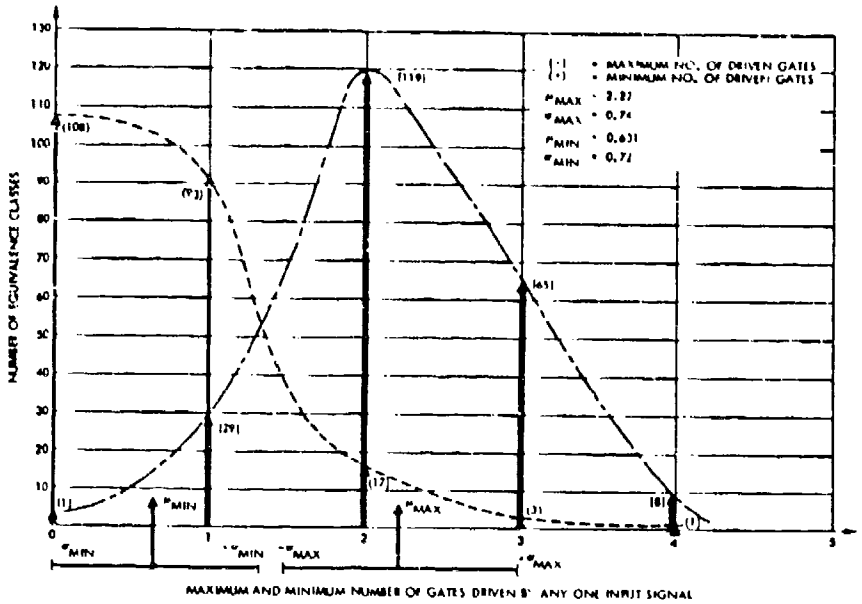

Figure 5. Number of equivalence classes versus maximum and minimum number of gates driven by any one input signal

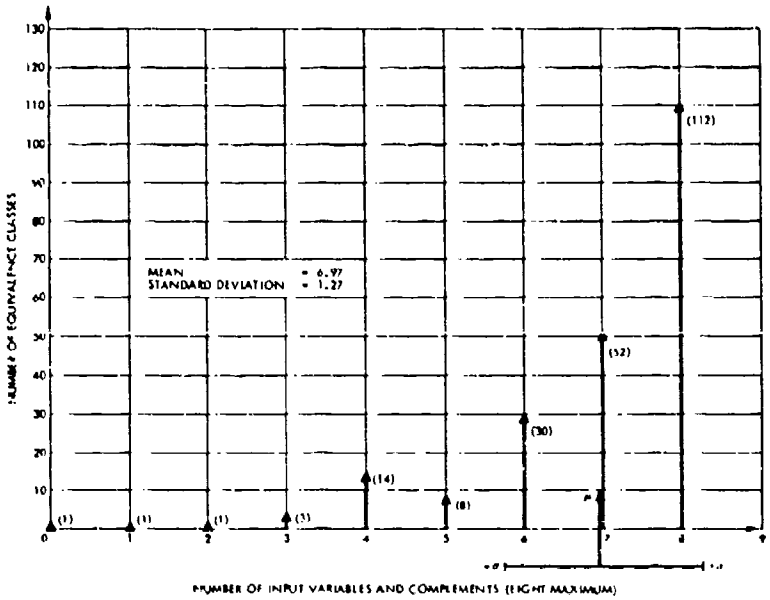

Figure 6. Number of equivalence classes for each number of input variables used

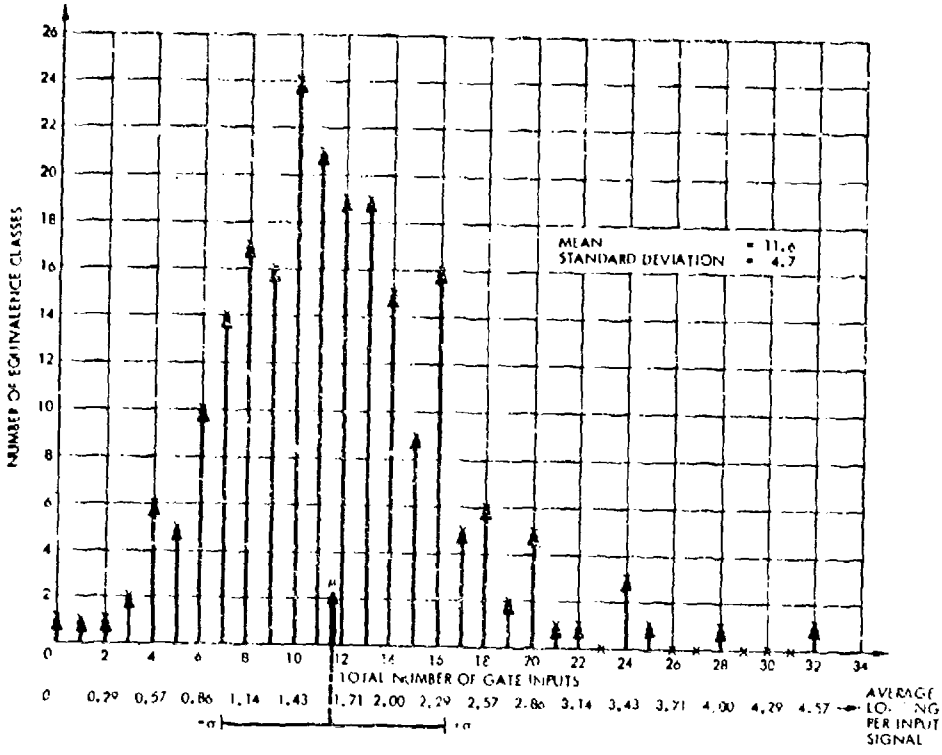

Figure 7. Number of equivalence classes versus number of gate inputs and average loading per input signal

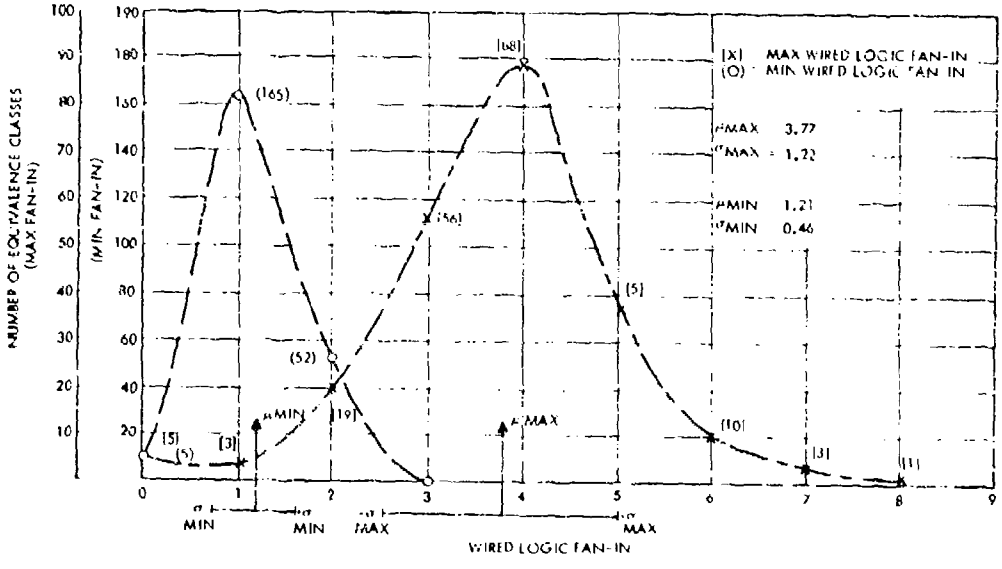

Figure 8. Number of equivalence classes versus maximum and minimum wired logic fan-in

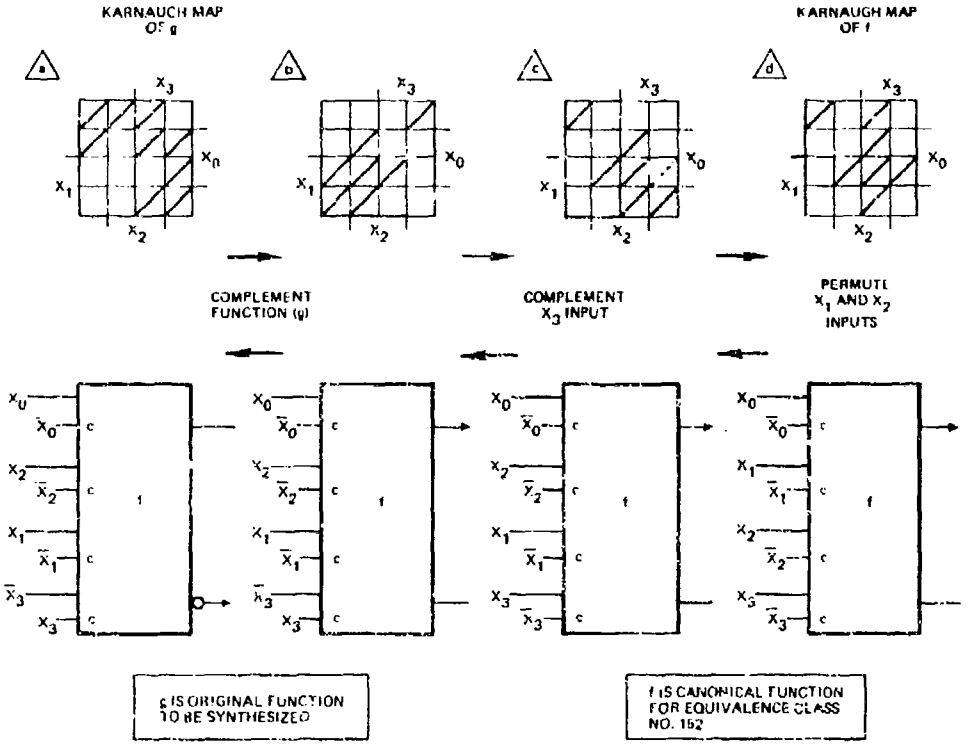

Figure 9. Example of conversion of given function to canonical form for catalog look up of minimum delay-minimum cost implementation

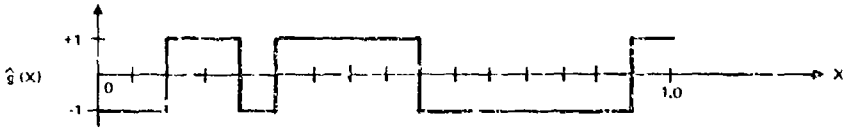

Figure 10. $\hat{g}(x)$ example function (where $\hat{g}(x) = [1-2g(x)]$) Evaluation of Walsh Transform of this function is first step in classification process

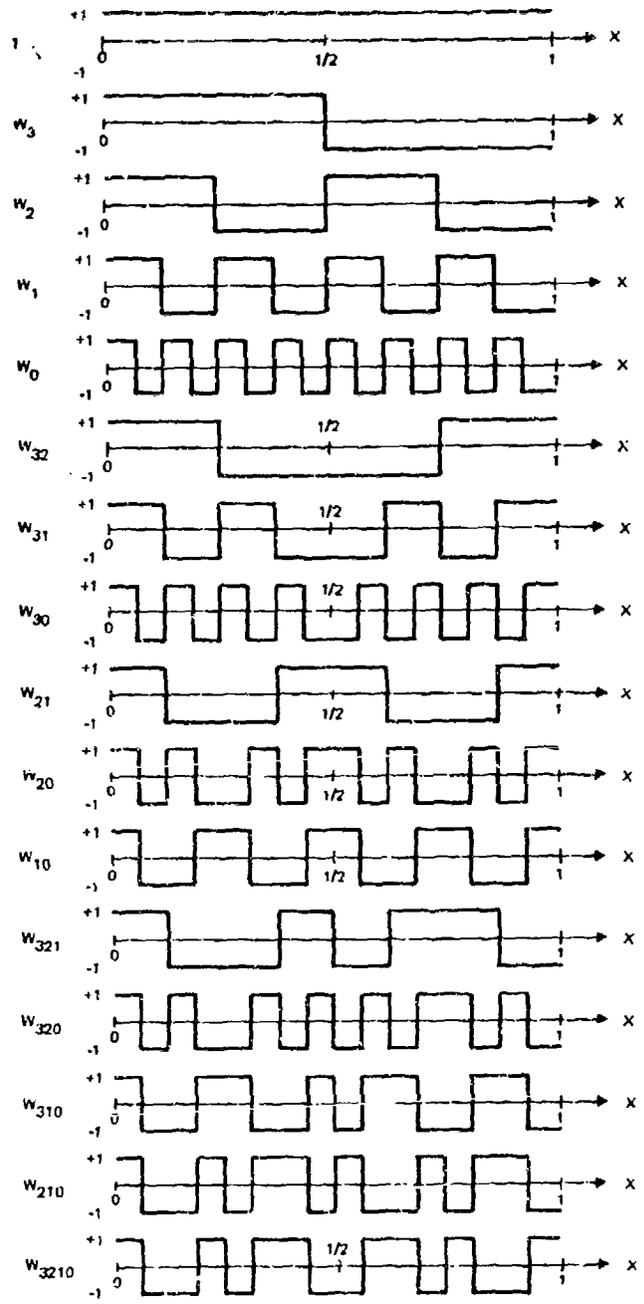

Figure 11. First 16 Walsh functions used in 4-variable function classification

ADVANCES IN HIGH SPEED A-TO-D CONVERSION

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ABSTRACT

Some limitations of the conventional approach to high speed analog-to-digital conversion are reviewed and two recent innovations in converter design are presented: the VAROM ("voltage addressable read-only memory") concept and the "sampling on-the-fly" concept. These novel design approaches lead to systems which are faster and more amenable to microelectronic implementation.

APERTURE

Analog to digital converters measure the instantaneous amplitude of an analog input signal and present the measurement result in digital form. Measurement, in this context, consists of determining in which one of 2^n subranges the signal amplitude fits, where n is the number of bits of the digital result.

With increasing signal frequency the time which the signal amplitude spends in any one subrange becomes shorter. In an n-bit converter a full range signal of maximum frequency, f, can traverse a subrange in the "minimum subrange transit time" $\tau = 1/(2^n \pi f)$. τ is a measure for the precision with which the time of measurement must be known. This time is established by the sampling procedure in which the continuous change of the input signal is periodically interrupted. The timing tolerance of this interruption is called "aperture" and it must be smaller than τ, the minimum subrange transit time. Figure 1 shows the relationship between n, f and τ. For processing a 100-MHz signal with a 6-bit resolution (appr. ± 1%) τ is 50 ps and the aperture must thus be smaller than 50 ps.

SAMPLING

In conventional high speed converters a narrow aperture is obtained with a fast opening switch or "sampling gate", in a track and hold configuration. (Figure 2). Such sampling arrangements are in principle capable of achieving very narrow apertures, partly because of the speed of the sampling gates used and partly because of the switch paradox, explained in Figure 3. In practice, however, track and hold sampling systems are found to be subject to many frequency and repetition rate dependent errors, which become prohibitive above 100 MS/s (100 megasamples per second).

In the novel approach of sampling on-the-fly some of the errors inherent in track and hold sampling are avoided. Sampling takes place in the digital domain after the analog signal has already been broken up into subrange signals. The analog signal remains continuous and is never interrupted. Consequently, no sampling transient is introduced in it as is the case in track and hold. The mechanization of sampling on-the-fly will be discussed in conjunction with the description of the VAROM converter approach.

CONVERTER ORGANIZATION

In conventional high speed converter systems the conversion invariably is carried out in a number of steps. Each step consists of comparison, reconversion of the digital result to analog, and subtraction of this latest analog value from the previous one. This is a cumbersome procedure, but it is attractive for two reasons: much less comparator hardware is required than for a one-step conversion and the second step of the conversion can be performed while the first step of the next conversion takes place, thus permitting a certain measure of speed-up by paralleling operations. With the advent of microelectronics the hardware savings afforded by conversion in steps has become less important and the time for a new generation of one-step high speed converters has arrived.

VAROM

While in conventional systems the digital output is generated as the conversion progresses, in the VAROM system all 2^n possible digital output words are already present and stored in a read-only memory. The voltage to be digitized is used to select the address in the memory that contains the correct output word. The basic VAROM structure is shown in Figure 4. A linear array of 2^n comparators, each with a different threshold which corresponds to one of the 2^n subranges, is followed by only one layer of logic, which feeds directly into the read-only memory. At any one time only one of the logic outputs is high, selecting the proper word in the memory. The comparators consist of a differential input amplifier followed by a strobed latch. The latch strobe acts as a sampling gate and its precise timing constitutes the major engineering task facing the VAROM designer. The simplicity and the potential for high speed of the VAROM system is obvious. Systems based on this principle

are expected to allow sampling rates of 400 MS/s with resolutions unattainable with less straightforward approaches.

The simplicity and repetitiveness of the VAROM structure invites a microelectronic implementation. To make such an implementation successful, a method had to be found for modularizing the read-only memory. Such a memory, if realized in a routine manner, would require 2^n access wires from widely separated points in the converter. The capacitance of these interconnections would be inconsistent with the high speeds of operation sought. An elegant solution to this problem is shown in Figure 5. The read-only memory is modularized in blocks of eight words. One type of module suffices. From its eight words all 2^n different words can be easily derived by a simple discretionary wiring method. For columns which are to contain zero's the module sense wires are left disconnected from the common sense buses. In a 30 MS/s, 7-bit converter, which was an early test vehicle built at the Advanced Technology Laboratories, the read-only memory module consists of fast, ultra-low capacitance silicon-on-sapphire diodes on a 55x55 mil substrate. This substrate is mounted in 1 inch square hybrid packages together with the IC's for eight comparator and associated logic gates.

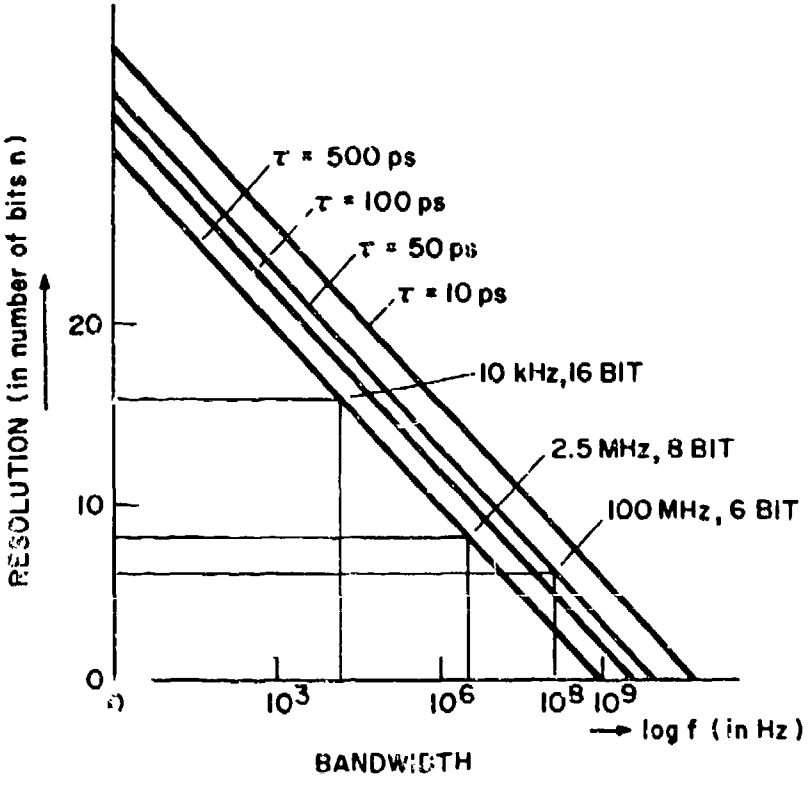

Figure 1. Relationship between the maximum frequency, f, and the resolution, n, with the minimum subrange transit time, τ, as parameter. The aperture time must be less than τ.

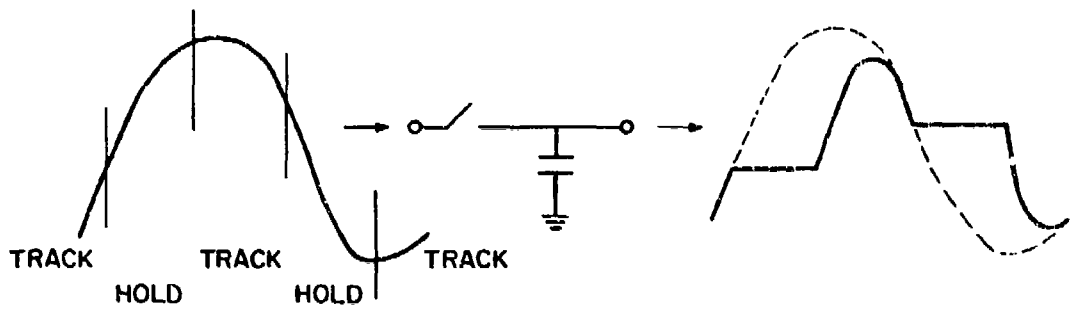

Figure 2. Conventional track & hold sampling. At high sampling rates errors tend to become prohibitive.

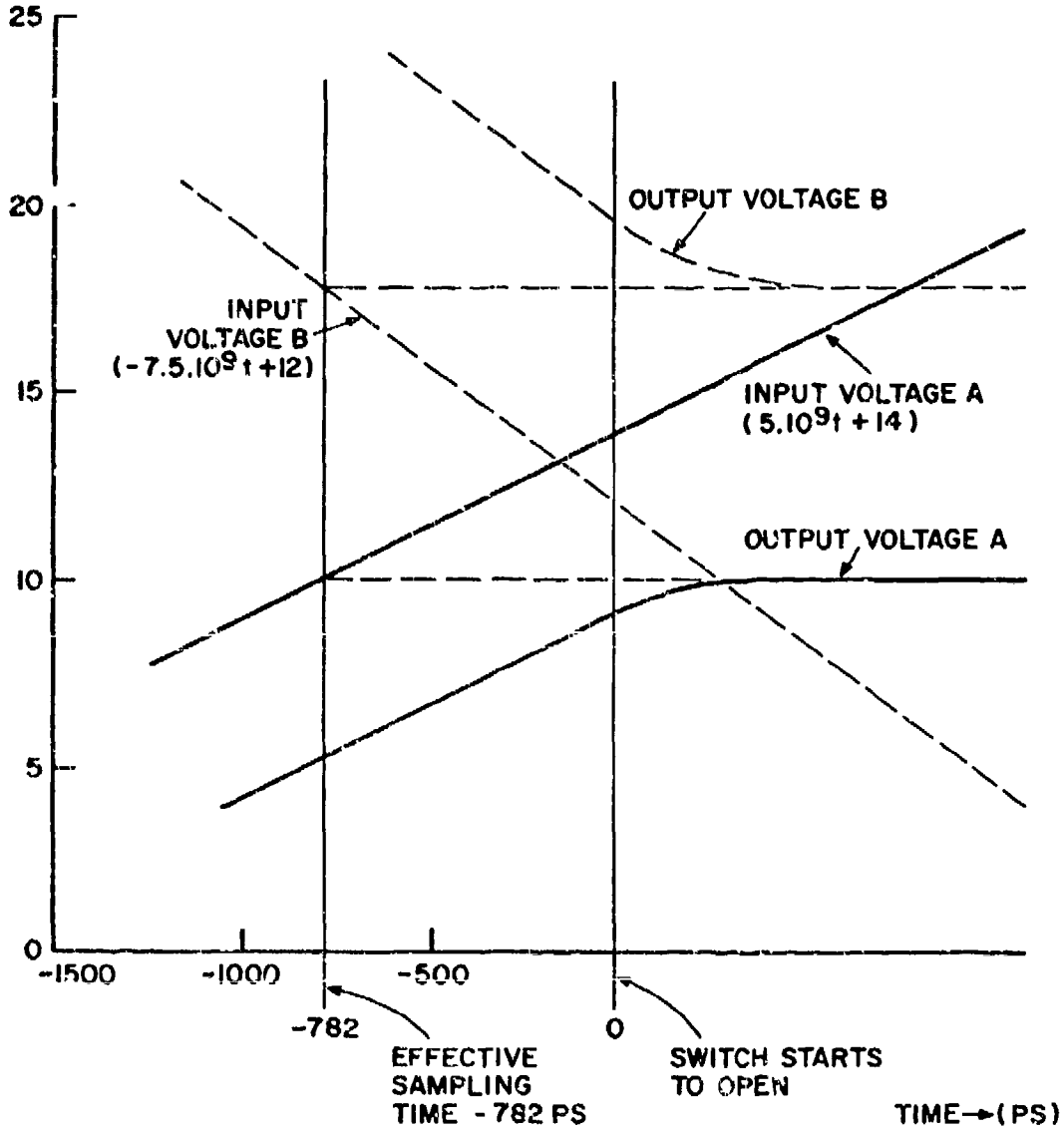

Figure 3. The switch paradox. Any switch which changes its resistance from low (closed) to high (open) in a finite time can be interpreted as an ideal switch which opens instantaneously. Shown are two ramp input voltages, A and B, charging a 50 pF holding capacitor through a switch with a time-dependent resistance $r=20\exp(t/2.10^{-10})$ for $t\geq 0$ and $r=20$ Ohm for $t<0$. The computed output voltages can be interpreted as the result of an ideal switch with zero resistance, opening instantaneously at $t=-782$ ps, well before the actual switch starts to open at $t=0$.

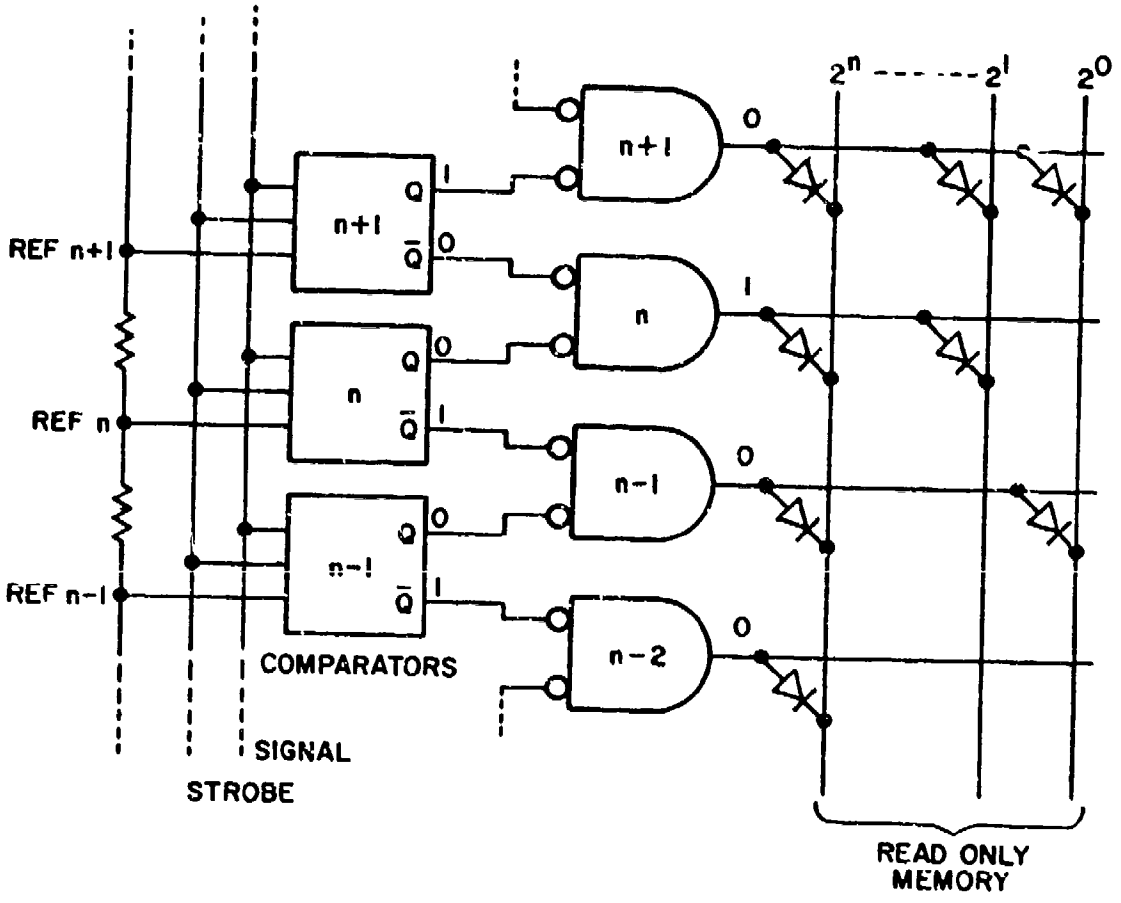

Figure 4. Section of VAROM, shown for a signal amplitude between reference n and n+1. The word selected from the read-only memory contains the output code corresponding to this amplitude.

1	1	1	1	1	1	1		1	0	0	1	1	1	1
1	1	1	1	1	1	0		1	0	0	1	1	1	0
1	1	1	1	1	0	1		1	0	0	1	1	0	1
1	1	1	1	1	0	0		1	0	0	1	1	0	0
1	1	1	1	0	1	1	becomes	1	0	0	1	0	1	1
1	1	1	1	0	1	0		1	0	0	1	0	1	0
1	1	1	1	0	0	1		1	0	0	1	0	0	1
1	1	1	1	0	0	0		1	0	0	1	0	0	0

Figure 5. The read-only memory can be modularized by using the same basic array, shown above at left, for every block of 8 comparators. To obtain the coding shown above at right, the module sense lines which correspond to the "zero" columns are left disconnected from the common sense line buses.

ADAPTIVE MOS/LSI MODEMS

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ABSTRACT

Six MOS/LSI chips almost entirely contain an adaptive half-duplex 4800/2400 bps modem plus a 110 bps modem. The two modems operate concurrently in opposite directions over a single dial-up channel. A non-MOS version has performed well over actual dial-up channels, and testing of the MOS version has started.

A higher-performance, full-duplex modem capable of operating over various types of channels at several bit rates up to nearly six times the channel bandwidth has been breadboarded and tested. Tentative plans are to implement this modem almost entirely on 7 or 8 MOS/LSI chips. The features include: (1) automatic, adaptive equalization, carrier recovery, timing and AGC that jointly and rapidly converge under extremely wide ranges of conditions and near-optimally combat the combined effects of both distortion and noise; (2) error correction that requires no digit redundancy and combats various disturbances; (3) jitter correction. Measured data showing the outstanding performance of this modem is presented herein.

Introduction

The following two high-speed data modems for voice-band channels (plus variations on these modems) have been developed at North American Rockwell, Inc.:

Modem 1, a 4800/2400 bps, 5 MOS/LSI Chip Modem for Dial-up Channels. The present model is half-duplex and the 5 MOS/LSI chips contain essentially all of the modem hardware except interface circuits and power supply. This modem is completely automatic and thoroughly adaptive. One additional MOS chip contains a 110 bps modem. The 4800 bps and 110 bps modems operate simultaneously in opposite directions on the same 2-wire dial-up circuit. This MOS modem has been undergoing successful field testing since December, 1971. In addition, a non-MOS version of this modem has been extensively tested, including quite successful tests over various dial-up channels over widely separated geographical regions. Full-duplex demonstration models of this 4800/2400 bps modem are presently being constructed. The MOS/LSI implementation offers a several-fold reduction in initial cost plus major reductions in maintenance, logistics, size, weight and power consumption.

Modem 2, A Higher-Performance Modem. Although Modem 1 provides relatively high performance, Modem 2 provides far higher performance by incorporating newer techniques.* Modem 2 has been breadboarded and thoroughly tested. Now, we are efficiently digitizing the hardware in preparation for implementing this modem in MOS/LSI. Thorough computer emulation in machine language is contributing heavily toward efficiency of digitization. We tentatively plan to implement this modem almost entirely on 7 or 8 MOS/LSI chips.

The present experimental model operates at 9600 or 4800 bps over leased telephone channels. Computer simulation indicates that data rates up to 19,200 bps on high quality voice-band channels and up to 9600 bps on dial-up channels can be provided while keeping the error rate sufficiently low for some applications. At bit rates up to 9600 bps on leased channels and up to 4800 bps on dial-up channels, the bit error rate can be kept quite low, as the measured curves presented below indicate.

A major advantage of the digital implementation is that, without substantially increasing the cost of the hardware, we can provide high flexibility including several data rates, versatile signal shaping to optimally shape the signal spectrum for different channel types, and provision for the insertion of various optional features. Most of this modem will also be used in 19.2 kilobit-per-second data transmission over VHF/UHF links.

This modem is not merely automatically equalized. It is completely automatic and thoroughly adapts to various combinations of channel characteristics and disturbances, including the intersymbol interference caused by severe amplitude distortion and delay distortion, Gaussian noise,

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*Some of these "newer" techniques have been under development and refinement for about five years.

carrier phase offset, and jitter of the carrier phase and timing. No data stream interruptions are required for learning purposes and completely hands-off operation is provided.

The remainder of this paper will emphasize Modem 2, because this modem will offer both outstanding performance and the major cost advantages of MOS/LSI. In any given type of circuitry, Modem 1 and Modem 2 require about the same quantity of hardware.

Implementation, Summary

The modem employs a special combination of partial response signal shaping and simple coding to simultaneously achieve several important advantages. The coding makes it feasible to use signals that overlap heavily in time (controlled intersymbol interference), thereby achieving high data rates for a given bandwidth with relatively few signal levels. The relatively small number of signal levels for a given data rate makes the system far more immune than conventional signaling schemes to Gaussian noise, impulse noise, phase jitter, and various other transmission disturbances than conventional signaling schemes. The coding requires no digit redundancy and no special synchronization. The detailed signal shaping in both transmitter and receiver has been carefully designed to jointly optimize the overall modem performance while minimizing the overall cost of implementation.

To a close approximation, the effective amplitude-frequency characteristic of the overall transmitter (when all effects are translated to baseband) is $A(\omega) = \sqrt{\sin T\omega \div c(\omega)}$ for $|\omega| \leq \frac{\pi}{T}$ and $A(\omega) = 0$ for $|\omega| > \frac{\pi}{T}$, where T is the time per symbol and $c(\omega)$ is the amplitude-frequency characteristic of a nominal channel. Excluding the equalizer, it has been found that pertinent optimization constraints require both the receiver and transmitter signal shaping characteristics to be the same. Thus, ideally, the overall system amplitude-frequency characteristic is $\sin T\omega$ for $|\omega| \leq \frac{\pi}{T}$. With sampling at the baud rate, the sequence of normalized amplitudes of samples of the ideal impulse response of the overall system is ... 0, 0, 0, 0, 1, 0, -1, 0, 0, 0, 0 ... .

Efficient utilization of bandwidth is obtained by achieving essentially pure single-sideband modulation. The separation of sidebands is facilitated by the method of signal shaping, which requires no d-c component in the baseband.

Figure 1 presents the transmitter. The present implementation is partly analog, but all of the circuitry to the left of the dashed line, except the timing oscillator, is presently being implemented digitally. A relatively versatile fast-processor type of implementation is being used for experimental refinements in real time. We plan to subsequently implement the entire transmitter, with the exception of timing circuitry and the circuitry to the right of the dashed line, on a single MOS chip. Another MOS chip will contain the timing circuitry for both the transmitter and the receiver.

MODEM TRANSMIT SECTION

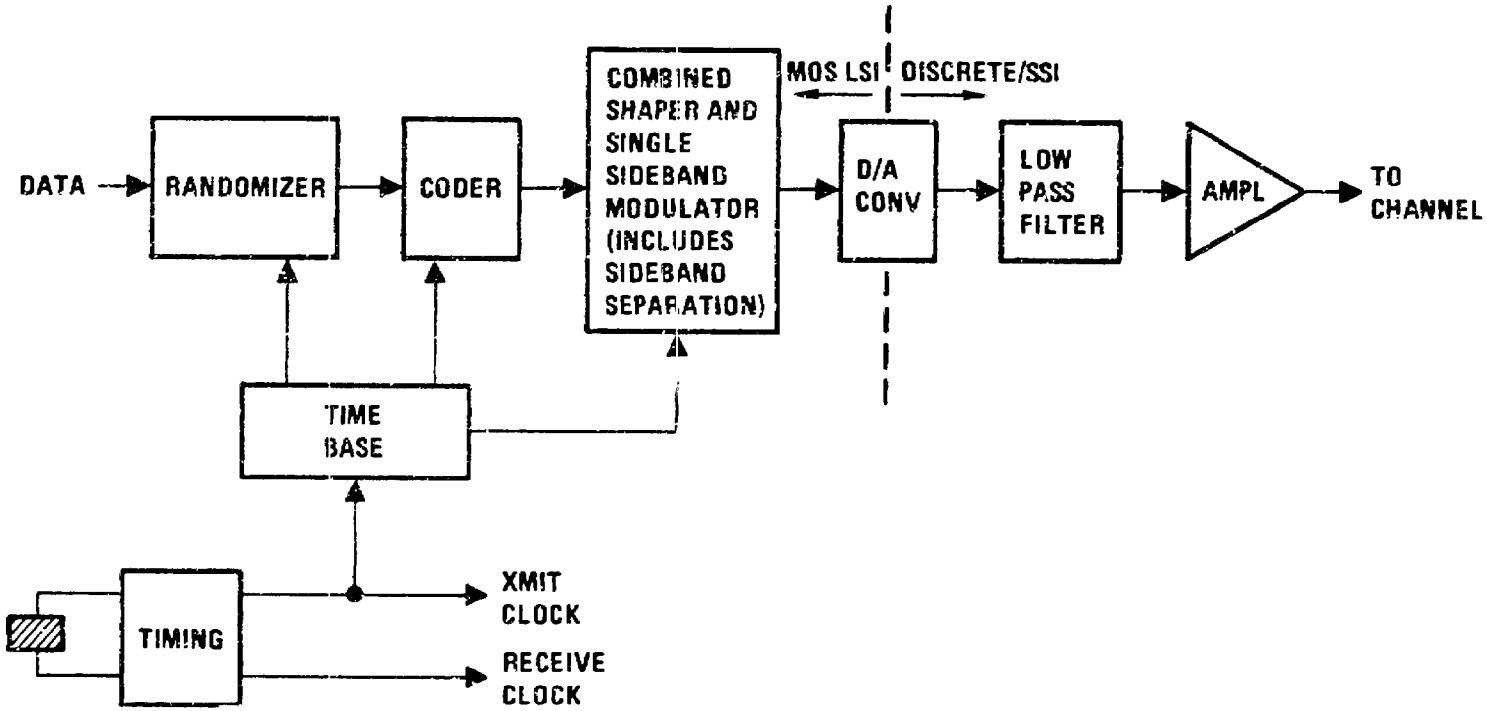

Figure 1. Transmit Section, Modem 2

The data enters level converters (not shown) and passes through a randomizer consisting of a 17-stage linear sequence generator assuring essentially zero auto-correlation in the data stream. This randomization aids the adaptive receiver. The coder allows the received data to be detected without reference to previous data, thereby preventing error propagation effects that would otherwise be caused by the controlled intersymbol interference (overlapping signal elements) used.

Actually, the coder, signal shaper, modulator and sideband separation are all combined and mainly consist of stored, sampled, quantized waveforms, which are read out of a read-only-memory (ROM) at 2 samples per symbol time and are multiplied by the data. At this point, the data is binary (± 1) at 4800 bps and quaternary (± 1, ± 3) at 9600 bps, as examples, on leased or dial-up telephone channels.

The completed digital signal is converted to analog form by the D/A converter. The D/A converter storage and switches are included in the MOS chip. The output low-pass filter, though by necessity analog, is quite inexpensive. This filter separates the desired signal spectrum (nominally 480 Hz to 2880 Hz) from aliasing spectra that result from the sampling.

The receive section of the modem is shown in Figure 2. Except for the simple input filter, AGC, and the thick film ladder network for the A/D converter, the receiver will consist of five (5) MOS chips. The input filter is identical with the transmit output filter. The AGC consists of a voltage variable resistor, an integrated operational amplifier, and other discrete components. After A/D conversion, the sampled signal is translated to baseband by multiplication with samples of a sinusoidal carrier. The baseband spectrum is separated from the upper sideband by the digital sideband filter. The baseband signal is then equalized by a transversal equalizer (1,2,3,4) in which the tap gains are automatically adjusted to minimize the combined effects of intersymbol interference and noise. Because of the controlled intersymbol interference mentioned earlier, the receiver makes 7-level decisions when 4-level data was transmitted, for example. The slicer makes threshold decisions and the decoder converts these decisions into data in the code that originally appeared at the transmitter input. The data is derandomized in the self-synchronizing derandomizer and converted to the appropriate output level.

The phase-locked loop (PLL) locks to the carrier. The carrier is phase shifted to correct for phase offset of the carrier relative to the ideal carrier phase, which offset is caused by delay distortion on the channel. The phase offset corrector and timing error are precisely controlled by logic operating from tap-gain information from the equalizer.

On initialization of operation, before the equalizer tap gains have converged, coarse phase offset and timing error information is derived from a preamble transmitted for that purpose. Then, equalization is obtained using a signal equivalent to the regular pseudo-random data signal in the 2-level partial response signaling mode. Overall receiver learning is achieved in a fixed time interval, which is now being reduced to approximately 200 milliseconds. Then, the modem automatically switches to the regular data transmission mode.

MODEM RECEIVE SECTION

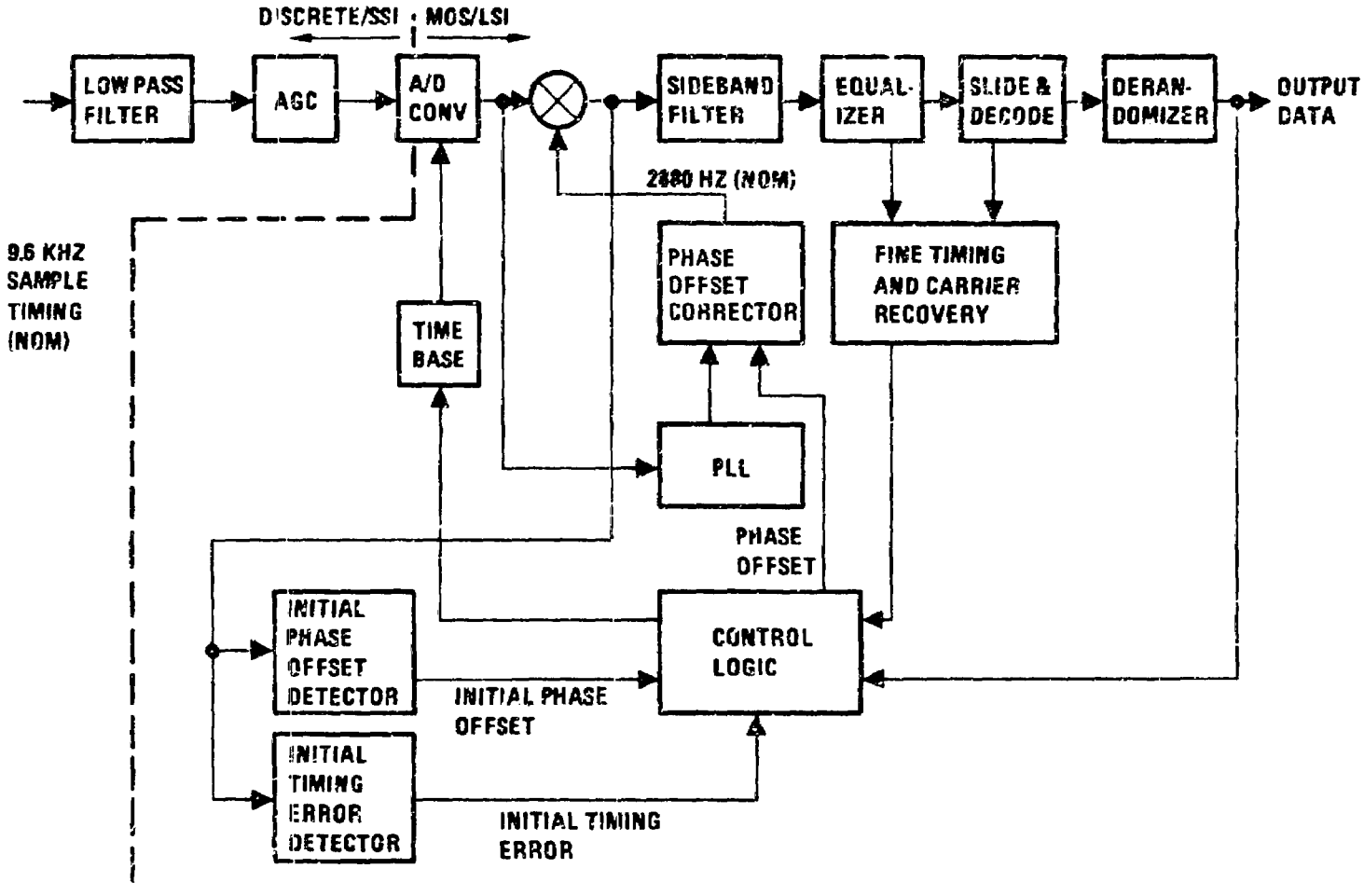

Figure 2. Receive Section, Modem 2

Automatic, Adaptive Equalization, Carrier Recovery and Timing Recovery

The equalizer is an automated, digitized transversal equalizer[1,2,3,4]. The automatic equalizer adjustments are, in effect, controlled by cross-correlation functions to achieve the following objectives:

a. Convergence of the automatic adjustment process under extremely wide ranges of conditions.

b. Near optimum minimization of the combined intersymbol interference and noise.

The following is believed to be the first practical automatic equalizer adjustment algorithm to accomplish these two objectives.

In z-transform notation, with sampling at the symbol rate,

$$\ell(z) = g(z)\, h(z), \quad z = e^{sT} \tag{1}$$

where $h(z)$ and $\ell(z)$ represent the sampled, impulse response of the transmission system as seen at the equalizer input and output, respectively, and $g(z)$ is the sampled transfer function of the equalizer. The equalizer adjustment criterion is as follows:

Once each baud time, increment each tap-gain, g_k, in the direction that drives the cross-correlation function

$$C_k = \sum_{j=-\infty}^{\infty} e_j h_{j-k} \tag{2}$$

toward zero, where h_{j-k} is the $(j-k)^{th}$ sample of the transmission system's impulse response as seen at the input of the transversal equalizer, and e_j is the error in the jth sample ℓ_j of the system impulse response as seen at the output of the equalizer; i.e., e_j is the jth undesired intersymbol interference term.

By straightforward implementation, each cross-correlation Eq. (2) would require an infinite number of multiplications and 30 such cross-correlations would be required for a 30-tap equalizer, for example. However, our iterative, time-shared implementation is quite inexpensive.

The overall combination of carrier recovery, timing recovery and equalization initially converges automatically, even under severe channel distortion (such as that encountered on dial-up channels), compounded by phase jitter and by any initial errors in timing and carrier phase. Furthermore, the equalization, timing and carrier phase all rapidly converge to jointly optimized values and track these values with high precision and stability. Neither non-data signals nor data stream interruptions are required in order to achieve this continuous, optimized adaptation.

Optional Error Detection and Correction without Digit Redundancy

Error detection and correction that requires no digit redundancy other than that inherent in the selected method of signaling has been implemented and tested. This error corrector is quite effective against various types of transmission disturbances. Measured results are presented below. In those applications where any conventional method of error correction would require an increase in the number of signal levels in order to achieve a given information rate, this new method of error correction is especially advantageous. This method does not require any increase in either the number of signal levels or the symbol rate.

Performance of Modem 2

Modem 2 has been thoroughly tested in the laboratory under various combinations of channel characteristics and disturbances, as well as on real channels. Figure 3 depicts representative results under Gaussian noise. This data was taken on a simulated channel with distortion slightly worse than a worst-case Type C-2 telephone channel.

Note that at 9600 bps (and on channels that do not introduce significant phase jitter) the bit error rate is exceedingly low at signal-to-noise ratios above the specified minimum of 26 db for Type C2 channels. Even without the error corrector, the performance is outstanding. A relatively simple version of the error corrector eliminates 95 to 99.5% of errors, depending upon conditions, without reducing the useful data rate. A more sophisticated version can reduce the bit error rate by several orders of magnitude under some conditions without reducing the useful data rate.

Figure 4 presents the performance at 9600 bps under phase jitter of 15° peak-to-peak at 60 hertz, which is approximately the worst phase jitter encountered on leased telephone channels. For reference purposes, two curves for the case of no phase jitter are repeated from Figure 3. With no corrector, the performance under this phase jitter at the specified minimum S/N for Type C2 channels is marginal for some applications. Our error corrector that requires no digit redundancy improves the performance substantially under phase jitter. The combined error corrector and jitter corrector improves the performance further.

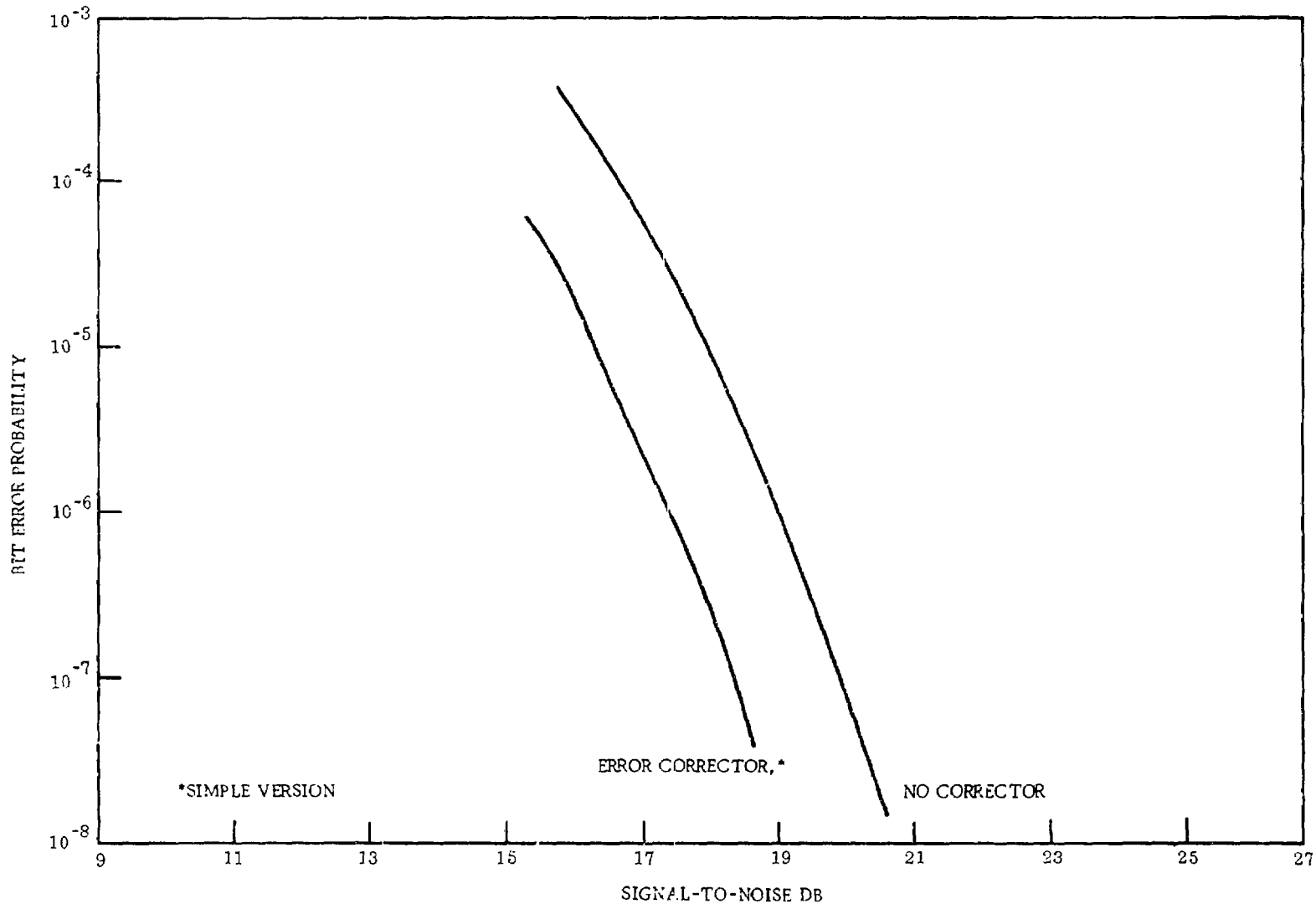

Figure 3. Modem 2 Performance on Worst-Case C-2 Channel (No Jitter), 9600 bps

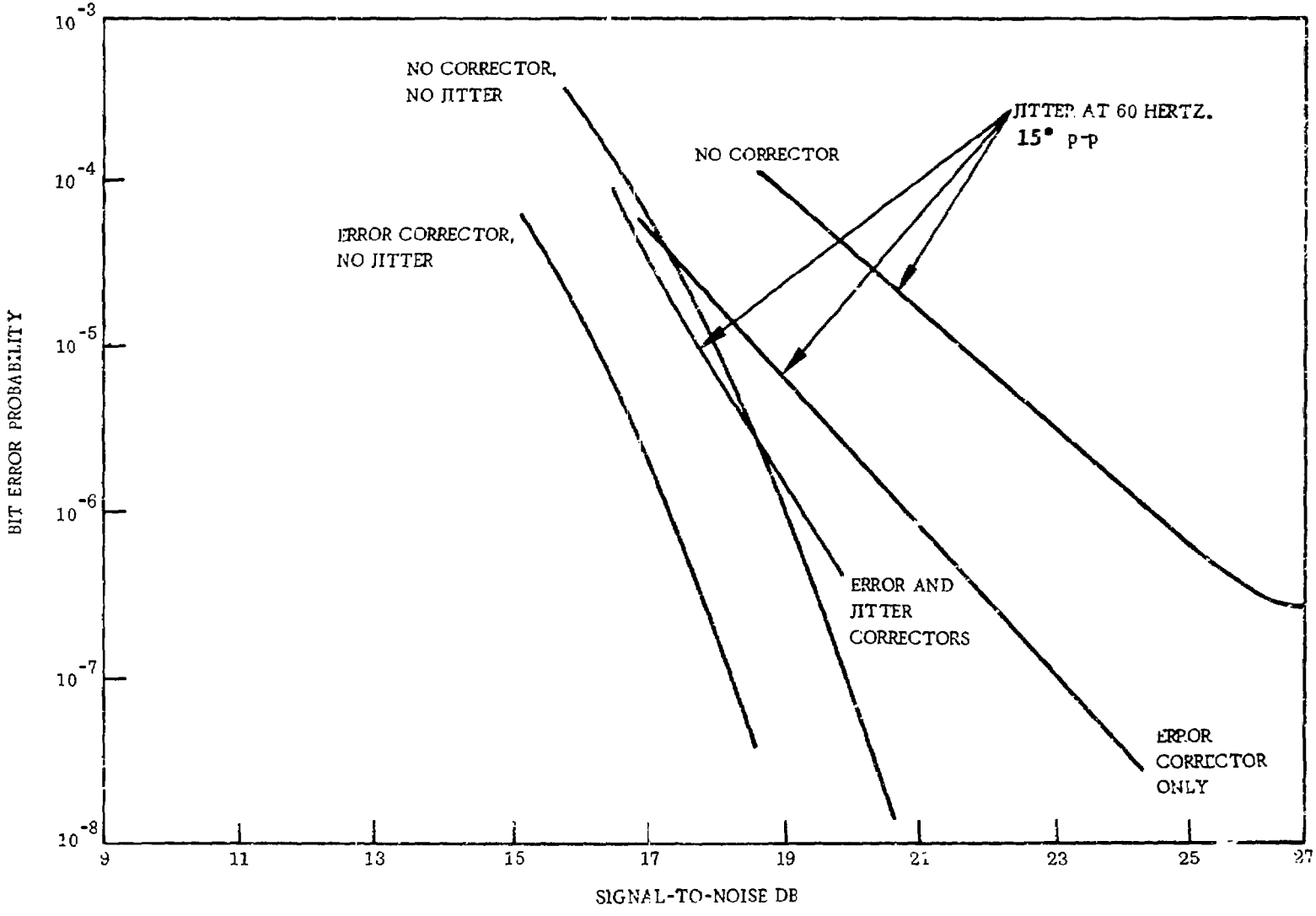

Figure 4. Performance on Worst-Case C-2 Channel (Jitter), 9600 bps

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(1) Gibson, E. D., "A Highly Adaptive 9600/4800 bps Data Modem for Voice-Band Telephone Channels", Conference Record, 1970 IEEE International Conference on Communication, p. 12-1.

(2) --- "A Intersymbol Adjustment Method of Distortion Compensation", Proceedings of MIL-E-CON, pp. 196-207, 1961.

(3) --- "Automatic Equalization Using Time-Domain Equalizers", ACF Industries Report ACFE-880275-88, August 1960. Summarized in Proceedings of the IEEE, Correspondence, August 1965, p. 1140.

(4) --- U. S. Patents:

(a) No. 3,274,582 "Interdigit Interference Corrector", filed August 25, 1961, granted Sept. 20, 1966.

(b) No. 3,184,544 "Noise and Distortion Reduction in Communication Systems", filed Oct. 12, 1961, granted May 18, 1965.

A GENERAL PURPOSE COMPUTER FOR SATELLITE APPLICATIONS

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ABSTRACT

A computer intended for use as a spaceborne real time controller has been designed at the Johns Hopkins University Applied Physics Laboratory and will be utilized in a Navy Navigation Satellite.

Introduction

The computer reviewed in this digest is the third generation digital system for the Navy Navigation Satellites. The first generation system was first launched in 1962 and consisted of core diode circuitry used to perform logic and drive a 50 mil core memory array. The second generation system was first launched in 1966 and consisted of a special-purpose processor designed with series 51 RCTL and a 30 mil core memory array driven with hybrid circuits.

Purpose

Figure 1 shows the computer relation to other satellite systems. The RF data link to the computer is via the ten bit per second and thousand bit per second bit detectors. Each bit detector input is three line serial and consists of an interrupt line, clock line, and data line. Proceeding clockwise on Figure 1, the computer output to the command logics are also three line serial. Six lines from the disturbance compensation system, DISCOS, give the computer the six micro-thruster valve on-off waveforms for partial data reduction, formatting and storage. DISCOS contains a ball centered in sphere servo system and is designed to compensate for air drag and solar pressure. The computer provides timing and direct delayed on-off commands to the Pseudo Random Noise Generator, PRN. The computer outputs data to the transmitters either as 50 bits per second Navy navigation message, NAVSAT, or 325 bits per second telemetry, TM. The computer interface with the real time TM system consists of a nine bit TM commutator address or TM data bus, a serial computer to TM data channel, and four interrupts; status request, dump request, TM data ready, and frame synchronization. A 5 megahertz stable oscillator output is used to generate the computer clock, either directly or via an incremental phase shifter, IPS. The purpose of IPS is to provide more accurate satellite timing. The computer provides programmed up or down counts to a counter in IPS to regulate the phase shift rate.

Energy Conservation

Most of the computer is pulse powered and shuts down when not in use. When an interrupt is recognized the computer enters the continuous computing mode. In this mode the computer using core memory for both program and data storage executes 250,000 instructions per second at a power level of 62 watts. Sufficient energy is stored on capacitors for two milliseconds of continuous operation. Interrupts may be internally initiated under program control via output instructions. These internal interrupts serve as low overhead entry to background computation.

The computer has four background computing rates which may be selected under program control by two bits in a status register. Using core memory for both program and data storage the power consumption for the four background computing rates are as follows:

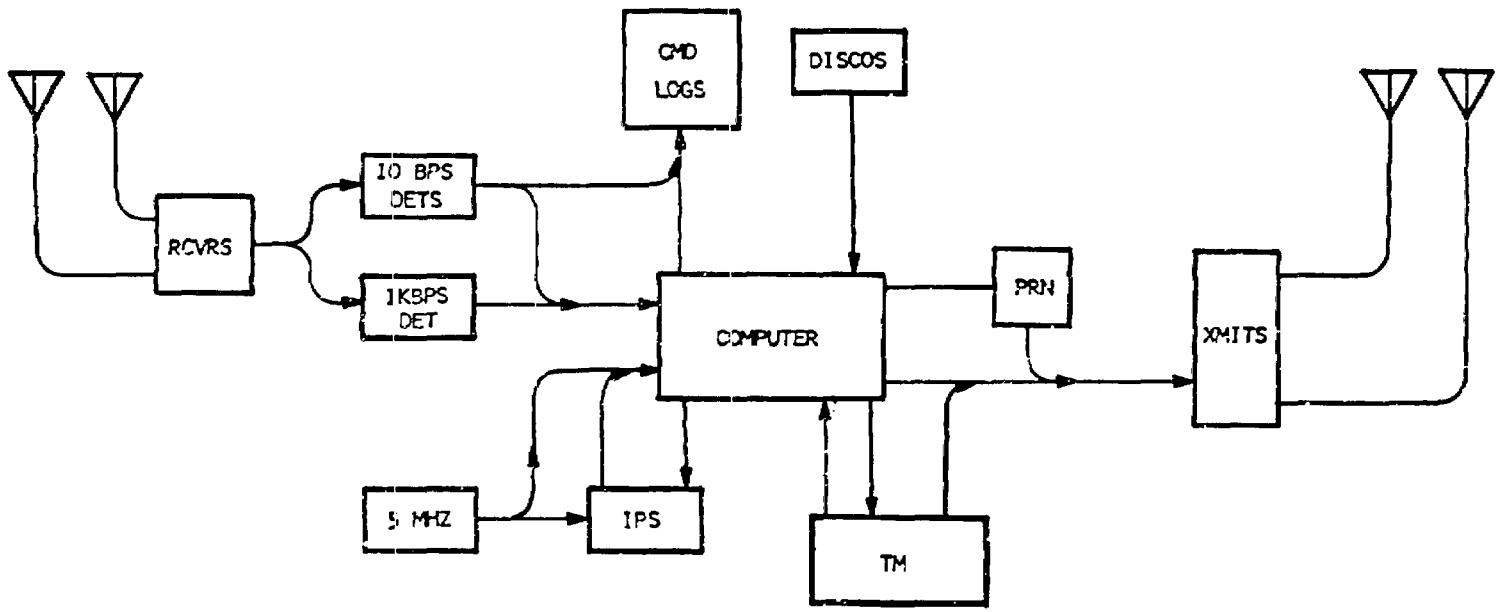

FIGURE 1 COMPUTER RELATION TO OTHER SATELLITE SYSTEMS

TABLE 1. COMPUTING CAPABILITY VERSUS CONFIGURATION

ENERGY/INSTRUCTION	INTERRUPT RATE	INSTR/INTR at 1W	CONFIGURATION
200 μJ	50 per sec.	100	3D Core & Std. TTL CPU
50 μJ	50 per sec.	400	2-1/2D Core & Std. TTL CPU
20 μJ	50 per sec.	1,000	Plated Wire & LP TTL CPU

Instructions/SEC	POWER
2,000	1.5 watts
4,000	2.0 watts
8,000	3.0 watts
16,000	5.0 watts

The satellite power system is capable of continuously powering the computer operating in the background mode.

Table 1 summarizes the decrease in energy required to execute an instruction that can now be achieved with two other possible configurations. The present configuration which utilizes a 3 wire 3D 20 mil core memory and standard power circuits in the processor requires from the computer power processor 200 microjoules per instruction. Giving this a more useful interpretation for a small satellite, the computer can process at a one watt average power level, an average of fifty interrupts per second with an average of one hundred instructions per interrupt. Replacing the original core memory with a 2-1/2D 18 mil low drive core memory can yield a four-to-one improvement over the original design. Replacing the original core memory with plated wire memory and repackaging the processor utilizing all low power TTL can yield a ten-to-one improvement over the original design.

Computer Organization

Figure 2 shows the computer organization. The interface with the other satellite systems through the input-output logic is depicted in the upper left with the SAT to IO interface. Below the IO interface is shown the Read Only Memory which contains the bootstrap loader program, the Read Write Memory used for data storage and other programs, and the priority interrupt logic. The sixteen-bit parallel two-function operator logic, OPR, is shown in the upper right corner. The output of the operator, the Z Bus, inputs to the arithmetic registers. First is shown the status register, U, which contains the carry, overflow, and input-output flags, the power mode control bits, and eight interrupt masks. Next is the accumulator, A, and the index register, X. The real time clock register, T, consists of a sixteen-bit binary counter and a sixteen-bit synchronizing latch. Negative overflow of the counter causes the real time clock interrupt. Operations that are performed with the A register can also be performed with the T register. The program address register, P, the memory address register, W, and the main exchange register, D, comprise the remainder of the arithmetic registers. The control portion of the computer shown in the center of the diagram consists of an associative Read Only Memory addressed by the state register, R, iteration counter, N, instruction register, I, and the Z bus. The microinstructions, MICROS, control the data flow paths.

Table 2 lists the major considerations used to determine the machine architecture. Of these considerations, the attainment of item 2 proves the efficiency of utilizing a general-purpose computer over utilizing a special-purpose processor and memory. To satisfy the Navigation Satellite data storage and formatting requirements, NAVSAT, a special purpose

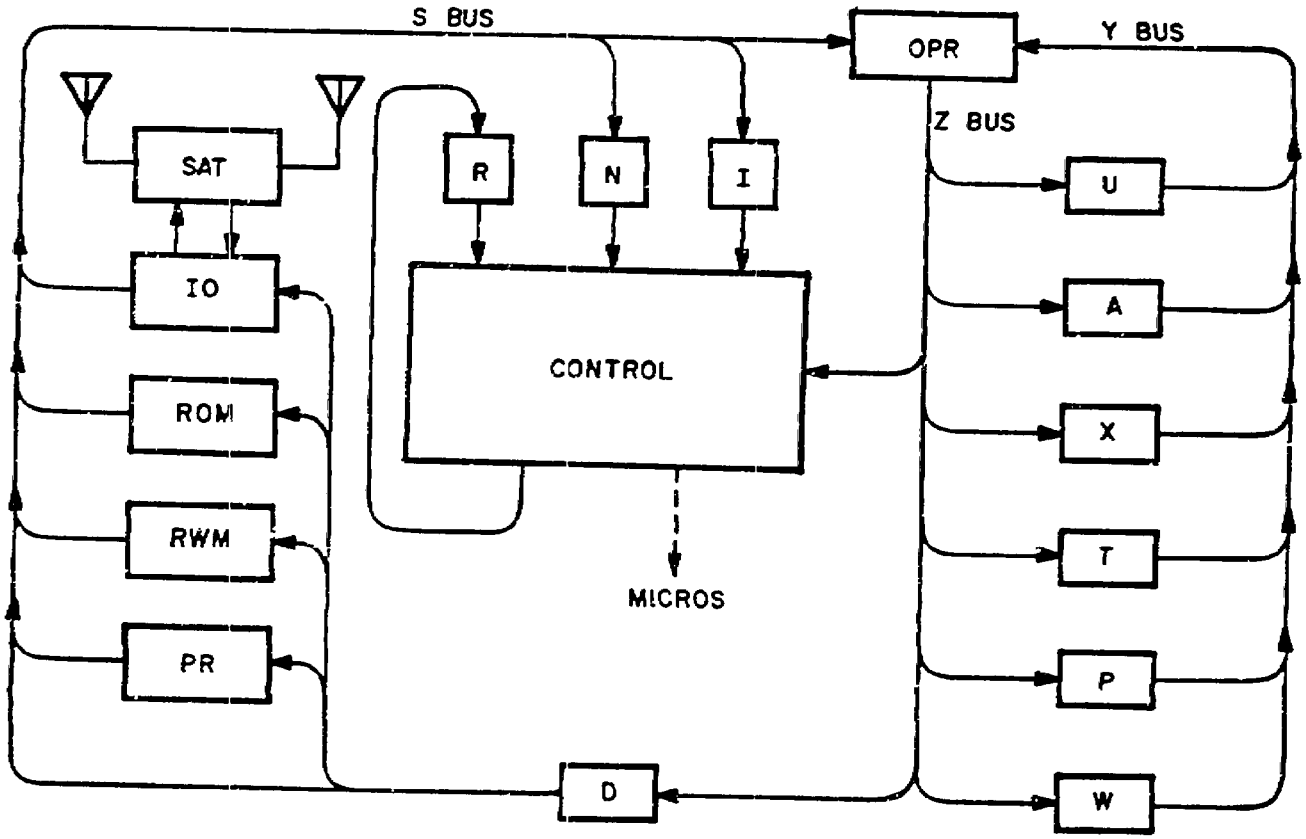

FIGURE 2 COMPUTER ORGANIZATION

TABLE 2. ON DETERMINING MACHINE ARCHITECTURE

1. Low overhead for entry into and exit from short data formating tasks.

2. High program storage efficiency comparable to data storage requirements. NAVSAT min = 25K.

3. Fast reaction time to interrupts to eliminate extensive I-O buffering, but capable of extended background computing on available power.

4. NAVSAT output formating primary original task and used as benchmark test for instruction repertoire.

5. NAVSAT major design goal dictates that the power be kept off most of the computer when not performing a task.

TABLE 3. INSTRUCTION SUMMARY: PART 1

STORAGE REF; 11 10 9 = I X R

Transfer				
TSA	00	(S)→A	IF U16 = 1	
TAS	01	(A)→S	TSD	(S,S+1)→AX
IAS	04	(A)⇄(S)	TDS	(AX)→S,S+1
TSX	10	(S)→X	IDS	(AX)⇄(S,S+1)
TXS	17	(X)→S		
TST	11	(S)→T		
TTS	12	(T)→S		
TSU	16	(S)→U		
TUS	07	(U)→S		
Arith			IF U16 = 1	
ASA	02	(A)+(S)→A, C, OV	ASD	
SSA	03	(A)−(S)→A, C, OV	SSD	
MLT	24	(A)X(S)→A, X		
AST	36	(T)+(S)−2→T, C, OV		
Logic				
NSA	13	(A) AND (S)→A		
MSA	14	(A) OR (S)→A		
ESA	15	(A) EXOR (S)→A		
Control				
JMP	21	(P)=S		
SJP	22	(P)→S, (P)=S+1		
IRN	23	(S)+1→S, C, OV; SKP (S)≠0		
IRS	06	(S)+1→S, C, OV; SKP (S)=0		
CAS	05	SKP 1 (A)=(S), SKP 2 (A)<(S)		
CTS	37	SKP 1 (T)−1 = (S), SKP 2 (T)−1<(S)		
DOS	20	(S) I/O→N		

IMMEDIATE

TIA	260	I→A
TIX	261	I→X
AIA	262	(A)+I→A, C, OV
AIT	263	(T)+I−2→T, C, OV
AIX	264	(X)+I→X, C, OV; SKP X=0
AIN	265	(X)+I→X, C, OV; SKP X=I
CAI	266	SKP 1 (A) = −I, SKP 2 (A)<−I
CTI	267	SKP 1 (T)−1 = −I, SKP 2 (T)−1<−I
NIM	270	I AND (M)→M
MIM	271	I OR (M)→M
EIM	272	I EXOR (M)→M
NIF	273	I AND (F)→F
MIF	274	I OR (F)→F
EIF	275	I EXOR (F)→F
TIM	276	I→M
TIF	277	I→F

INPUT-OUTPUT, IOF

TDS	Transfer Data Serial	33
TDE	Transfer Data External	34
TEA	Input Load A	164
MEA	Input OR to A	165
SKZ	Sense, Skip if 0	166
SK1	Sense, Skip if not 0	167

BRANCH	IF	
BAZ	A = 0	620
BA1	A ≠ 0	600
BAP	A pos	601
BAN	A neg	621
BAE	A even	602
BAO	A odd	622
BEZ	A16 ≠ A15	613
BE1	A16 = A15	633
BXP	X pos	605
BXN	X neg	625
BXZ	X = 0	626
BX1	X ≠ 0	606
BXE	X even	607
BXO	X odd	627
BOZ	Ov, U15, cl	603
BO1	Ov, U15, set	623
BCZ	Cry, U14, cl	604
BC1	Cry, U14, set	624
BF1	IOF, U13, set	630
BFZ	IOF, U13, cl	610
BJ1	J, U10, set	631
BJZ	U, U10, cl	611
BQ1	Q, U9, set	632
BQZ	Q, U9, cl	612
B1Z	SW1, cl	614
B11	SW1, set	634
B2Z	SW2, cl	615
B21	SW2, set	635
B3Z	SW3, cl	616
B31	SW3, set	636
B4Z	SW4, cl	617
B41	SW4, set	637

SHIFT, C, OV

ALR	A left Rot	3222
XLR	X left Rot	3212
ARR	A right Rot	3262
XRR	X right Rot	3252
ALS	A left shift	3220
XLS	X left shift	3210
ARS	A right shift	3260
XRS	X right shift	3250
ARA	A right arith	3261
XRA	X right arith	3251
LLR	Long left Rot	3234
LRR	Long right Rot	3274
LLS	Long left shift	3230
LRS	Long right shift	3270
LRA	Long right arith	3271
DLY	Delay	3200

processor of complexity nearly equal to a general purpose computer processor would be required and would not provide for programmable stored telemetry and delayed commands.

Instructions

Table 3 is a partial summary of the computer instruction set. Not included are 105 interregister instructions. The memory reference instruction format contains three address modifier bits which designate relative, indirect, and indexed addressing. All three address modifiers may be utilized in a single memory reference instruction. The conditional branch instructions are relative with a seven bit displacement field.

The extensive instruction repertoire is partially the result of apriori component selection. The relative balance of arithmetic, control, input-output and memory hardware indicated that an extensive instruction set may be incorporated without significantly expanding computer hardware. Were it ever planned to package the processor on a few LSI chips constraints on the LSI processor instructions would be necessary.

Memories

The memories used with the processor to complete the first satellite computer design consist of one 4K word x 16 bit core memory for modifiable program and data storage and one 64 word x 16 bit TTL read-only memory for the RF link bootstrap loader program. The core memory consists of 64 hybrid circuits designed around an EMI SM20 3D, 3 wire 20 mil lithium wide temperature core stack. These circuits consist of 16 X-Y axis complementary current switches, 16 X-Y axis complementary voltage switches, 16 dual digit regulated voltage switches, and 16 sense amplifier dual comparator threshold networks. The read-only memory utilizes the Harris field programmable fusable link TTL IC's. Both memories are designed for complete power shutdown when not being accessed. Table 4 lists the memories considered for the first flight computer.

Choice of Microcircuits

The choice of TTL for the computer was at the time necessitated by the consideration of environmental degradations. The proven low random failure probability of TTL also weighed heavily in favor of choosing TTL. Table 5 lists the combinations of components considered for the processor logic. The fourth option was adopted as the best compromise of low component count and low gated power consumption. Table 6 lists logic components ruled out early in the original decision making process. It should be kept in mind that these decisions reflect the status of microcircuit logic elements available in mid-1969.

TABLE 4. MEMORY OPTIONS FOR FIRST CONFIGURATION

RANDOM ACCESS MEMORIES

A. Plated Wire
   1. Low power
   2. Low weight and volume in development
   3. High potential reliability

B. Core (20 mil)
   1. Low cost
   2. Acceptable power weight and volume
   3. High proven reliability.

READ-ONLY MEMORIES

1. TTL custom film.
2. Field programmable fusible link diode arrays.
3. Field programmable fusible link TTL.

TABLE 5. COMPONENTS CONSIDERED FOR PROCESSOR LOGIC

1. Five basic TTL IC's that were available as high power dielectrically isolated semiconductor, thin film resistor circuits.
2. Five basic lower power TTL circuits that showed potential for becoming available as dielectrically isolated semiconductor, thin film resistor circuits.
3. All available low power TTL circuits including the MSI low power 4 bit register section.
4. All available low power and standard power TTL circuits including the standard power MSI 4 bit address, 1 of 8 and 1 of 16 decoders, and 8 input multiplexers.

TABLE 6. COMPONENTS RULED OUT EARLY

1. MOS low power circuits, MOS MSI circuits, and custom designed MOS LSI arrays.
2. Custom designed low power dielectrically isolated semiconductor thin film resistor arrays.
3. Core diode logic
4. Hybrid semiconductor logic.

Packaging

Figures 3 and 4 show two views of the prototype flight computer logic. The right hand card on the open view Figure 3 contains the processor control. The connector in the upper right corner is used for preliminary test monitor and display. The next card contains the arithmetic logic. The combined control and arithmetic logic form the central processor. All of the processor control card is fabricated with medium power TTL. The entire processor control card is pulse powered and shuts down when not in use. The registers on the arithmetic card are fabricated with low power TTL and may stay powered during energy recharge periods when background computing is in process, on shut down with the arithmetic logic and the control board logic during energy recharge periods when background computing is not in process. The remaining two cards contain peripheral logic consisting of the bit detectors input buffer and overflow counter, delayed command format error detection circuits, transmitter modulation encoder, TM input output buffers, and priority interrupt buffers. The Read Only Memory, S bus multiplexer, and connectors for the core memory and satellite systems are also on the peripheral cards.

The construction method consists of point-to-point welded wire on feedthrough pins for signals and laminated planes with access holes for power and ground. Microcircuits are parallel gap welded to the top of the board as a final step in board fabrication. The four processor and peripheral logic boards bolted into a magnesium casting weigh two pounds. The core memory which consists of two boards and the core stack bolted into another magnesium casting weighs two and one-half pounds. The two castings clam-shelled together in the satellite occupy 200 cubic inches. The power processor which consists of current limiters, energy storage capacitors, and gated voltage regulators weighs two pounds and occupies 50 cubic inches.

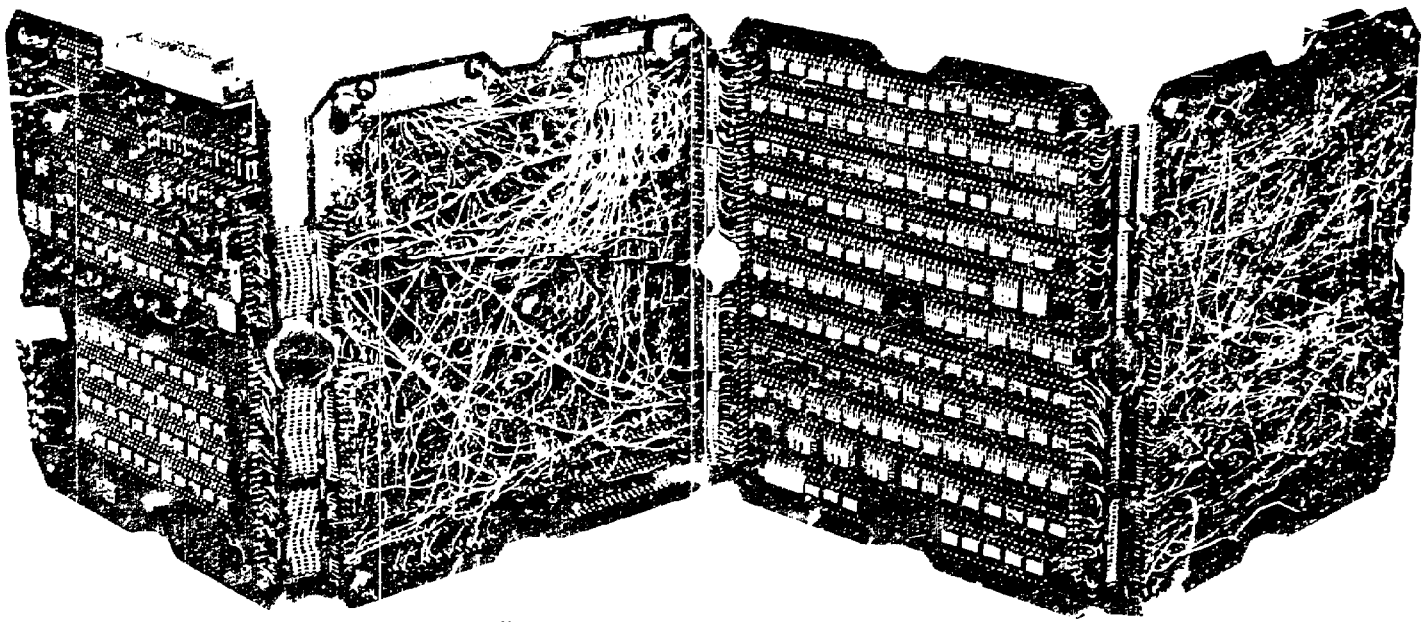

Figure 3. LOGIC BOARDS -- OPEN VIEW

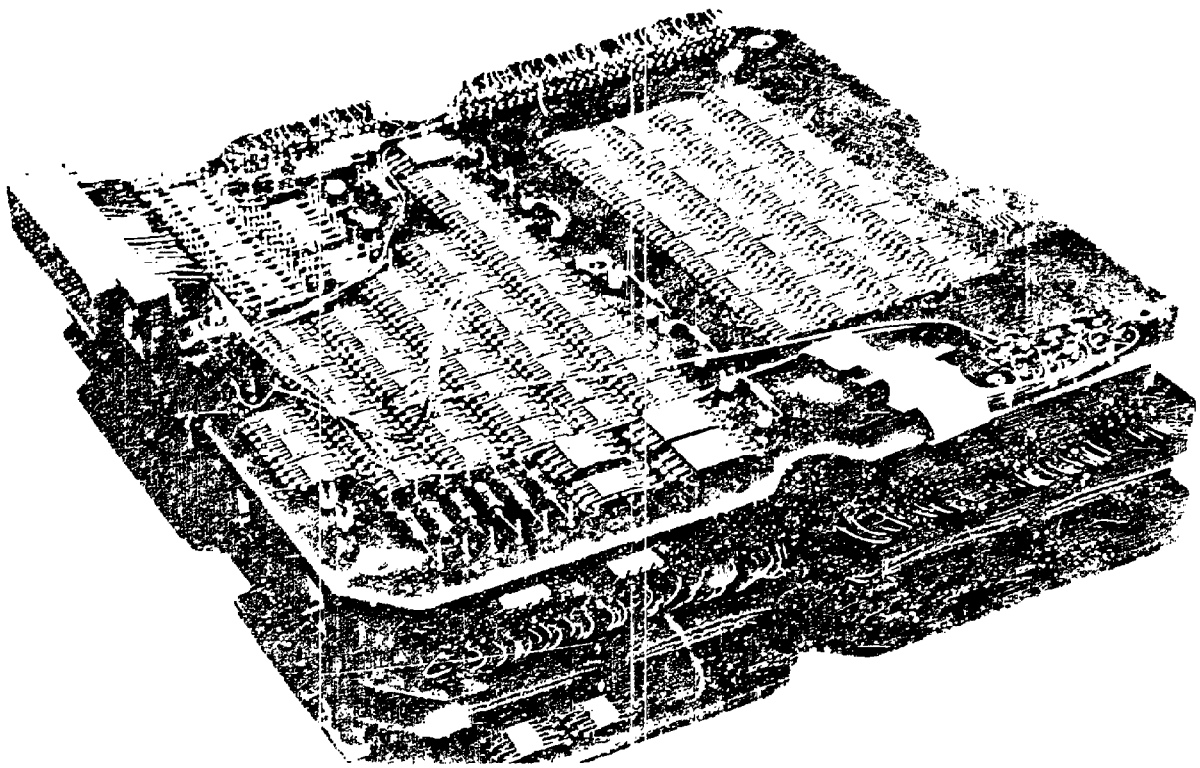

Figure 4. LOGIC BOARD -- FOLDED VIEW

A TORPEDO SYSTEM DIRECTOR: LOGPRO#3

J. E. Brewer

Westinghouse Electric Corporation

An economical digital processor, LOGPRO#3, has been developed to serve as the system director for underwater vehicles such as torpedoes and mobile acoustic targets. LOGPRO's architecture and special instruction set allow efficient use of instruction memory.

INTRODUCTION

LOGPRO#3 (LOGic PROcessor) was developed to serve as the controller for a torpedo research vehicle. Its purpose was to explore the feasibility of software oriented tactical and control routines in advanced torpedo systems, and to aid in the definition of the systems architecture for future weapons. This paper describes the LOGPRO#3 prototype machine.

PHYSICAL CHARACTERISTICS

As shown in figure 1, two wire wrap boards form the LOGPRO#3 machine. The boards are approximately 16 x 8 inches in area and 5 pounds in weight. The logic and IO circuitry was implemented using Fairchild 9300 Series TTL, and appears on the lower board in figure 1. The upper board contains a 3,072-word by 16-bit random access instruction memory. The primary memory component was the Intel 1101 chip. This prototype was constructed for flexibility in experimentation. All of the integrated circuits used are available off the shelf from multiple vendors.

In general, machines of the LOGPRO class were not meant to be stand alone processors. Physically and electrically this processor should be integrated into the electronics of the torpedo. The LOGPRO circuits can be partitioned onto cards similar to those used throughout the torpedo, and can share the same power sources.

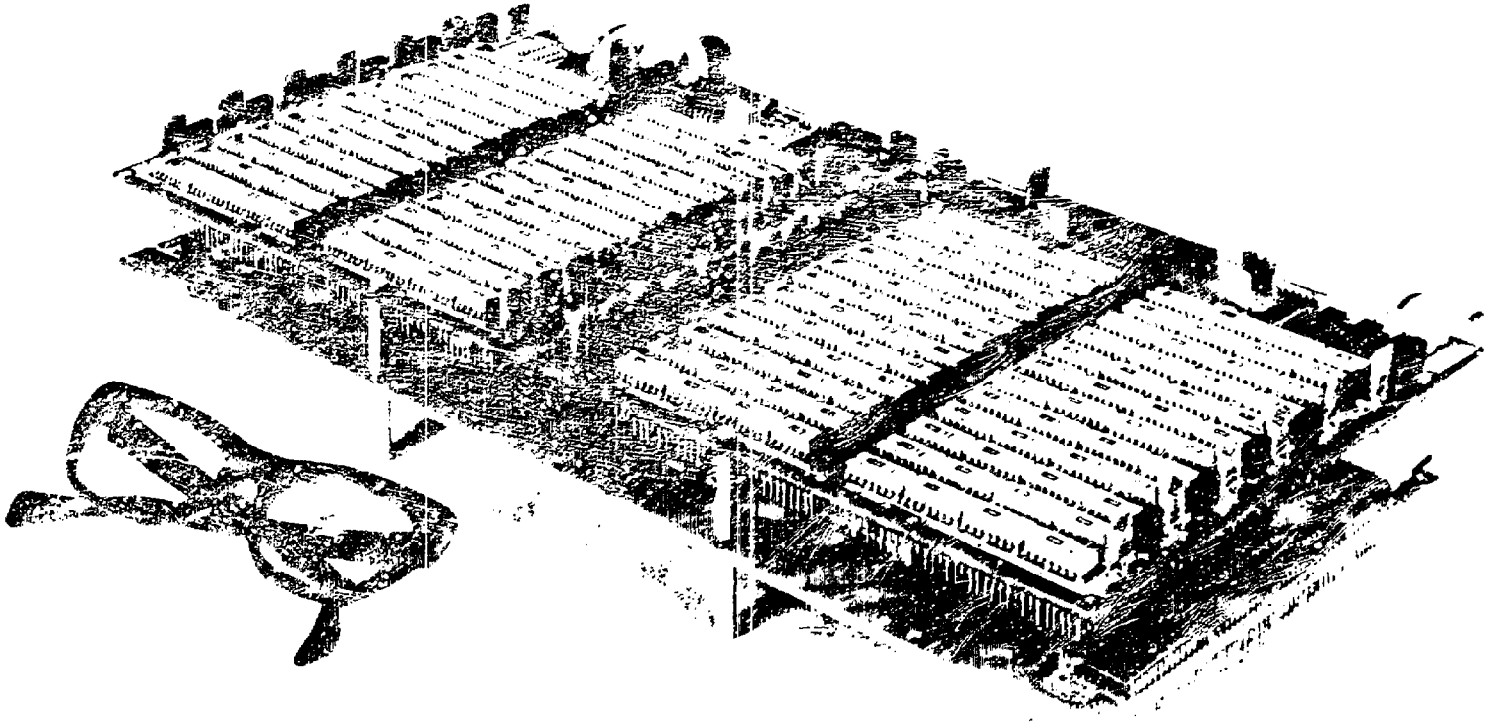

FIGURE 1: The LOGPRO#3 prototype configuration

The block diagram presented in figure 2 outlines the internal organization of LOGPRO#3. Instruction memory is used to store the program or torpedo operating algorithm. Memory is the largest hardware cost associated with LOGPRO, and efficient use of instruction memory was a major design goal.

During a torpedo run, the instruction memory operates in a read-only mode. In a production system this memory would be partially or entirely implemented in some form of read-only memory (ROM). In the LOGPRO#3 prototype, a read-write system was employed to allow experimentation with software.

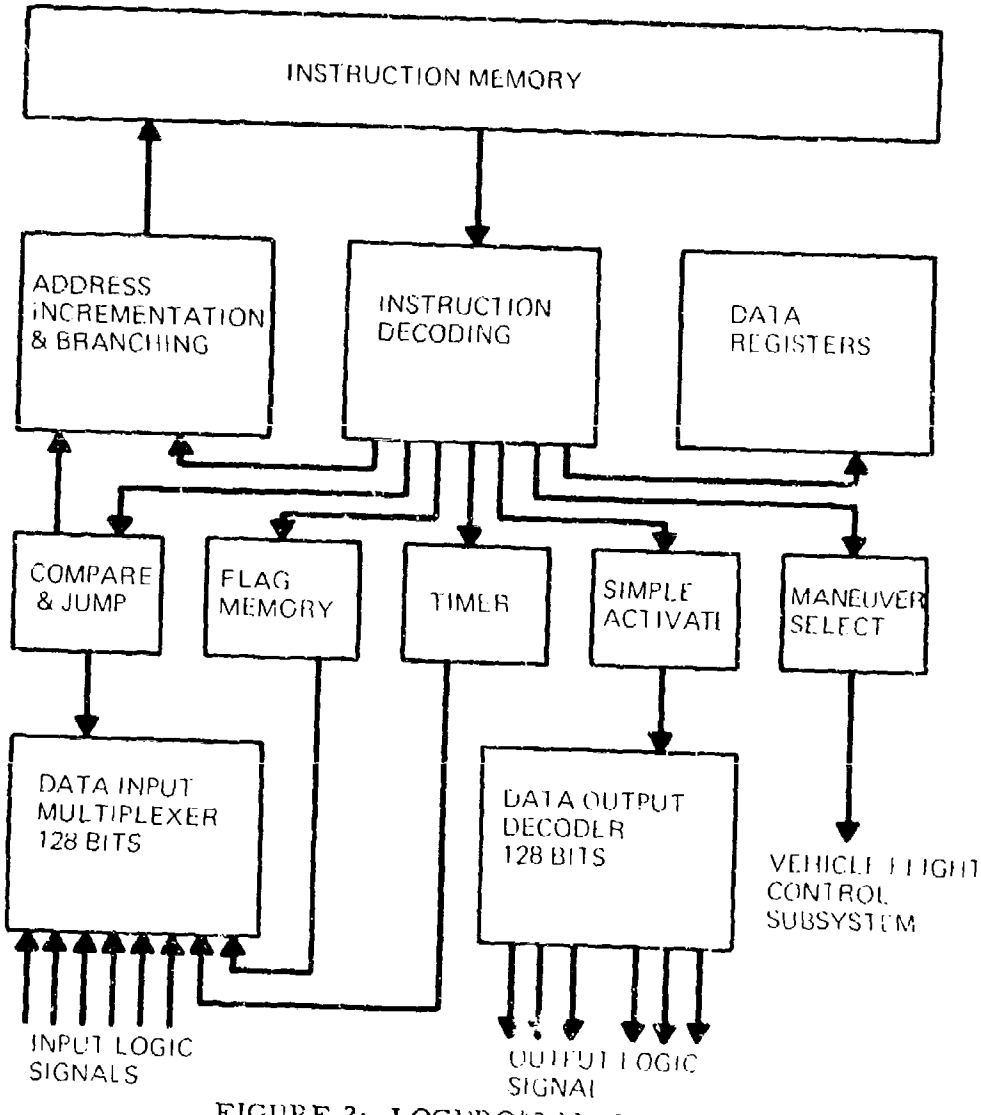

FIGURE 2: LOGPRO#3 block diagram

THE SYSTEM DIRECTOR FUNCTION

The selection and use of a LOGPRO machine implies a commitment of the torpedo to a hierarchial multiprocessor organization such as that shown in figure 3. LOGPRO was designed specifically to be the executive processor or system director. The director decides when and what each sub-system is to do. It provides set point information and cues action. Figure 4 provides a broad outline of the functions performed by the director.

Awkward separation between the processor and other sub-systems has been eliminated by design. LOGPRO directly addresses and loads registers in other sub-systems. It can directly address and force or test the state of binary variables anywhere in the system. These functions are accomplished using single instructions. The need for investment in multiplexers and decoders external to LOGPRO is eliminated because these features are built into the machine.

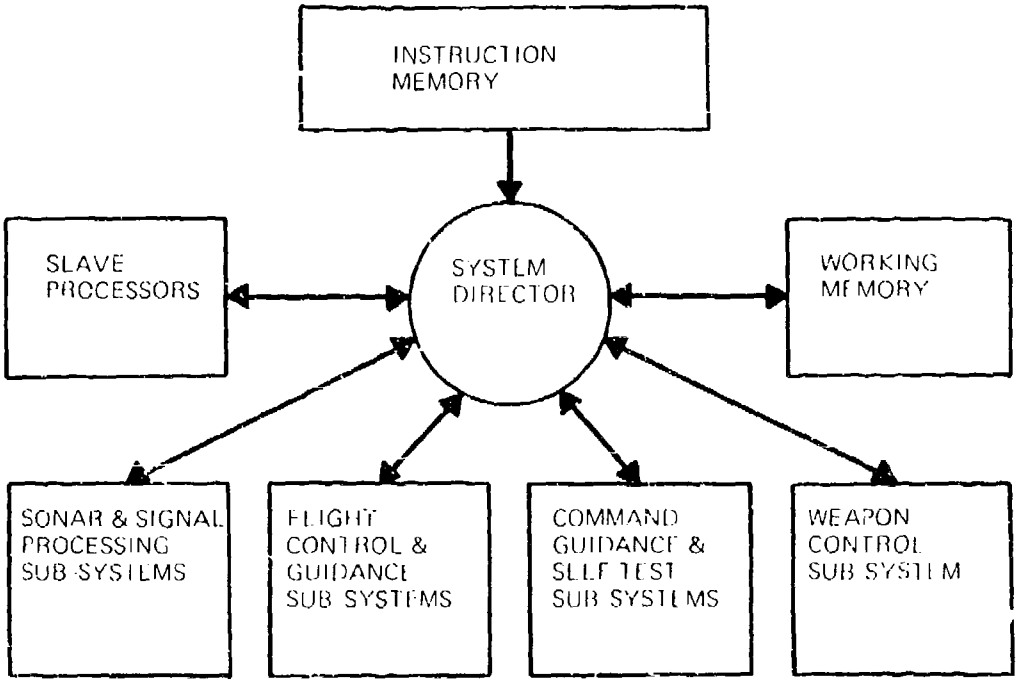

FIGURE 3: Simplified diagram of a torpedo multiprocessor organization co-ordinated by a system director machine.

The bulk of input data associated with decision making consists of one-bit logic variables which may originate from any sub-system. The decision making process requires the evaluation of a combinational Boolean expression where the terms of the expression are some subset of the input variables, time dependent variables, or the remembered result from earlier logical tests. The structure of the computer program (flow and branching) contains the decision rules mentioned in figure 4. The director may influence the system by forcing the state of logic variables or words within sub-systems.

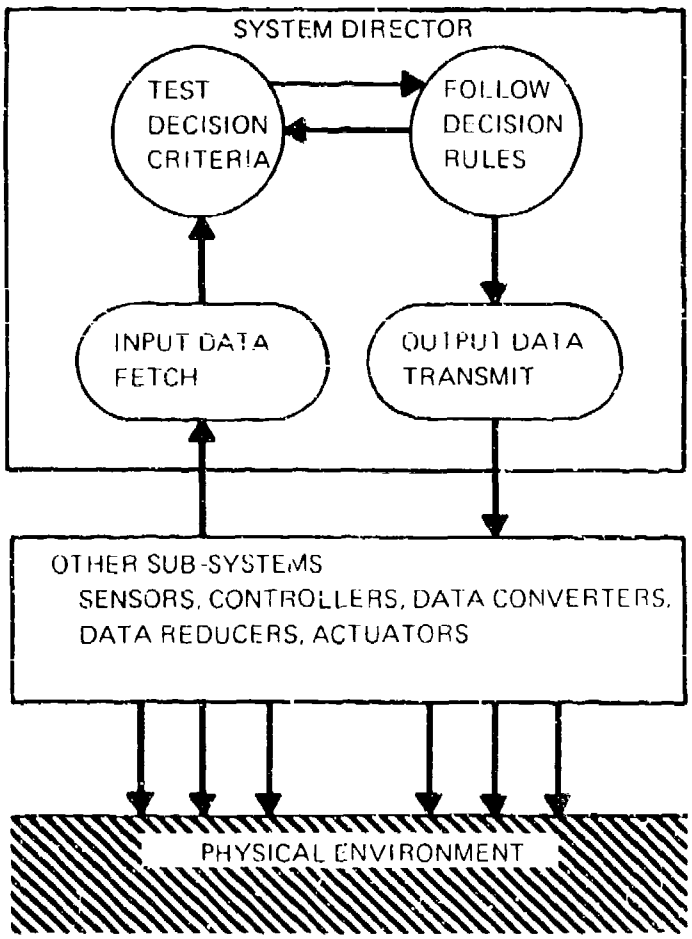

FIGURE 4: The functions performed by a digital director machine

THE INSTRUCTION SET

LOGPRO#3 has a machine language vocabulary of 11 instructions:

jump absolute	JA (m)
jump subroutine	JS (m)
return	RT
jump if true	JT (d) (s)
jump if false	JF (d) (s)
simple activate	SA (g) (p) (q)
set register	SR (r) (n)
set flag	SF (f, D) (f, D) (f, D)
set timer	ST (t) (e)
wait	WA
maneuver select	MS (k) (D) (ψ)

To test a Boolean expression a computer must be able to test a single Boolean variable. The "jump if true" (JT) and "jump if false" (JF) instructions provide this ability. A single instruction will directly address the variable, test its state, and branch conditionally to a specified address. Execution of all these actions in one instruction cycle provides a time saving and a reduction in instruction memory requirements. In contrast, computers which access the variable thru a non-transparent multiplexer will trypically execute 6 or more instructions to accomplish the same thing.

The director is of course a real-time decision maker. Time constraints are provided for by creating time dependent logic variables which can be tested in the same manner as any other binary variable. When the "set timer" (ST) instruction is executed a logic signal goes to the one state for the time interval specified by the argument of the instruction. A companion instruction call "wait" (WA) allows the option of halting machine operation until the specified time interval transpires.

Given the LOGPRO ability to efficiently test a single variable, the task of testing an expression is readily accomplished by software. If the Boolean expression is written as the sum of products, the number of instructions required to test the expression will be equal to or less than the sum of the number of variables in each term plus 2.

Expression: $A\bar{B}C + DE + \bar{F}GH$

Instructions required: $(3 + 2 + 3) + 2 = 10$

An important feature contributing to the efficient use of instruction memory is the provision for sub-routine branching. The "jump sub-routine" (JS) and "return" (RT) instructions allow multiple nested sub-routine calls out to 16 levels. The return address is saved automatically on execution of JS, and is recalled automatically on execution of RT.

Programming experiences to date indicate that the use of a LOGPRO machine offers a factor of 4 saving in instruction memory requirements. Assembly language programming has proven to be quite simple. Engineers responsible for a torpedo system have written their own programs without any special assistance.

SUMMARY

The physical and organizational aspects of the LOGPRO#3 prototype have been described. When a torpedo system employs a hierarchical multiprocessor architecture the use of a LOGPRO machine as the executive processor is appropriate. The LOGPRO design provides hardware economy and allows software simplification.

DESIGN OF POWER HYBRID MICROCIRCUITS FOR HIGH RELIABILITY APPLICATIONS

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ABSTRACT

In anticipation of the use of power hybrids (>25 watts) on the Space Shuttle, NASA awarded a study contract (NAS 8-26383) to develop guidelines for the design, fabrication, and screening of power hybrid circuits. The material presented in this paper is a summary of the results of that study.

INTRODUCTION

The study found significant differences between customary design, fabrication, and screening techniques for low power hybrid circuits, and these now evolving for power hybrids. These differences are primarily the result of the following considerations:

- Avoiding second breakdown in power transistors
- Minimizing thermal feedback from power transistors to temperature sensitive low power circuitry
- Providing interconnections with current carrying capability in excess of 1 ampere
- Providing resistors with power dissipation capability in excess of 0.5 watt
- Providing resistors below 1 ohm in value
- Considerably different form factor requirements

A summary of the findings in each of these areas is presented.

THERMAL DESIGN

Perhaps the most difficult of the above design considerations to achieve is a low enough chip to ambient thermal impedance to avoid second breakdown in power transistors. The first step in this direction is obtaining a hybrid package which is designed to

be mounted to a heat sink. The types most commonly in use are the bolt-down type and the stud-mounted packages (Figure 1). Inside the package, beryllia substrates, copper heat spreaders on alumina substrates, and thin alumina substrates are techniques which are being used to minimize junction to case thermal impedance.

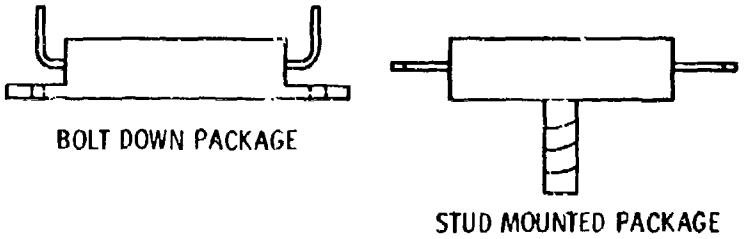

Figure 1. Package Types

In choosing between these techniques, a general rule of thumb, from a thermal impedance point of view, is to use a thicker, more conductive thermal structure in preference to a thinner, less conductive one. As an example, consider two designs with equal substrate impedance (Figure 2).

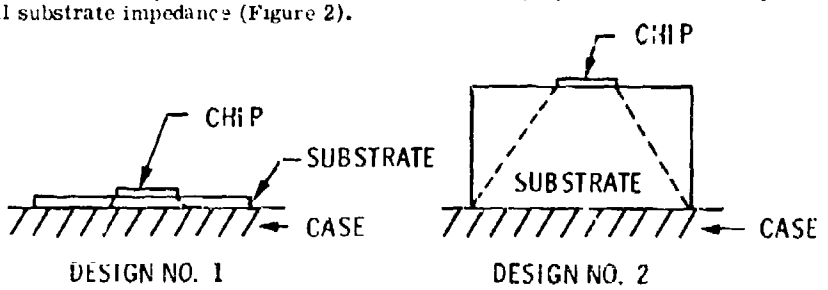

Figure 2. Substrate Thickness Comparison

Design No. 1 has a thin alumina substrate with the same thermal impedance as the thicker, more conductive beryllia substrate in Design No. 2. Assuming that the heat generated in the chip flows at a spreading angle of 45° [1], the heat in Design No. 2 will flow across the substrate-case bond over an effectively larger area than will be true for Design No. 1. This will result in a lower substrate to case thermal impedance for Design No. 2. Similarly, the case and case to heat sink impedances will be lower for Design No. 2 because the heat is flowing over a larger area.

THERMAL FEEDBACK

An important design consideration in circuits such as voltage regulators, where temperature sensitive low power components are located inside the package, is minimizing thermal feedback from power components to the temperature sensitive components. Analysis shows that thermal feedback is minimized when:

- Power component to heat sink impedance is minimized
- Temperature sensitive component to heat sink impedance is minimized
- The impedance between the two components is maximized

Achieving these three conditions simultaneously suggests using a thick conductive structure for mounting power devices and a thinner, less conductive, structure for mounting low power temperature sensitive components. One way of doing this is to use an alumina substrate for low power devices and a separate beryllia substrate for power devices.

INTERCONNECTIONS

High power circuit designs frequently require interconnections which will carry significantly more current than the film conductors typically found in low power hybrids. Double printing of thick film conductors, conductor runs up to an order of magnitude wider than those usually found in low power circuits, and large diameter aluminum wires (5-20 mils) similar to those found in power transistors are being used to conduct currents in the 1 to 40 ampere range. Typical thick film conductors produced by usual processes will support 1 to 2 amperes per 10 mils of conductor width. However, the series resistance of these conductors may become significant. Therefore, it is important to keep runs as short and as wide as possible. Many thick film manufacturers include minimum design widths in their design specifications when the resistance of conductor runs becomes critical. Most thick film conductors will fall within the range of 0.001 to 0.1 ohm per square. Resistances on the lower end of this range are achieved by specifying maximum percentage gold and maximum thickness. Increased thick film conductor thickness and thus lower resistance may be achieved through the use of larger screen mesh and/or emulsion thickness or very simply by repeated printings of the conductor.

RESISTORS

Thick film resistors printed with palladium-silver, ruthenium oxide and/or platinum based metal systems can reliably handle power densities as high as 1000 watts per square inch of resistor material, if adequate heat sinking to maintain temperatures below 150°C is available. Test resistors printed with these materials remained stable to a continuous power loading of 500 watts per square inch for more than 3000 hours. A drift in resistance of less than 0.5% was observed for all the resistors except those printed with a 10 ohms per square palladium-silver material. These changed less than 2.0% after 3000 hours.

Another aspect of resistor stability to be considered when high-power handling is involved is that of long term stability to elevated temperatures. The results of many investigators show that the resistors fabricated with the above paste systems have excellent long-term stability to temperatures up to 200°C. Some paste manufacturers claim less than 0.5% drift in resistance after 10,000 hours at 150°C in air for all resistivities ranging from 1 ohm per square to 1 megohm per square.

Another concern for the engineer designing thick-film resistors in high power applications is their sensitivity to voltage. The effect of this sensitivity is minimized by designing long (multiple square) resistors in preference to short (fractional square) resistors. The use of paste systems that have been shown to be less sensitive to voltage gradients also minimizes the danger of resistor drifts in high power applications. Paste systems rated in excess of 2000 volts per inch of length for most resistivities are available from several paste manufacturers.

CONDUCTOR RESISTORS

Film conductors may be used to form the low value high current resistors one often finds in power circuits. Resistances on the order of 0.005-0.1 ohm per square are generally obtainable. This approach is most useful when:

- The relatively high TC (up to 4000 ppm/°C) of conductors can be tolerated
- Use of this technique results in a smaller area requirement than a standard film resistor
- Tolerance is acceptable (obtainable tolerance will depend heavily on the individual trimming process; for example, whether or not laser trim is available)

An excellent example of where this technique can be used to good advantage is in the construction of sense resistors which are used to limit the output current of power amplifiers and series regulators during an overload.

FORM FACTOR

Form factor requirements for power hybrids differ substantially from those for low power hybrids. The user of low power hybrids normally places hybrid circuits on a printed circuit board along with many other components. Thus to complete the function of the hybrid circuit by requiring external components elsewhere on a printed circuit board is not a significant tradeoff.

In the case of power hybrids, the situation is quite different. The power hybrid will normally be mounted on a heat sink where it is not so convenient to mount external components. Therefore, to achieve an acceptable form factor, mounting of external components directly to the hybrid package, and modules designed specifically for power hybrids are being used.

CONCLUSION

The findings of the study clearly indicate that micro (hybrid microelectronic) is no longer synonymous with micro power. Hybrid microelectronic techniques were found to be readily adaptable to high power circuit designs (>25 watts).

REFERENCES

(1) L. Balents, R.D. Gold, A.W. Kaiser, W.R. Peterson, "Design Considerations for Power Hybrid Circuits," Proceedings 1969 Hybrid Microelectronics Symposium, October 1969.

SUBMINIATURIZATION OF TELEVISION CAMERAS THROUGH HYBRID I.C. TECHNOLOGY

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The effective utilization of hybrid I.C. packaging in television systems will be surveyed to clarify the steps which led to the creation of a series of self-contained subminiature television cameras.

Over the past decade, television technology has achieved significant advances in performance capability through new sensor developments, as well as improvements in physical format through solid state techniques. However, television systems, like the majority of other hardware areas, have not kept in stride with the rapidly emerging Multichip Hybrid Package concepts. In an attempt to rectify this situation, a series of subminiature television cameras have been developed which effectively mate the state-of-the-art capabilities in both sensor and hybrid I.C. techniques.

The creation of an MHP full-capability television camera followed use of emerging hybrid IC fabrication techniques in miniaturizing the digital circuits required in imaging systems. The EIA Sync Generator shown in Figure 1, was initiated in 1967 and was the first production-oriented unit designed for TV. It uses 22 monolithic digital chips to provide full EIA mixed sync, mixed blank, and horizontal and vertical drive outputs. It was used in a Compact Camera series and the Apollo Color TV Camera, and it demonstrated high reliability in the extremes of environmental testing for these uses.

The Sync MHP contains an all-digital sync generator, in which a high-frequency clock is divided by 25 to provide twice the horizontal. The logic available in the ÷ 25 counters is used to generate the horizontal blanking, equalizing pulses, and serrations. The vertical reference is generated by a ÷ 525 countdown. The logic available in these counters generates the vertical drive and blanking and the vertical sync intervals. Mixed sync and blank outputs are formed by summation. The unit can operate in the 525 mode (60Hz vertical American standard, or with one jumper, in the 625 (50 Hz vertical) European standard.

The 1-inch square sync MHP is a direct replacement for commercially available units typically one hundred times its size. Having successfully achieved the implementation of the digital circuitry necessary in a television system, the self-contained SUBMIN-TV (Figure 2) was initiated to make full utilization of MHP capability for both the digital and analog functions required in a television camera. Some of the basic parameters of the SUBMIN-TV are listed below.

Sensor	½" Vidicon
Beam Focus	Electrostatic
Beam Deflection	Magnetic
Size	1.5 x 1.5 x 5 in.
Weight	9.6 ounces
Input Voltage	12 ± 1 Vdc
Input Power	6.0 W at 12 V
Scan Format	525 line, 30 frame/sec switchable to 625 line, 25 frame/sec
Video Bandwidth	6 MHz
Video Format	1.4 V video into 75 ohms EIA RS 170
Operating Temperature	-20 to +55°C
Maximum Resolution	450 TVL/RH
S/N at 4 fc Faceplate Illum	36 dB

The implementation of digital circuits and use of new techniques makes the SUBMIN-TV electronics as unique as the packaging. As shown in the block diagram (Figure 3), the unit is divided, electrically and physically, into functional blocks that provide isolation and logical signal flow. Each of the 6 major blocks is contained in a 1-inch square hybrid package.

The Preamp MHP uses an FET front end and a feedback configuration to compensate for the target RC knee.

The Postamp Package amplifies and clamps the Preamp output and processes it with mixed sync and mixed blank logic to form the EIA RS 170 composite broadcast video format, which contains full equalizing and serration pulses.

The Sweep Package (Figure 4), is a five layer thick film unit and uses a Miller run-up feedback configuration to generate the vertical current sawtooth. The horizontal deflection sawtooth is generated by an inductive flyback approach.

The SFP block contains the master oscillator, high voltage drive, horizontal and vertical sweep fail protection, and cathode blank driver circuits. The HVPS drive circuits synchronize inverter switching transients with the horizontal interval to eliminate pick-up. Sweep fail

detection circuits blank the sensor cathode if a sweep failure occurs.

The hybrid fabrication techniques used in the original SUBMIN-TV lend themselves directly to an off-the-shelf building block type of production. Small package size and simple interconnections allow adaptations to nearly any configuration. This capability was used to advantage in the development of the WTC-25 low cost television camera (Figure 5). As shown in Figure 6, the camera uses four of the basic SUBMIN-TV 1-inch square thick film MHP to provide the electronics required. As indicated by the camera assembly, the four MHP are mounted thru connector strips and are thus field replaceable. In a production orientation, the MHP are tested in individual test fixtures, installed in a final camera for a total system checkout and then sealed and marked.

Again using the SUBMIN-TV technology as a building block, a miniature low-light level camera was developed using eight MHP units to drive a 16mm EBS image tube (EBSICON). The MINSIT TV Camera (Figure 7) is a completely self-contained unit and contains automatic gain, light level, aperture correction, and iris drive control loops in addition to a complete built-in-test capability. The camera's basic parameters are listed below.

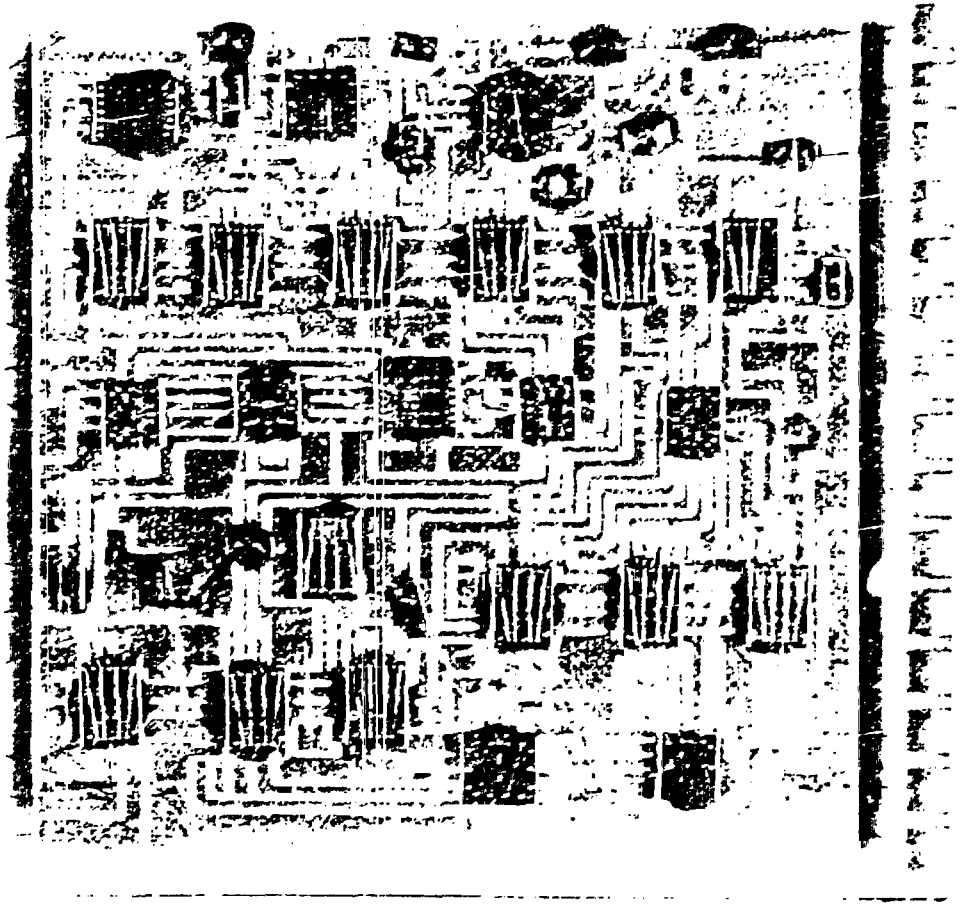
Sensor	16mm SIT
Image Focus	Electrostatic
Deflection and Focus	Magnetic
Size	2.7 in. dia, 9.87 in. long
Input Power	10 W at 12 $\pm$ 2 V
Scan Format	525 line, 30 frame/sec
AGC/ALC Range	< 6dB change over 10,000:1 light range
Video Bandwidth	7.5 MHz
Resolution	625 TVL/RH to 10^{-3} fc (Faceplate)
	400 TVL/RH at 5×10^{-5} fc (Faceplate
Video Output	1.4 V p-p EIA RS 170

The Minsit Aperture Corrector MHP shown in Figure 8 is indicative of total thick film units possible in a large volume orientation. Prior packages have used resistor chips because of the greater cost effectiveness and substrate versatility for small quantity development units.

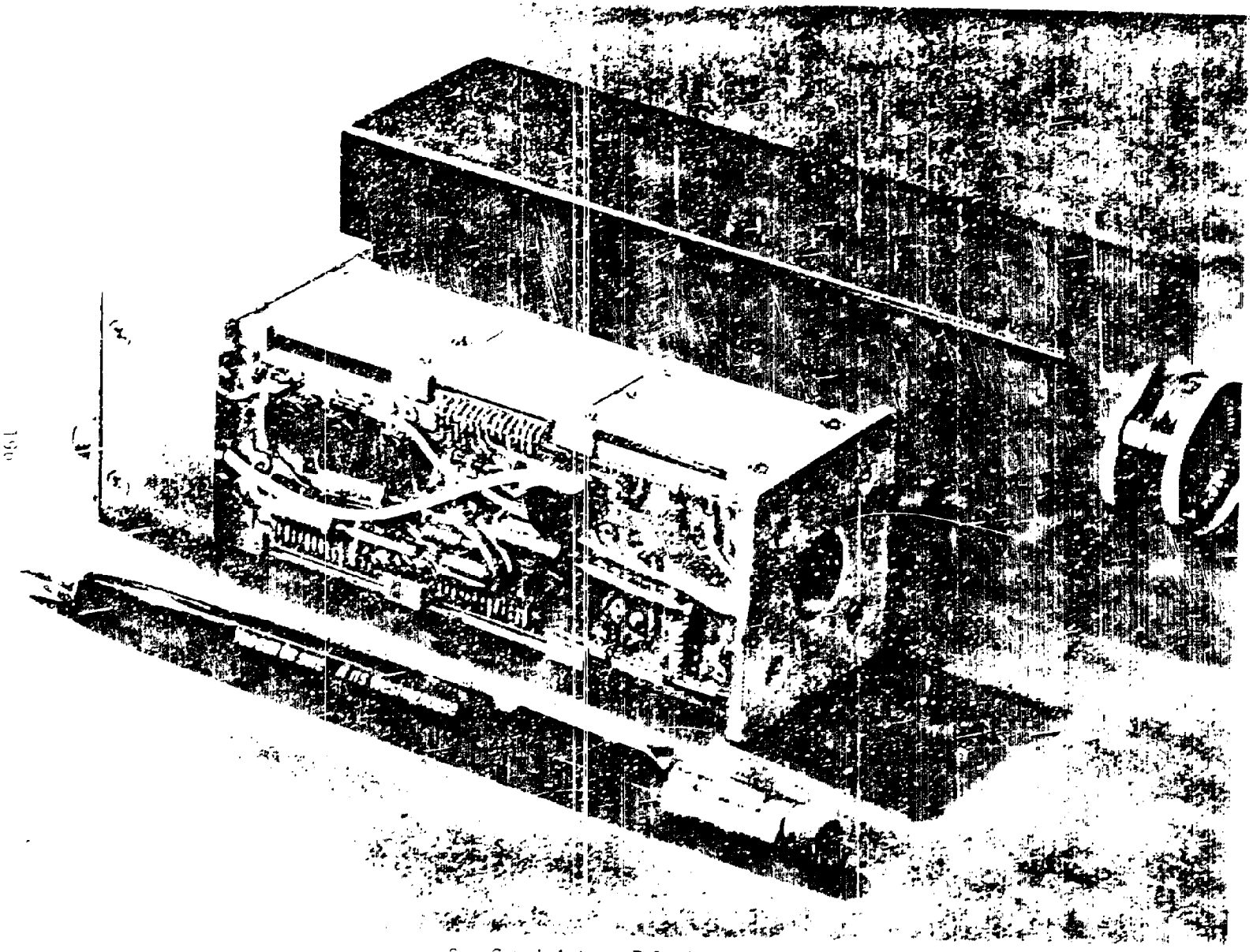
The three basic television camera units described are used in a vast array of applications which take particular advantage of the size and weight afforded by the use of MHP units. Typical applications

include project instrumentation, weapon delivery, gimbal mounted video tracking, drone reconnaissance, oceanographic surveillance, and mine rescue operations.

The successful utilization of hybrid technology in television camera systems exemplifies the advantages inherent with this approach. Its application to other forms of hardware can be made with similar results.



1. Sync Generator MHP



2. Subminiature Television Camera

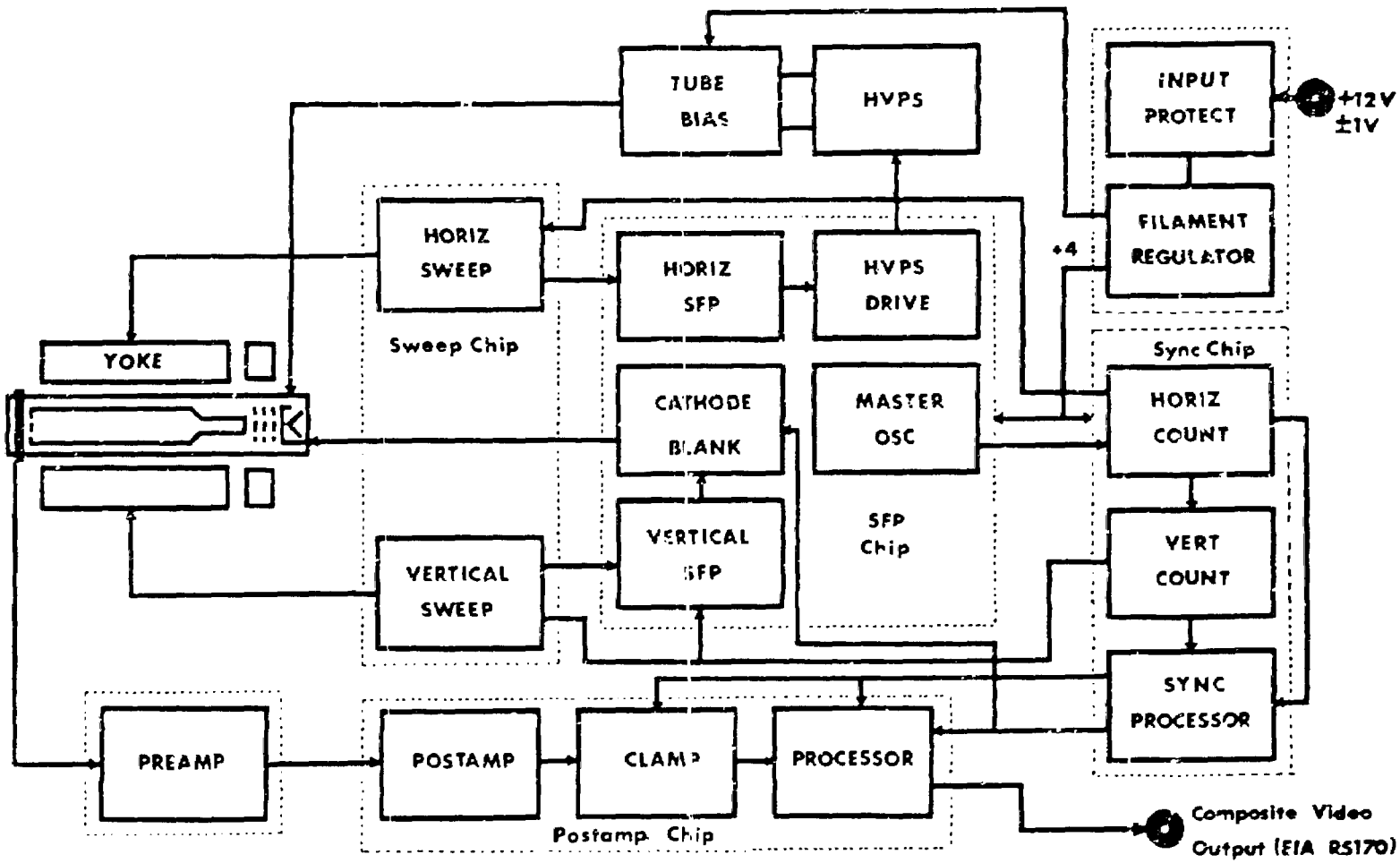
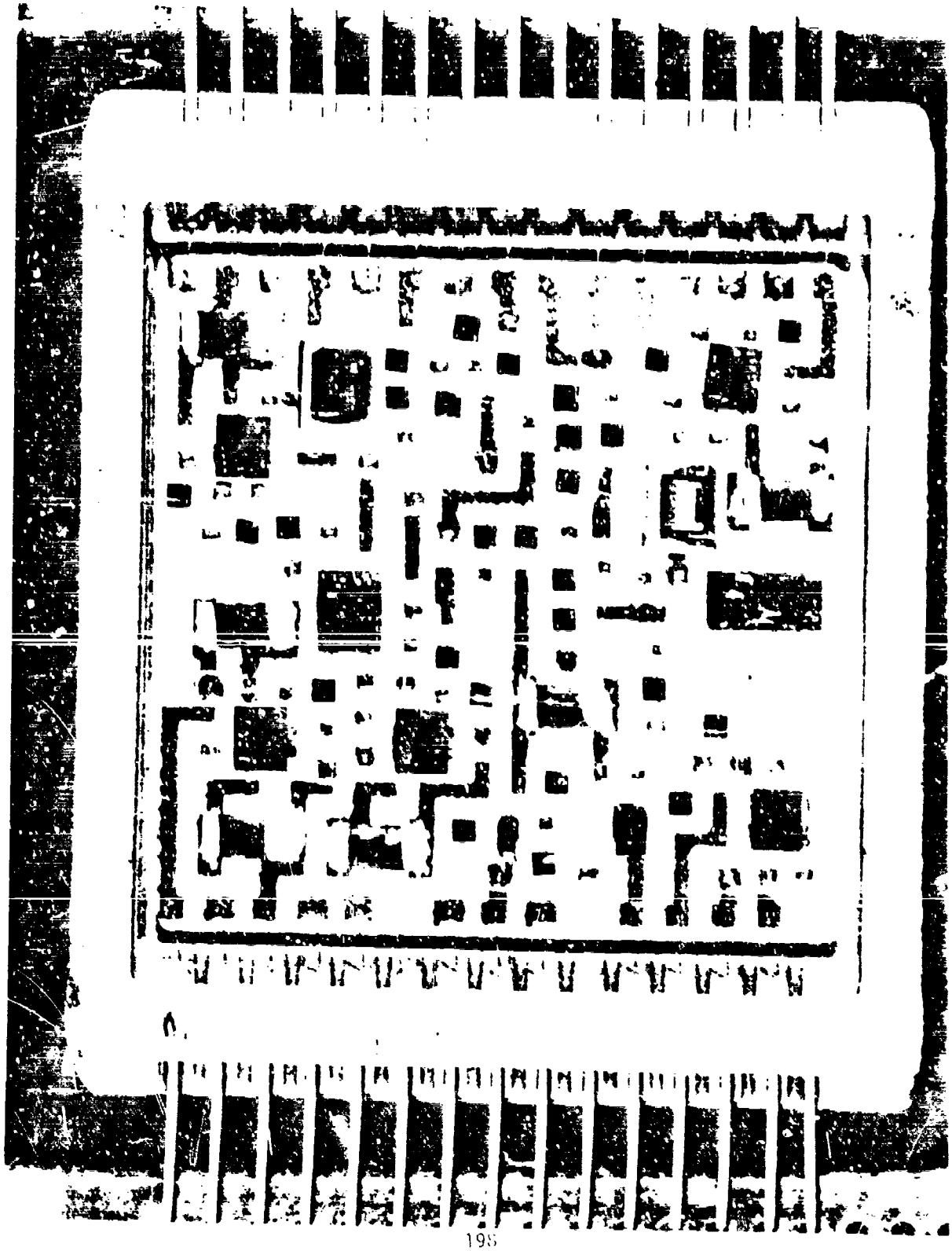
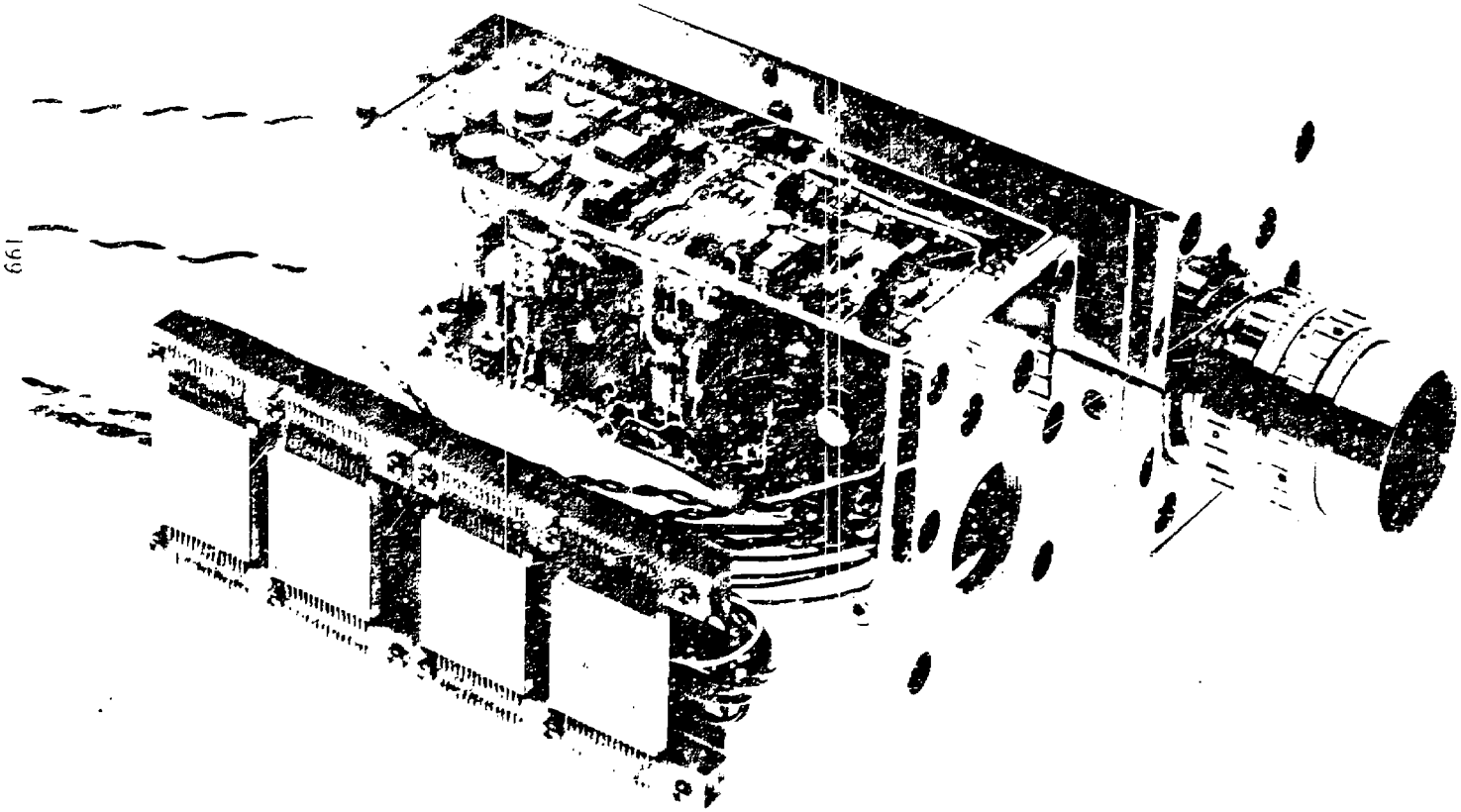
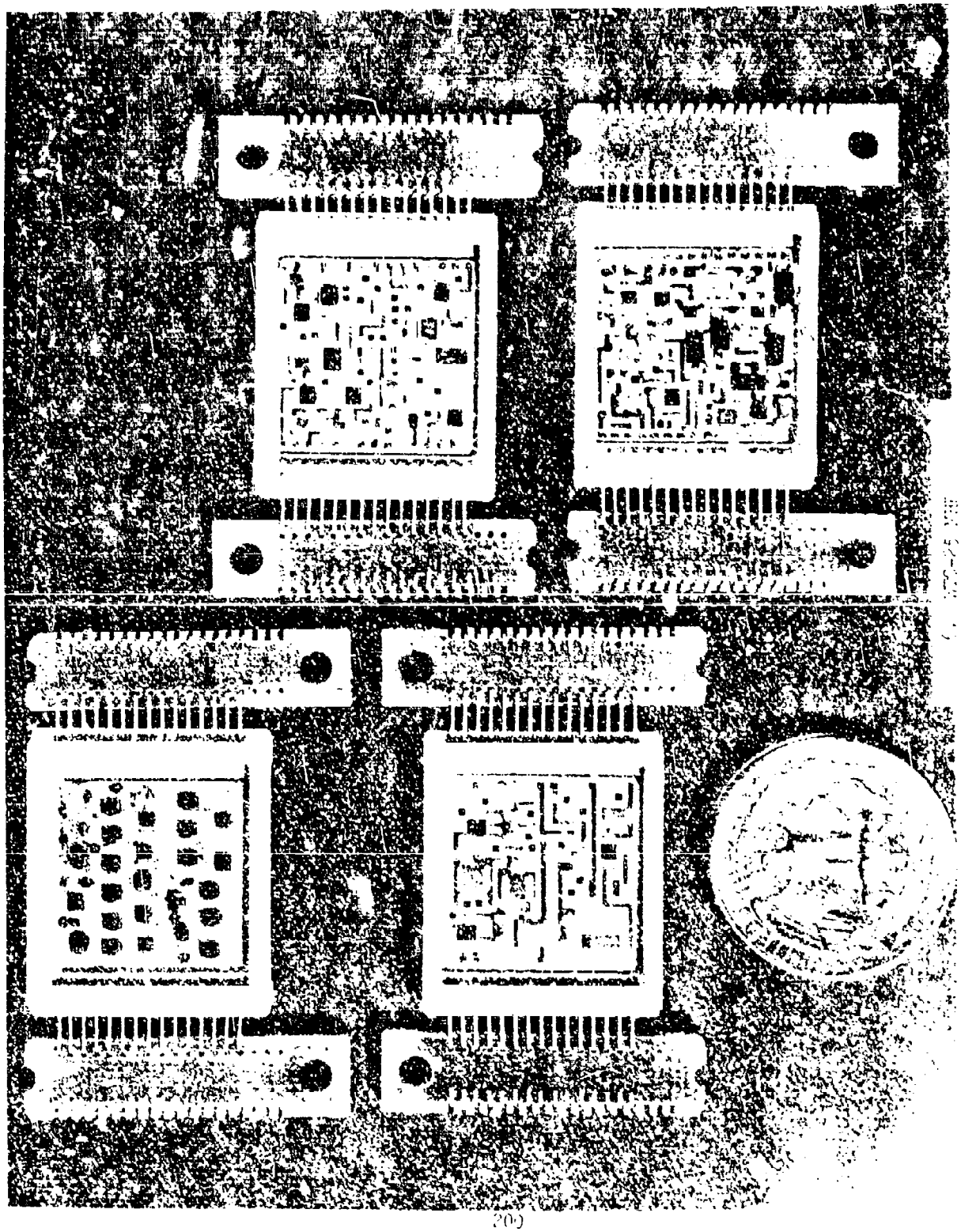


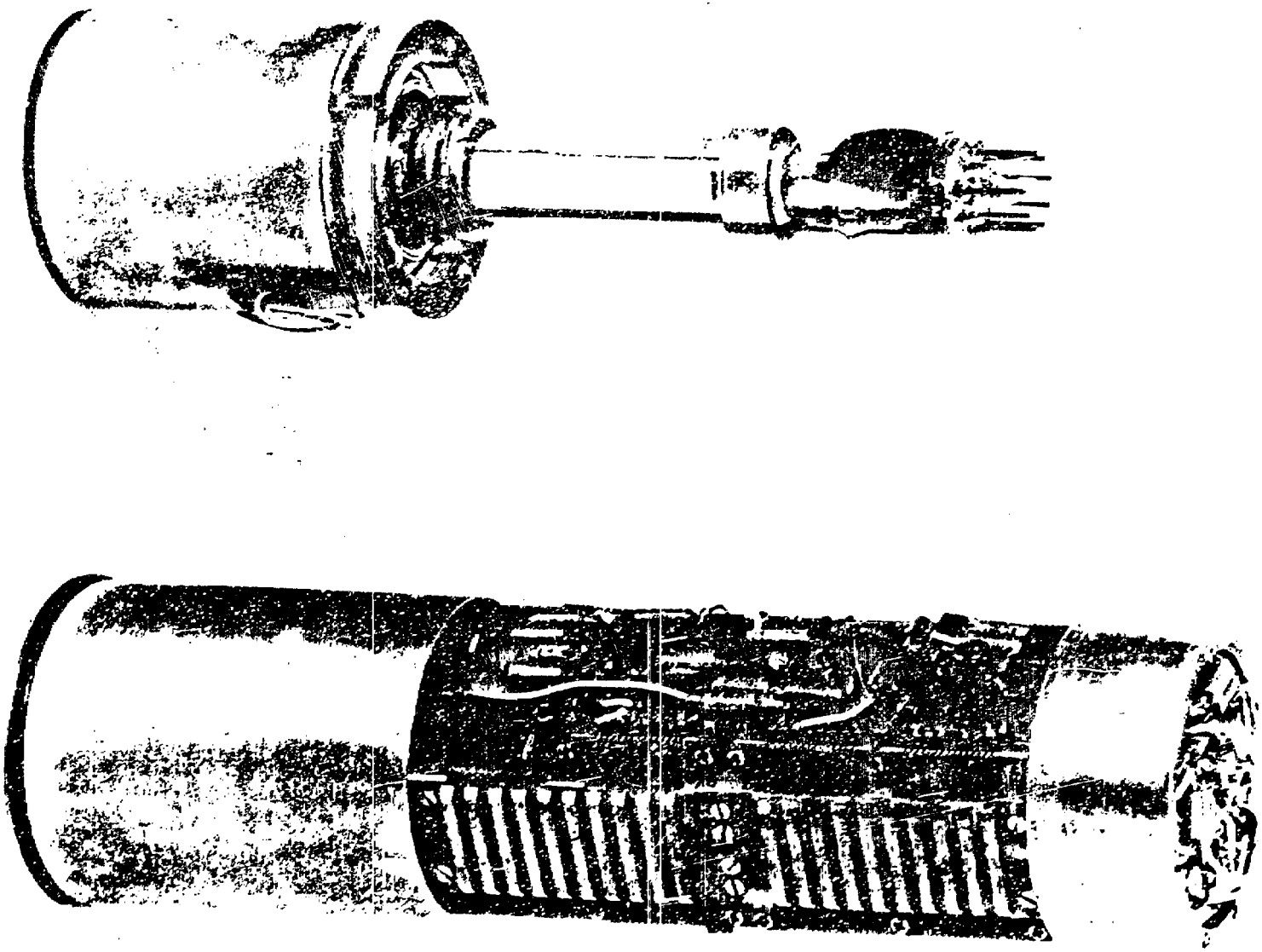
Figure 3 SUBMIN-TV System Block Diagram



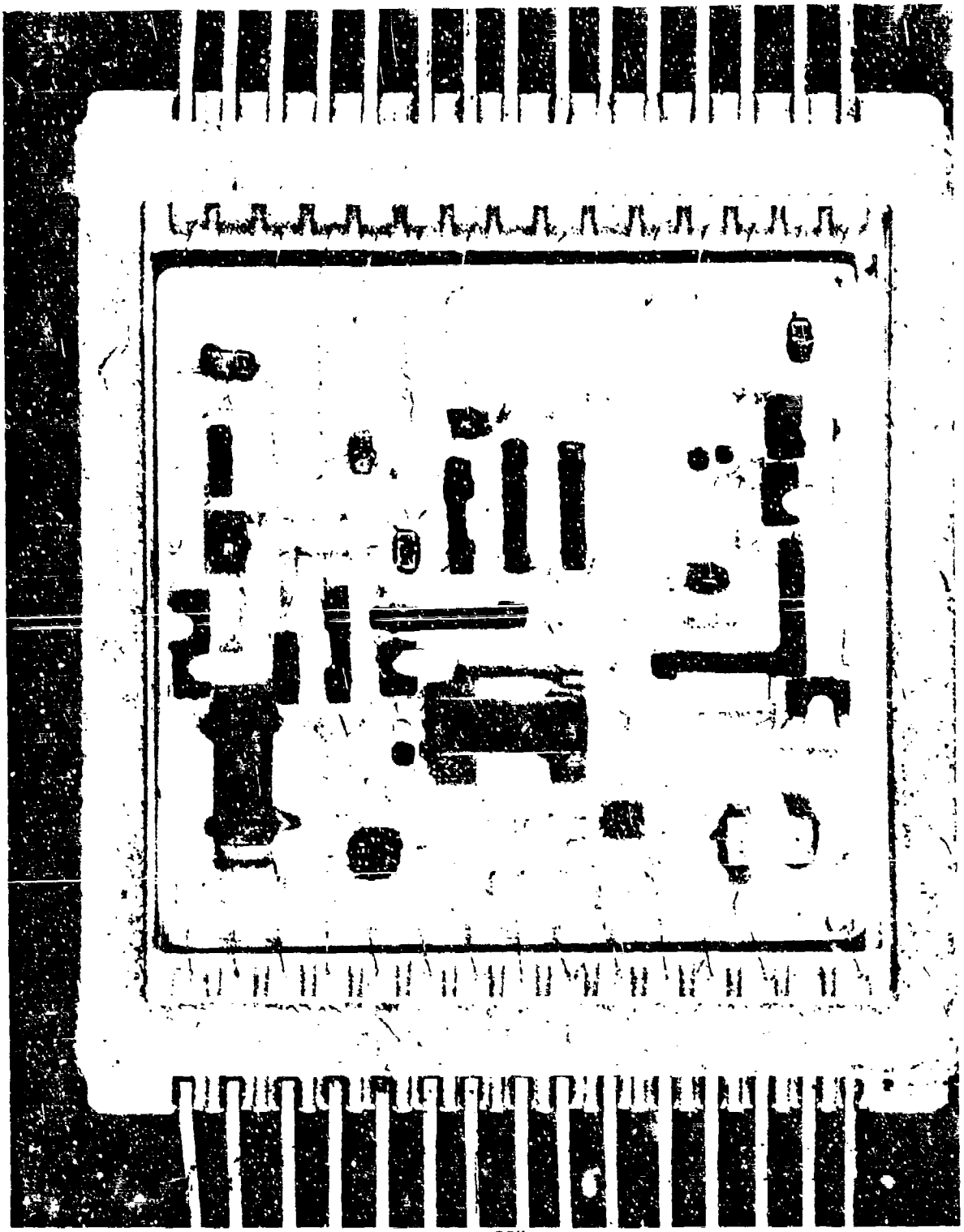


5. WTC-25 SUBMIN-TV





7. MINSIT L^3TV Camera



8. Aperture MHP

RADIATION CHARACTERISTICS OF HARDENED DIGITAL IC FAMILY

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ABSTRACT

This paper presents the radiation characterization in simulated nuclear environments of pilot production units from a recently developed hardened low-power Transistor-Transistor Logic (TTL) integrated circuit family. The devices were developed by the Air Force Material Laboratory, Wright-Patterson AFB, Ohio, and were monolithic integrated circuits designed for use in radiation environments. The technologies utilized in development of these devices included dielectric isolation, thin film nichrome resistors, minimum transistor geometry, photocurrent compensation and resistor current limiting.

A total of ten device types were fabricated including six different gate structures, three different bistable multivibrators and a monostable multivibrator. A total of 310 devices were received for this parts characterization program. The devices were irradiated in five separate radiation facilities which included a Cobalt-60 source, a low-energy x-ray, a linear accelerator (LINAC), a flash x-ray and a nuclear reactor. The device parameters that were monitored and reported include saturation voltage, rise time, fall time, power drain, transient response, burn-out and latch-up.

TEST PROGRAM

The devices characterized during the test program were low-power radiation hardened TTL integrated circuit devices designated as the RSN 54L series. They were pin-for-pin replacements for their unhardened low-power counterparts in the SN 54L family. Table 1 tabulates the device types characterized in the radiation environments.

In addition to the nine device types tabulated in Table 1, a special radiation hardened flip-flop family was fabricated in accordance with circuit design specifications provided by Hughes Aircraft Company. These special devices were designated as HIC 117A, HIC 117B, HIC 117C and HIC 117D and were a modified circuit design of the RSN 54L 71 RS Flip-Flop device. The Hughes specifications for these modified devices were calculated to significantly improve the radiation error threshold of the RS Flip-Flop when irradiated in a highly ionizing environment.

TABLE 1. RSN 54L FAMILY SERIES

1.	RSN 54L 00	Quad-2 Input Gate
2.	RSN 54L 10	Triple-3 Input Gate
3.	RSN 54L 20	Dual-4 Input Gate
4.	RSN 54L 57	And-Or-Invert Gate
5.	RSN 54L 71	RS Flip-Flop
6.	RSN 54L 74	Dual D Edge Triggered Flip-Flop
7.	RSN 54L 122	Monostable Multivibrator
8.	RSN 54L 130	Dual-3 Input Gate
9.	RSN 54L 131	Dual-3 Input Gate with Extender

All of the above devices utilized design techniques for improved survivability in a hostile nuclear radiation environment. Dielectric isolation was used to preclude the possibility of radiation induced latch-up and to minimize photocurrents. Minimum transistor geometry was used to minimize photocurrents and minimize neutron induced degradation. Thin film nichrome resistors and photocurrent compensation were used to minimize the transient photocurrent responses. Resistor limiting was used in all leads connected to the power distribution bus to minimize the possibility of burn-out. The hardened integrated circuits were irradiated at the five radiation facilities listed in Table 2.

TABLE 2. RADIATION TEST FACILITIES

Facility	Location	Range of Irradiation Levels
Cobalt-60	Hughes	1×10^4 to 2×10^7 rad(Si)
Steady X-Ray	Hughes	1×10^3 to 1×10^7 rad(Si)
Linac	Hughes	1×10^7 - 1×10^{10} rad(Si)/s
Flash X-Ray	HERMES II	1×10^{10} - 5×10^{11} rad(Si)/s
Nuclear Reactor	WSFBR	1×10^{13} - 1×10^{15} n/cm^2

TEST RESULTS

A close examination of the bias current data before and after each irradiation series for each device reveals less than 5% difference between the BEFORE and AFTER readings for most devices. This is approximately the error range for visual reading of the bias current meters. Thus, the general conclusion is made that the change in bias current for all of the devices was negligible for the radiation test levels at all five radiation facilities.

Transfer characteristics were monitored for devices in the Cobalt-60 tests, x-ray tests and in the LINAC tests. The transfer characteristics before and after irradiation were plotted. No appreciable changes in the transfer characteristics were evident even when the devices were irradiated to the maximum levels in the permanent effects degradation tests.

The saturation voltage was measured on every device tested in each environment at five values of load current ranging from unit load to 4X overload. The test data shows an increase of only a few millivolts at full load for all devices except those irradiated at the nuclear reactor. Those devices showed acceptable levels of degradation up to neutron irradiations approximating 2×10^{14} n/cm^2.

The rise-time, fall-time data is important since it indicates a decrease in maximum operating speed with increasing radiation dose. The test results showed that in all cases the device fall-time was not significantly affected at any levels of irradiation. The device rise-times, however, were significantly increased in all environments.

The devices irradiated in the Cobalt-60 exhibited a fairly linear increase in rise-time reaching approximately a 50% increase at 3×10^7 rad(Si). The devices irradiated in the steady-state x-ray also exhibited a fairly linear increase in rise-time reaching approximately a 50% increase at 1×10^6 rad(Si). The devices irradiated in the linear accelerator exhibited an exponential increase in rise-time reaching 50% at approximately 3×10^6 rad(Si). The devices irradiated at the super flash x-ray exhibited a 50% increase in rise-time over a dose range of 1×10^4 to 1×10^5 rad(Si). The devices irradiated in the neutron environment exhibited an exponential increase in rise-time reaching 100% increase as indicated in Table 3.

TABLE 3. NEUTRON FLUENCE INDUCING 100% RISE-TIME INCREASE

Device	n/cm^2	Device	n/cm^2
Quad-2 Input Gate	2E14	Monostable MV	1E14
And-Or-Invert Gate	2E14	Dual D Flip-Flop	8E13
RS Flip-Flop	1E14	Triple-3 Input Gate	6E13
Dual-3 Input Gate	1E14	Dual-3 Gate Ext.	2E13

A total of 65 devices were irradiated in the linear accelerator test program at dose rates up to 3×10^{10} rad(Si)/s. A total of 60 devices were irradiated in the flash x-ray test program at dose rates up to 5×10^{11} rad(Si)/s. Each device was exercised after every irradiation pulse and monitored for evidence of latch-up or burn-out. No evidence of latch-up or burn-out was seen during either the linear accelerator testing or the flash x-ray testing.

Table 4 lists the range of transient error threshold for each device type. Error thresholds for Table 4 are defined as the dose rate level causing an output voltage transient to drop below 3.0 volts when the output is in the logical ONE state or to raise above 0.8 volts when the output is in the logical ZERO state. This data was measured at the linear accelerator with the devices maintained in a steady DC condition.

TABLE 4. RANGE OF TRANSIENT ERROR THRESHOLDS

Device	Threshold rad(Si)/s
Dual D FF	1E10 - 3E10
HIC 117D	8E9 - 1E10
HIC 117C	7E9 - 2E10
HIC 117B	5E9 - 2E10
Triple-3	5E9 - 2E10
AOI	3E9 - 6E9

Device	Threshold rad(Si)/s
Dual-3	2E9 - 3E10
Dual-3 Ext.	2E9 - 1E10
Dual-4	5E8 - 7E9
RS FF	5E8 - 4E9
Quad-2	1E8 - 7E9
MV	1E7 - 5E7

Table 5 shows the results for the flash x-ray testing to determine the static phase shift error threshold. This error threshold is defined as the radiation level required to induce an erroneous change of state in a multivibrator circuit. These are static tests which means that the multivibrators were not being clocked or triggered during the irradiation pulse. No attempt was made to clock or trigger these circuits concurrent with the flash x-ray pulse since a satisfactory synchronization pulse could not be established with the Hermes II machine. The Monostable Multivibrator device has the most sensitive static error threshold of 4×10^8 rad(Si)/s. The table shows the progressive hardness of the device types culminating in the HIC 117D which has a hardness level above the capability of the Hermes II machine.

TABLE 5. MULTIVIBRATOR STATIC PHASE SHIFT ERROR THRESHOLDS

Device	Designation	Static Phase Shift Error Threshold rad(Si)/s
Hardened FF	HIC 117D	5E11
Hardened FF	HIC 117C	5E11
Hardened FF	HIC 117B	1E11
Hardened FF	HIC 117A	4E10
Dual D FF	RSN 54L 74	4E10
RS FF	RSN 54L 71	1E10
Monostable MV	RSN 54L 122	4E8

Table 6 shows the results from the linear accelerator testing to determine dynamic phase shift error thresholds. The dynamic error threshold is defined as the radiation level required to induce an

TABLE 6. MULTIVIBRATOR DYNAMIC PHASE SHIFT ERROR THRESHOLDS

Device Type	Maximum Operating Speed (MHz)	Dynamic Phase Shift Error Threshold rad(Si)/s		
		100 ns pulse	200 ns pulse	400 ns pulse
Hard Flip-Flop HIC 117D	0.4	*	*	2E10
Hard Flip-Flop HIC 117C	0.7	*	*	8E9
Hard Flip-Flop HIC 117B	1.0	5E10	1E10	2E9
Dual D Flip-Flop RSN 54L 74	5.0	1E10	N/A	N/A
RS Flip-Flop RSN 54L 71	2.0	5E9	N/A	N/A
Hard Flip-Flop HIC 117A	2.0	2E9	7E8	6E8

* Dynamic error threshold greater than linear accelerator maximum capability of 5E10 rad(Si)/s.

erroneous change of state in the multivibrator circuit when that circuit is being clocked or triggered. These are dynamic tests, which means that the clock or trigger signal which exercises the multivibrator circuit is synchronized with the linear accelerator radiation pulse.

The dynamic phase shift error threshold tests showed four important results. First, they showed that all of the multivibrator circuits tested were more susceptible to radiation induced phase shift when the circuit output was in the process of changing states as a result of an applied clock pulse or trigger. Thus, the Dual D Flip-Flop was most sensitive immediately following the leading edge of the trigger signal while the RS Flip-Flop family was most sensitive immediately following the trailing edge of the clock pulse signal.

Second, these tests also showed that the circuits become more susceptible to radiation induced phase shift errors as the multivibrator devices are clocked at speeds approaching their maximum capability. This occurs since a multivibrator circuit being clocked at near its maximum operating capability does not have sufficient time for the internal reactive components (including distributed capacitance) to settle to their quiescent voltage levels, thus providing maximum noise rejection.

Third, these tests also show how the HIC 117 family of circuits become more susceptible to radiation induced dynamic error thresholds

as the duration of the radiation pulse is increased. This occurs since the hardening capacitance in these circuits becomes discharged at lower irradiation levels as the pulse duration becomes longer.

An finally, these tests show the ionization hardness achieved by the HIC 117 family series of circuits. This data shows the increase in dynamic error threshold achieved as larger capacitance values are added to the basic hardened flip-flop circuit. These figures also show how the additional capacitance decreases the maximum operating speed, and how radiation pulse width affects radiation hardness.

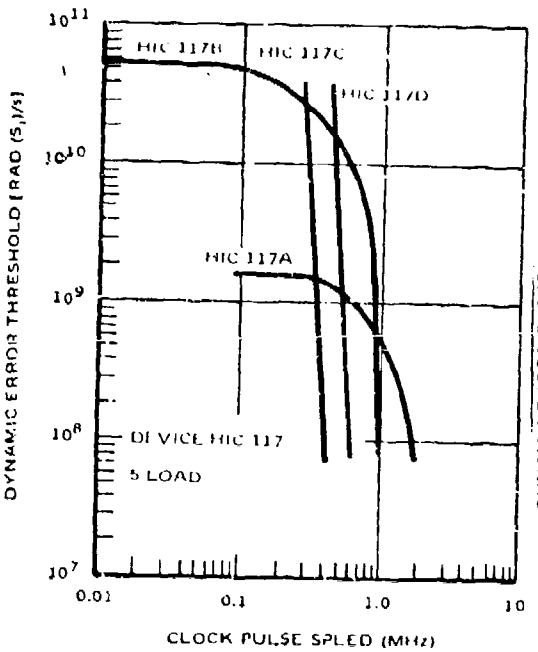

Figure 1.
HIC 117 Composite,
100 NS Pulse Width,
Dynamic Error Threshold,
Linac

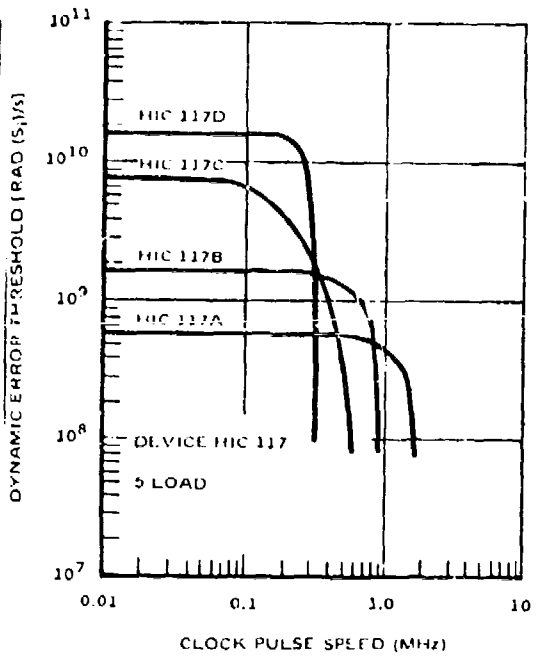

Figure 2.
HIC 117 Composite,
400 NS Pulse Width,
Dynamic Error Threshold,
Linac

UNIVERSAL DIGITAL INTEGRATED CIRCUIT*

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ABSTRACT

The Universal Digital Integrated Circuit (UDIC) is a radiation-tolerant, beam-leaded design capable of forming with appropriate external pin interconnections any one of four digital circuits.

INTRODUCTION

The Universal Digital Integrated Circuit (UDIC) is a radiation-tolerant design offering four digital functions on a single monolithic chip. With appropriate external pin interconnections, and the addition of timing and/or input triggering capacitors, the UDIC is capable of functioning as a (1) Dual Nand Gate, (2) Single-Shot Multivibrator, (3) Free-Run Multivibrator or (4) Pulse-Triggered Binary. The UDIC requires that two radiation hardening techniques be combined into beam-leaded form. These techniques are dielectric isolation of all active devices and the use of thin film resistors. The UDIC is a format 70 chip.

FUNCTIONAL DESCRIPTION

Since the schematic of the UDIC, shown in Figure 1, is symmetrical, the following discussion will be limited to one side. Darlington-connected transistors in both the pull-up (Q1-Q2) and pull-down (Q3-Q4) are used to insure proper operation after exposure to severe neutron environments. When Q3 and Q4 are "on," their Schottky-clamped collectors hold Q1 and Q2 "off." With an input less than three diode drops on any of the diodes CR7 through CR10, Q3 and Q4 will be "off" and Q1 and Q2 will be "on" if output current is required. Transistor Q9 with the addition of an external capacitor provides a means of ac pulse triggering to turn off the Q3 and Q4 pull-down combination.

The use of nonsaturating logic minimizes both absolute propagation delay and propagation delay variation with radiation. The use of the Schottky-clamped transistors achieves this nonsaturating logic with a minimum number of diode voltage drops and, hence, minimizes the supply

*This work was supported by the U. S. Atomic Energy Commission.

voltage requirements for a given postradiation transistor beta. The electrical design is such that the power dissipation in all functional hookups is compatible with the use of the circuit as an unpackaged beam-leaded device. Typical electrical characteristics for various hookups are given in Table 1.

As shown in Figure 2, the UDIC is capable of forming dual four-input Nand Gates with expandable input option. The conventional operation of a gate where the input variables appear on diodes CR7 through CR10 and the output is taken off the collector of Q3 is straightforward and will not be considered here. As required by the gate function, diodes CR3 and CR5 are base-emitter diodes since their high capacitance is required to quickly remove the stored charge during the turn-off of the pull-down. The fan-in diodes CR7 through CR10 are collector-base type, since the higher breakdown voltage is required with the gate input in the logical one state. The uncommitted base forcing resistors are intended to minimize power if only one gate is required.

A Free-Run Multivibrator (FRMV) can be formed with the UDIC and two external timing capacitors, as shown in Figure 3. The circuit operation is conventional in that one capacitor is being recharged by the active pull-up while the other capacitor is timing into the base of the opposite pull-down. The diode CR3 in series with the base of the pull-down prevents base emitter breakdown in either Q3 or Q4 and, more importantly, it prevents the base-emitter bypass resistors from influencing the timing equation. A Schottky diode CR1 is inserted in series with the active pull-up in order to remove timing equation dependence on the logical zero-voltage level which would otherwise exist. The half period timing equation is given by

$$T = R_3 C_T \ln 2.$$

Figure 4 shows the UDIC version of a Single-Shot Multivibrator (SSMV). This function requires the addition of an external trigger capacitor and an external timing capacitor. When power is applied to the circuit, Q3 and Q4 will be turned "on" due to the difference in base-emitter voltage drops between the Q and $\overline{Q}$ side. In the quiescent state, the $\overline{Q}$ side is held off by the cross-coupled CR11 diode. During the static state the C_T timing capacitor will be charged by the $\overline{Q}$ active pull-up. Prior to the initiation of the Single-Shot, a positive going pulse on the trigger line will have charged the C_{IN} input capacitor by way of the R 13 path into the Q side. The Single-Shot will trigger on the falling edge of the trigger pulse, at which time the voltage on C_{IN} will couple through Q9 introducing a negative voltage transient on the base of Q3 and Q4. This negative base voltage causes the Q side to turn off, thus releasing the cross-coupled diode CR11 which enables $\overline{Q}$ to turn on. This dynamic state exists until the timing capacitor C_T has timed out by reaching the base cut-in threshold of the Q side. When this occurs, the SSMV returns to the static state and C_T is recharged. The timing equation for the UDIC Single-Shot is the same as previously given for the Free-Run Multivibrator. The

resistor R 13 is necessary to limit the current from the trigger source, which must be sunk by Q3. Resistor R 24 limits the current which must be sunk by Q3. Resistor R 14 limits the current which must be sunk by the trigger source after trigger application.

The Pulse Triggered Binary (PTB) function of the UD1C is shown in Figure 5. A Direct Set (S_D) or Direct Clear (C_D) can be obtained by applying a logical zero to the fan-in diodes on either side. The two sides of the PTB are dc cross-coupled such that one or the other is on. The information on the Set (S) and on the Clear (C) steering lines must be complements of one another. For the purpose of explanation we shall assume that the Q side and S line are at a logical zero. To change states, a positive clock pulse must be applied to charge C_{IN} by way of R 13 and the logical zero on S. The trailing edge of the clock pulse will trigger the PTB exactly as has been described for the SSMV. But this time the transition is into a stable state, due to the dc cross coupling, instead of a dynamic one as in the case of the Single-Shot.

A photograph of a prototype UD1C chip is shown in Figure 6.

TECHNOLOGIES

The UD1C, presently under development, utilizes six technologies: (1) radiation tolerant diffusion processes, (2) dielectric isolation, (3) silicon chrome thin film resistors, (4) beam-lead construction, (5) Schottky transistors, and (6) MNOS capacitors. To our knowledge, the UD1C is the first integrated circuit to combine all the above technologies. All active devices in the UD1C are individually isolated to minimize perturbation and to eliminate burnout caused by exposure to a high intensity gamma environment. On each chip are located two diagnostic transistors (Q11, Q12) to be used for pre-irradiation screening of the UD1C.

DATA

At this writing a preliminary evaluation of the UD1C's response to neutron radiation has been completed. Figure 7 is a plot of h_{FE} vs. neutron flux for the diagnostic transistors. Figures 8 and 9 present a typical response of the gate circuit as a whole to neutron flux. In generating the data for Figure 9, a value of 0.5 volts for maximum "on" voltage was arbitrarily selected to define circuit failure. By trading noise immunity, this value could be increased yielding an even higher radiation tolerance.

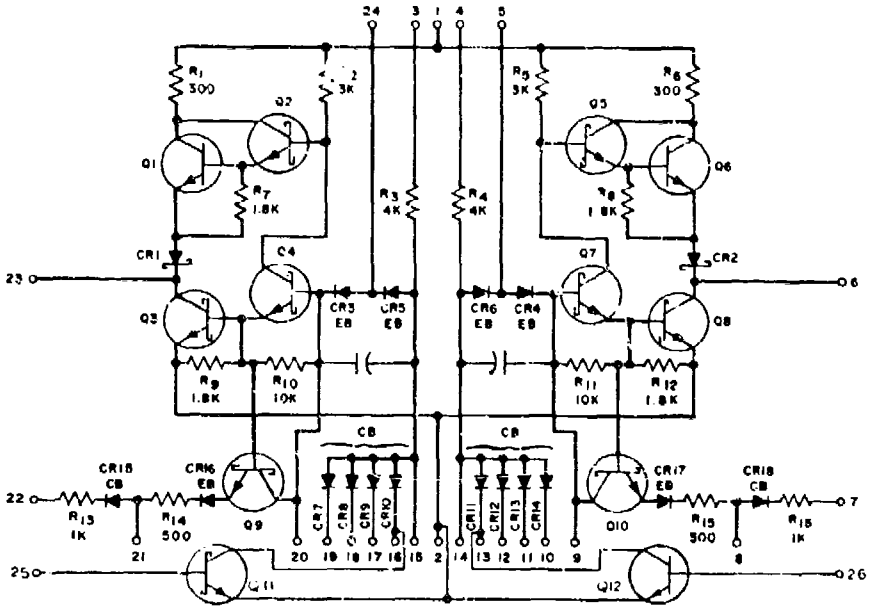
A more exhaustive evaluation of the UD1C is under way. Data from this evaluation showing the behavior of the UD1C in various function configurations under radiation will be presented at the conference.

ACKNOWLEDGMENTS

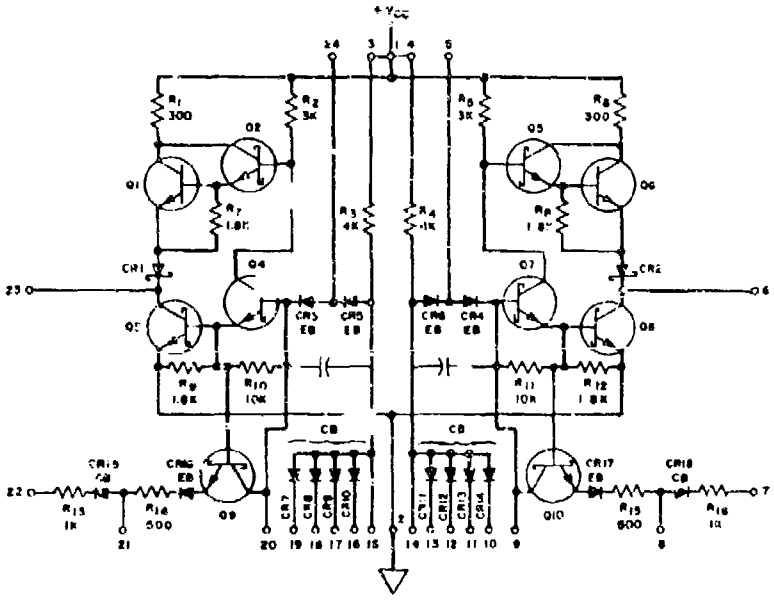
The process development necessary to realize the UD1C was performed at Texas Instruments. We wish to thank Tim Smith and his staff for their excellent work. We also thank Grayson Garrett for his help in obtaining data.

Symbol	Characteristic (Unless otherwise stated: Preradiation Conditions, V_{cc} = 8V, T_A = 25°C)	Typical Value	Units
	General Electrical Characteristics for the UDIC		
V_{OH}	Output High Voltage	7.0	Volts
V_{OL}	Output Low Voltage	.3	Volts
P_{VCC}	Power Dissipation	80-120	mW
t_{pHH}	Turn-Off Propagation Delay	10	ns
t_{pHL}	Turn-On Propagation Delay	10	ns
V_{CC}	Power Supply	9.0±1	Volts
	Electrical Characteristics for the Dual Nand Gate		
V_{IH}	Input High Voltage (minimum input to guarantee output logical zero)	2.4	Volts
V_{IL}	Input Low Voltage (maximum input to guarantee output logical one)	1.[illegible]	Volts
F.O.	D.C. Fan-Out (Postradiation)	4	
	Noise Margin (2-1/2 diode drops)	1.[illegible]	Volts
	Electrical Characteristics for the FRM		
F.O.	D.C. Fan-Out (Postradiation)	3	
f_{max}	Maximum Frequency of Oscillation	5	MHz
T	Output Pulse Width for 1/3 ≤ D.F. ≤ 2/3 operation given by $T = RC_T \ln 2$, where R = 4K		
	Electrical Characteristics for the DTRMV		
F.O.	D.C. Fan-Out (Postradiation)	2	
	Maximum Duty Factor	50	Percent
	Minimum Input Trigger Worst Case Conditions: 1. Amplitude equal to 6V 2. Fall time equal to 15 ns	100	ns
	Minimum Output Pulse	100	ns
T	Output Pulse Width $T = RC_T \ln 2$, where R = 4K		
	Electrical Characteristics for the FLB		
F.O.	D.C. Fan-Out (Postradiation)	2	
	Minimum Input Trigger Worst Case Conditions: 1. Amplitude equal to 6V 2. Fall time equal to 15 ns	100	ns
f_{max}	Maximum Toggle Frequency	5	MHz

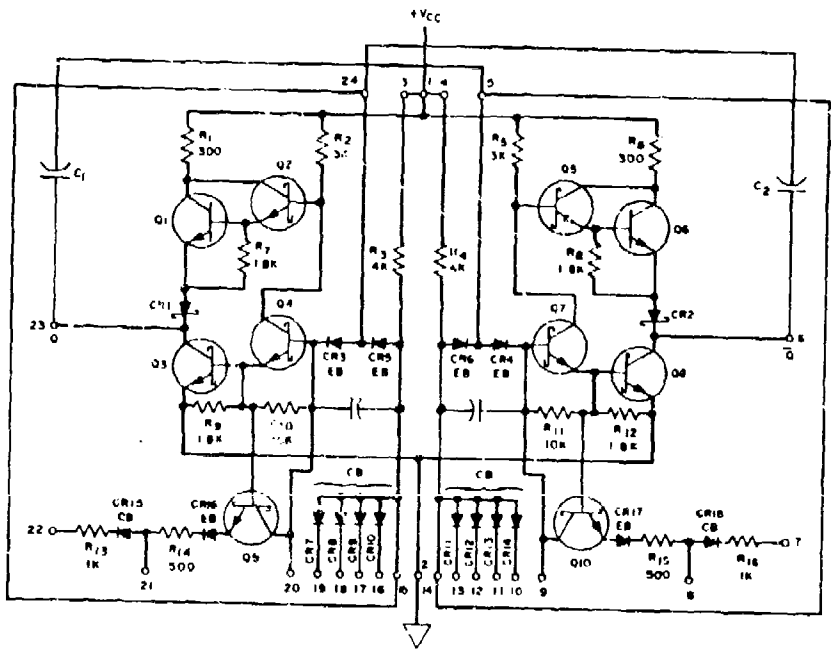
Table 1



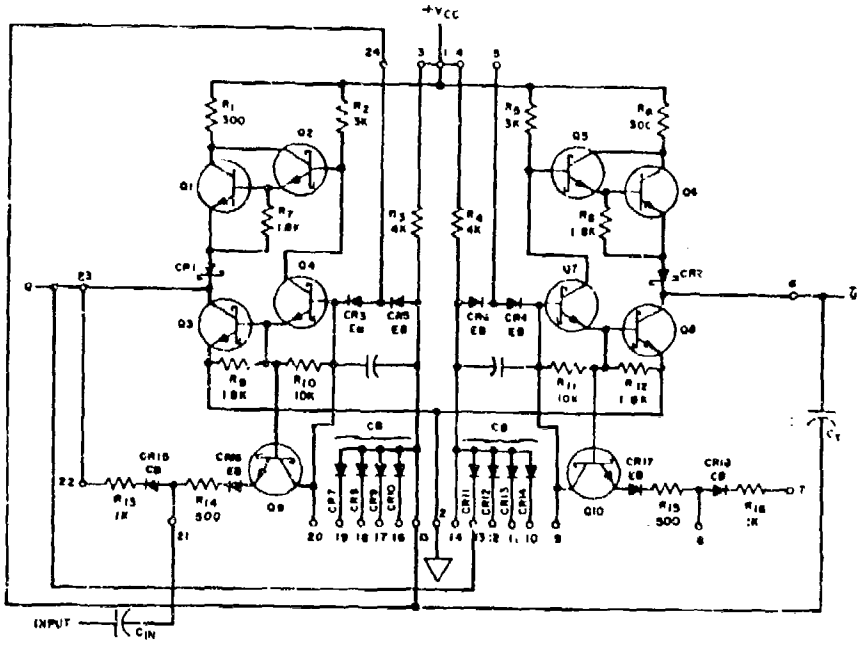
UNIVERSAL DIGITAL INTEGRATED CIRCUIT (UDIC) SCHEMATIC
FIGURE 1



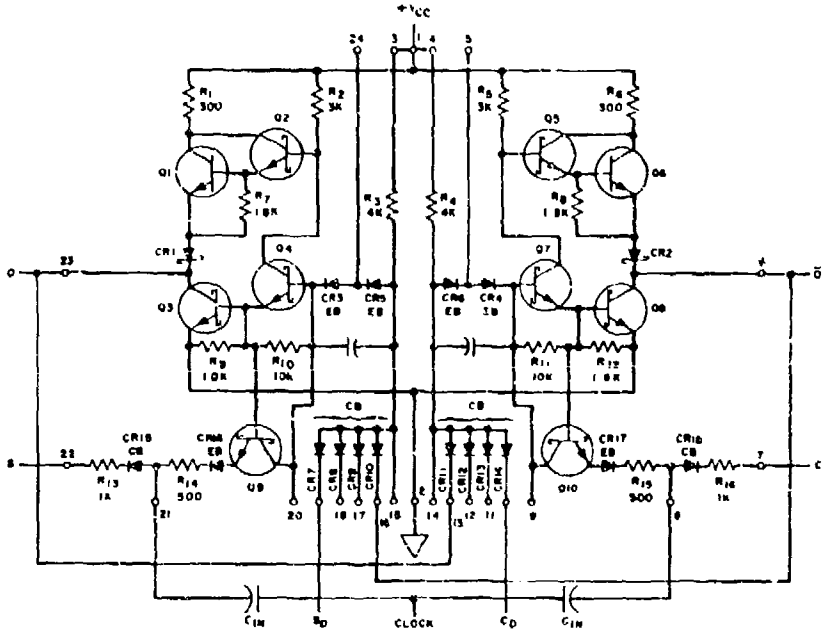
THE DUAL NAND GATE FUNCTION OF THE UDIC
FIGURE 2



THE FREE-RUN MULTIVIBRATOR (FRMV) FUNCTION OF THE UDIC
FIGURE 3



THE DIRECT TRIGGER SINGLE-SHOT MULTIVIBRATOR (DTSSM[illegible]) FUNCTION OF THE UDIC
FIGURE 4



THE PULSE TRIGGERED BINARY (PTB) FUNCTION OF THE UDIC
FIGURE 5

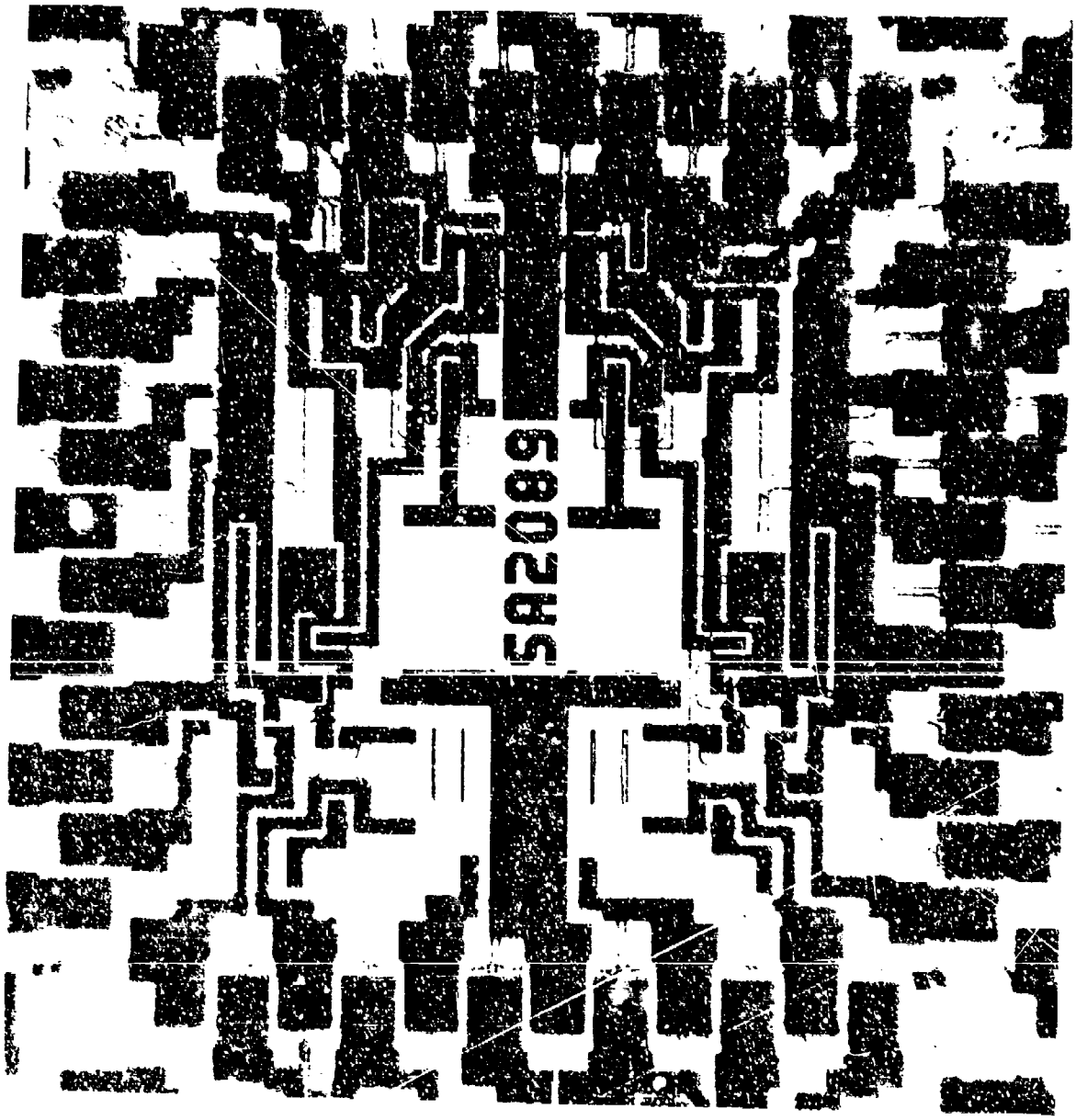


FIGURE C

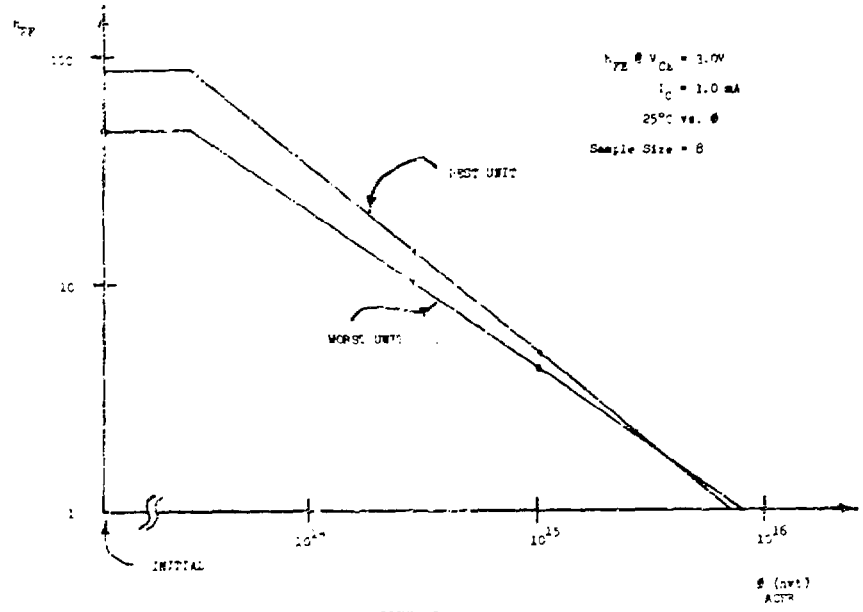


FIGURE 7

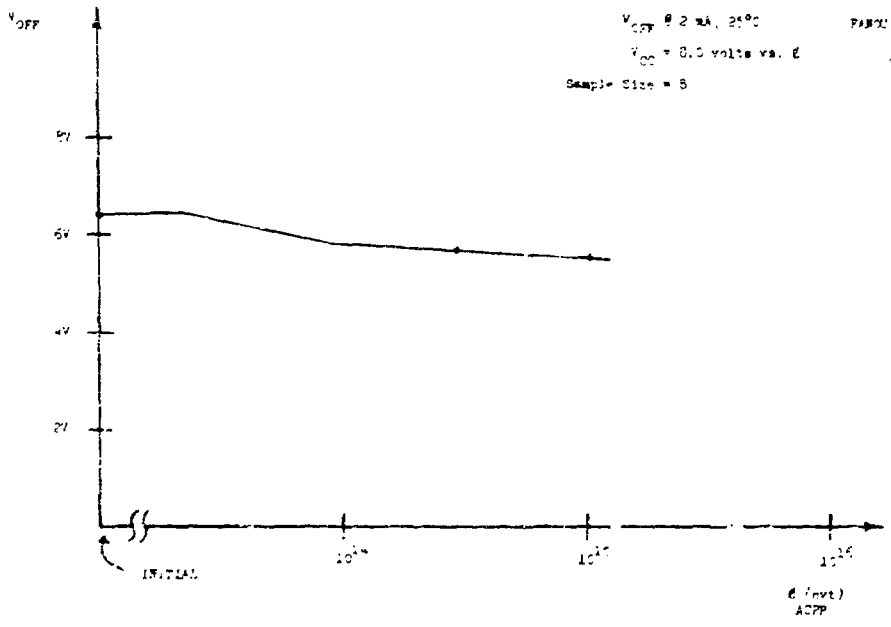


FIGURE 8

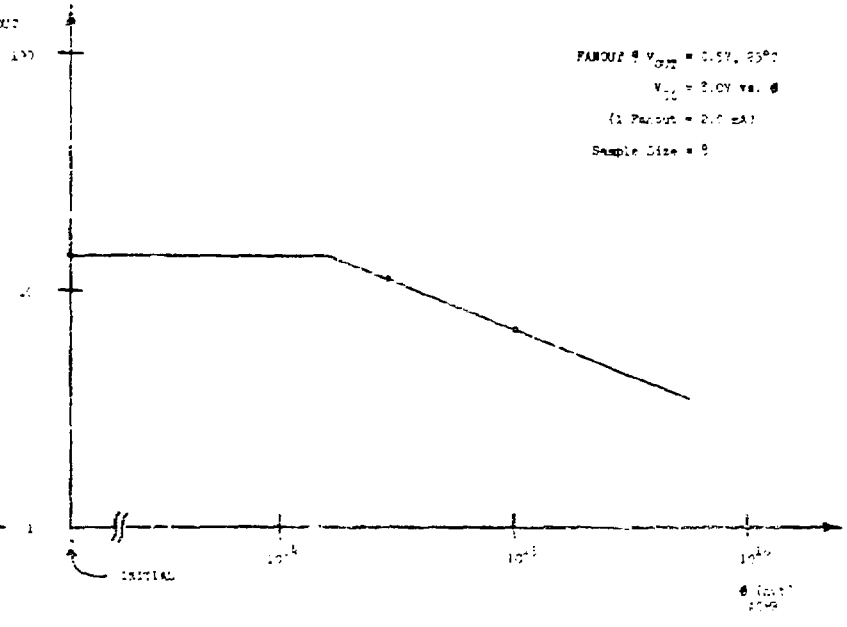


FIGURE 9

RADIATION TOLERANT GATED VIDEO AMPLIFIER*

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ABSTRACT

The circuit described is a radiation tolerant, gated, differential video amplifier. The amplifier is an all PNP design realized in monolithic integrated circuit form, featuring dielectric isolation, thin film resistors, and gold beam leads.

INTRODUCTION

This paper describes a video amplifier, designated the SA1958, which is designed to give reliable performance after an exposure to a severe neutron and gamma environment. The SA1958 is versatile in that it is a differential amplifier capable of cascade limiting and of being gated by current sinking logic.

In addition to describing the amplifier, this paper discusses the transient neutron and gamma hardening employed in the design. Conventional radiation hardening processes of dielectric isolation and thin film resistors are utilized. Data are presented to demonstrate the amplifier performance after neutron irradiation and over temperature. To the knowledge of the authors, the SA1958 represents the first radiation tolerant linear integrated circuit to be realized with gold beam leads.

SYSTEM REQUIREMENTS

The system requirement was for three separate circuit functions (1) a differential input-output video amplifier, (2) a hard limiter, and (3) a gated amplifier. In addition to operating over the full military temperature range, the circuit functions were required to operate shortly after an exposure to a severe radiation environment. All integrated circuits in the system were required to be gold beam leaded due to package density requirements and improvement in reliable component attachment within the hybrid microcircuit. Because of the inherent characteristics of the differential pair configuration, it was feasible to design a single amplifier, the SA1958, to perform all three circuit functions required by the system.

*This work was supported by the U. S. Atomic Energy Commission.

CIRCUIT DESCRIPTION

To operate the circuit as an amplifier, the terminal pins are connected as shown by the dashed lines in the amplifier schematic in Figure 1. The differential input stage consists of matched Darlington connected pairs (Q5-Q6) and (Q7-Q8). The maximum gain of the amplifier is ideally determined by the ratio of the load resistor R2 to the effective emitter resistor, which is R12 + $2r_{e6}$. When an exposure to a neutron environment results in severe beta degradation, the Darlington input connection is necessary to (1) maintain an adequate input impedance suitable for cascade operation, (2) minimize the degradation of amplifier voltage gain, and (3) decrease the effect of reduced current gain on the limit level.

Emitter followers consisting of the pairs (Q1-Q2) and (Q3-Q4) are used to buffer the output in order to enable the amplifier to drive its worst case cascaded input impedance. Again the Darlington connection is required to insure a low output impedance and to keep load variation from influencing the gain of the amplifier.

Current used to bias the output stage is summed by R10 and R15 and reused to provide bias for a stable voltage source consisting of a zero TC reference diode CR18 and resistors R25 and R26. The system requirement for a limiter necessitated a constant current source design which was independent of power supply voltage. The values of R25 and R26 are such that the effect of the Darlington base current required by Q11 and Q12 is negligible preradiation to postradiation. Base emitter diodes CR19 and CR20 are intended to track the base-emitter drops of Q11 and Q12 over all environments. Therefore, the portion of the reference diode voltage which appears across R25 by voltage divider action will also appear across R21 and set the emitter current of the Q11-Q12 Darlington pair. This emitter current is approximately equal to the collector current, which is the bias current for the amplifier.

A voltage sensitive current switch (Q9-Q10) appears in series between the constant current source and the amplifier. If the gate diode CR15 is at the logical zero level, then the current of the constant current source is switched from the amplifier through CR15 into an external current sinking logic gate. Without bias current, the amplifier is shut off and the quiescent output level falls to near the negative supply voltage. The Darlington configuration is employed for the current switch to avoid a decrease in the bias current of the amplifier after irradiation. In order to realize the gated function, the design seemed to favor an all PNP circuit in terms of power and simplicity.

The SA1958 design is capable of cascaded limiting in that the input terminals of the amplifier can accept and amplify the full output of a similar device without zero crossing distortion in the output waveform. In the limiter application, the constant current is switched between the input pairs (Q5-Q6) and (Q7-Q8) by the input signal. The

design is such that with a differential input signal equal to the maximum output swing the amplifier does not saturate and thus results in a good high frequency limiter.

The electrical characteristics of the SA1958 are shown in Figure 2. For the designed application, the amplifier was ac coupled at both its input and output terminals. The upper frequency response can be controlled by placing a capacitor between the collectors of Q6 and Q7. By controlling the high frequency response at the load resistors (R5 and R6), stable performance is assured preradiation to postradiation. The low frequency response, determined by the input coupling capacitors and the input impedance (Z_{IN}), will vary under radiation conditions since Z_{IN} changes. With the gain select terminals open, the amplifier has a voltage gain of 10 dB; with the terminals shorted it has a gain of 20 dB. Any gain between 10 dB and 20 dB can be obtained by connecting the appropriate resistor between these two pins.

By applying a digital waveform to the gate of the amplifier hookup shown in Figure 1, an input waveform can be sampled. More complex gated functions can easily be formed with the SA1958 since the bias and load terminals both are left uncommitted. For example, with the interconnects shown in Figure 3 two or more input channels can be multiplexed together.

The extensive use of Darlington pairs along with the inherent nature of the differential amplifier configuration insure operation after exposure to a neutron environment where the individual transistor current gain, beta, has degraded to five. Recovery from gamma transient generated photocurrents is aided by the use of compensation diodes shown by the dark heavy lines in Figure 1. Ideally, all the photocurrent generated in the collector base junction of each respective transistor would equal the photocurrent generated in the compensating diode. This compensation technique prevents excess current from flowing into the base terminal which when multiplied by beta could cause device saturation.

INTEGRATED CIRCUIT TECHNOLOGY

For any integrated circuit that is to withstand severe gamma radiation, the use of the dielectric isolation process is required. In the SA1958, dielectric isolation of all active devices is utilized to eliminate the possibility of photocurrent induced latch-up or burnout which might otherwise result if junction isolation were employed. Due to photocurrent generation in diffused resistors, the SA1958 utilizes nichrome thin film resistors in those positions where current limiting is necessary to prevent device burnout during a transient gamma exposure.

In addition to the hardening which is apparent on the schematic, the neutron tolerance is greatly increased by using a thin base transistor geometry. The amplifier performance variation is minimized from preradiation to postradiation conditions by gold doping the transistors.

The development of the SA1958 circuit demonstrated that dielectric isolation, gold doped PNP transistors, passivated thin film resistors, and gold beam leads can be used simultaneously to produce radiation tolerant amplifiers for hybrid circuits.

CIRCUIT PERFORMANCE

The circuit parameters, input impedance and voltage gain demonstrate the postradiation performance of the SA1958. Expressions which describe these parameters as a function of β are given by equations (1) and (2).

$$Z_{IN} \cong [2(\beta_D + 1)(R_{12} + r_{eD})] \,||\, R_{28} \tag{1}$$

$$A_V \cong \frac{R_2}{\left(\frac{\beta_D + 1}{\beta_D}\right)\left(R_{12} + r_{eD}\right) + R_S/\beta_D} \tag{2}$$

where $\beta_D \cong \beta_5\beta_6$, the Darlington effective current gain and

$r_{eD} \cong 2r_{e6} = \frac{2kT}{qI_{E6}}$, the Darlington effective small signal emitter resistance.

As shown in the above expressions, Z_{IN} and A_V decrease directly as a function of β degradation. Measured data for Z_{IN} and A_V as a function of neutron exposure are shown in Figures 4 and 5. These A_V data represent the worst case degradation since R_S, the source resistance, was at the maximum expected value. The largest source resistance occurs when the amplifiers are cascaded. R_S is then the output impedance of the preceding stage which increases as a function of radiation.

In the specified operating temperature range, the circuit performs well within the ±1 dB voltage gain tolerance. These results are depicted for a typical device in Figure 6. A_V decreases with increasing temperature primarily because of the temperature dependence of r_{eD}. Since the amplifier which generated these curves was operated in the 20 dB gain mode, the curves represent the maximum temperature sensitivity of the voltage gain. When the amplifier is operated in the 10 dB gain mode, the larger resistor in series with r_{e6} reduces the overall temperature sensitivity.

ACKNOWLEDGEMENT

The process development required to fabricate the SA1958 amplifier was performed by Motorola.

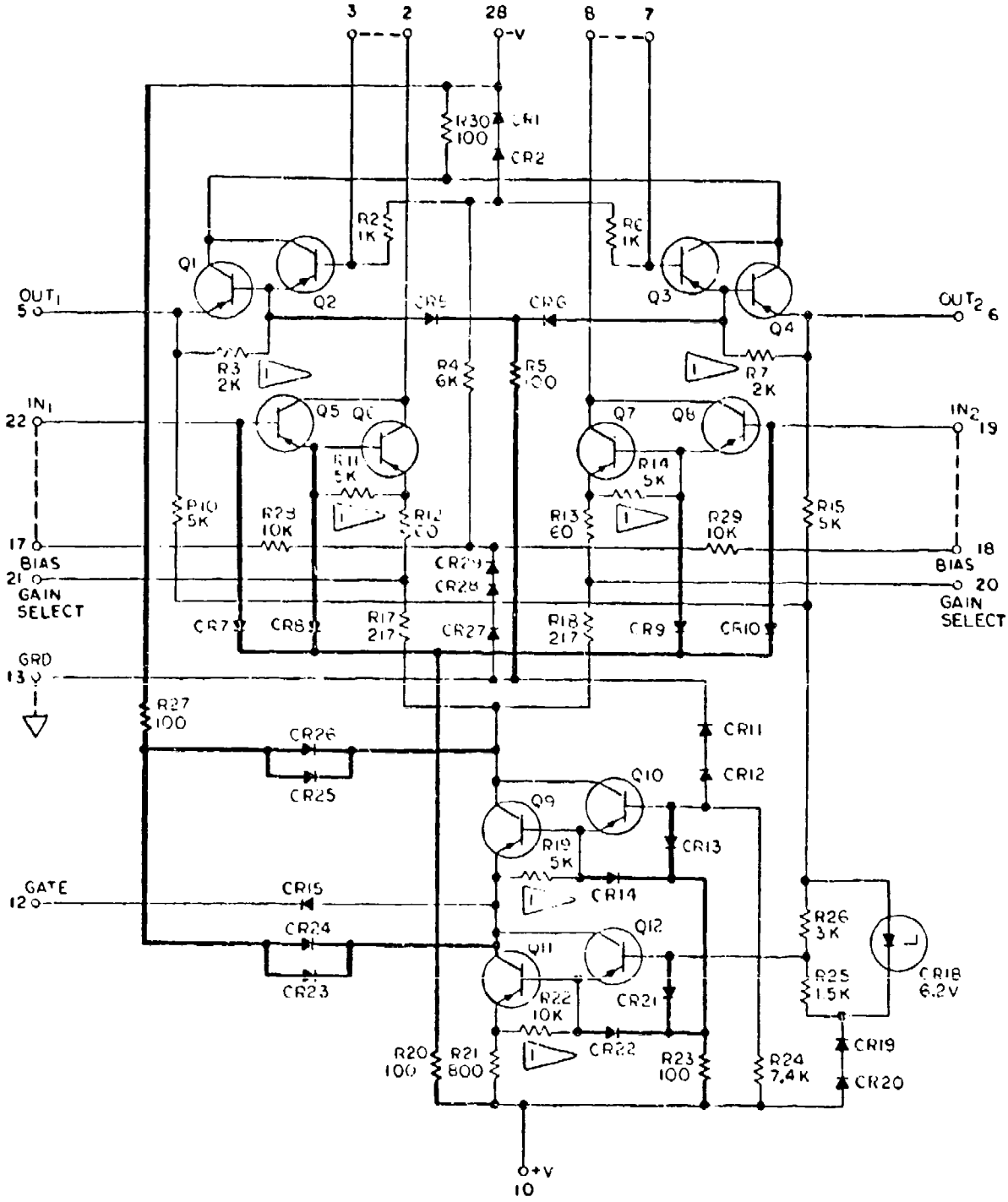
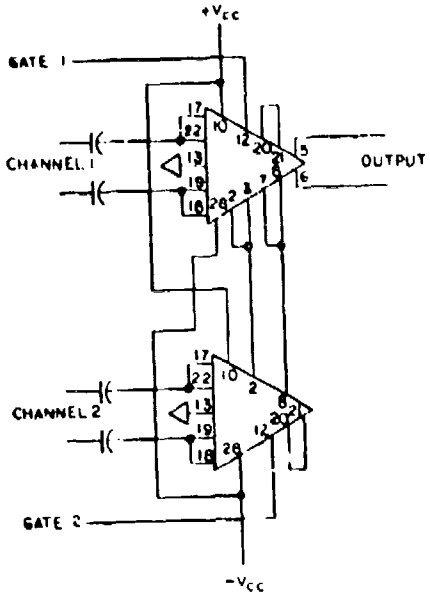


FIGURE 1 ELECTRICAL SCHEMATIC OF THE SA1958 AMPLIFIER

CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
Amplifier Voltage (+ and -)	9	10	11	V dc
Max. Input Voltage (Differential)		6		V pp
Output Voltage Swing (Differential) (R_L = 2k)		6		V pp
Voltage Gain (Differential)	-19.5*	21		dB
Voltage Gain Variation with Temp.		±1		dB
Bandwidth		15		MC
Input Impedance	5*	10		k Ohms
Output Impedance		50		Ohms
Input Voltage (Quiescent)		-2.5		V dc
Output Voltage (Quiescent)		-4.3		V dc
Power Dissipation (Single Amplifier)		160		mW
Rise Time		20		ns
Fall Time		20		ns
Channel - Select Time (Gate to Output)		25		ns
Operating Temperature Range	-25	25	125	°C
Common Mode Rejection Ratio (f = 2 MC)		50		dB
Input Bias Current		3		μA
Input Offset Voltage		2		mV
Gate Current Low (Gate Voltage = 0V)		3		ma

* Postradiation Parameters

Figure 2. Electrical Characteristics



MULTIPLEXER
FIGURE 3

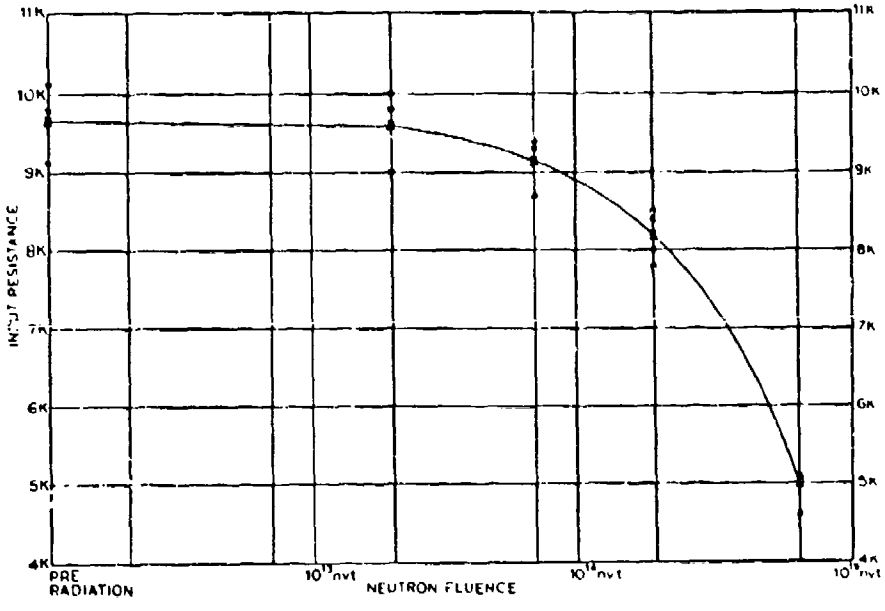


FIGURE 4 INPUT IMPEDANCE DEGRADATION OF THE SA1959 AMPLIFIER

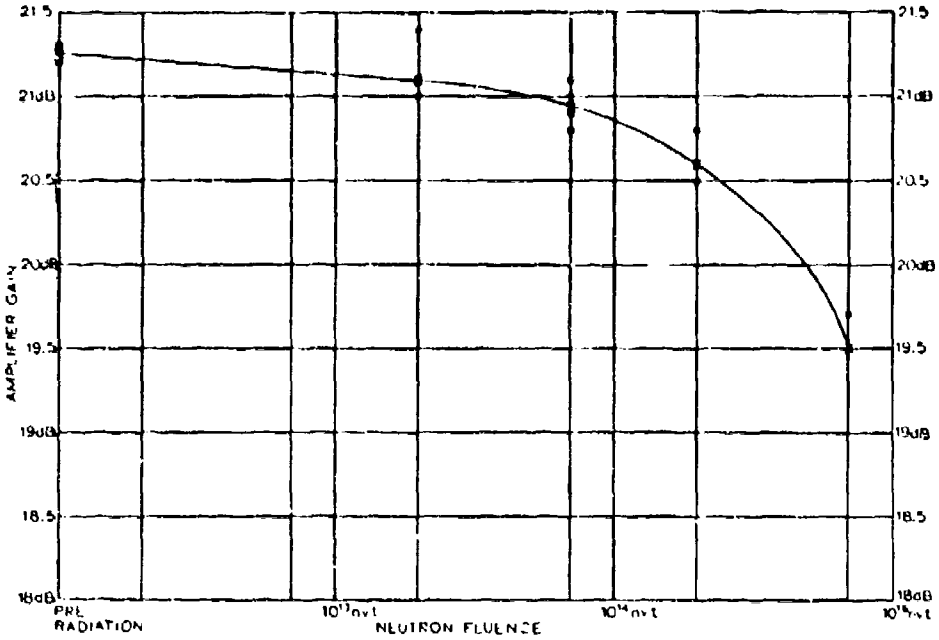


FIGURE 5 DIFFERENTIAL VOLTAGE GAIN vs NEUTRON FLUENCE

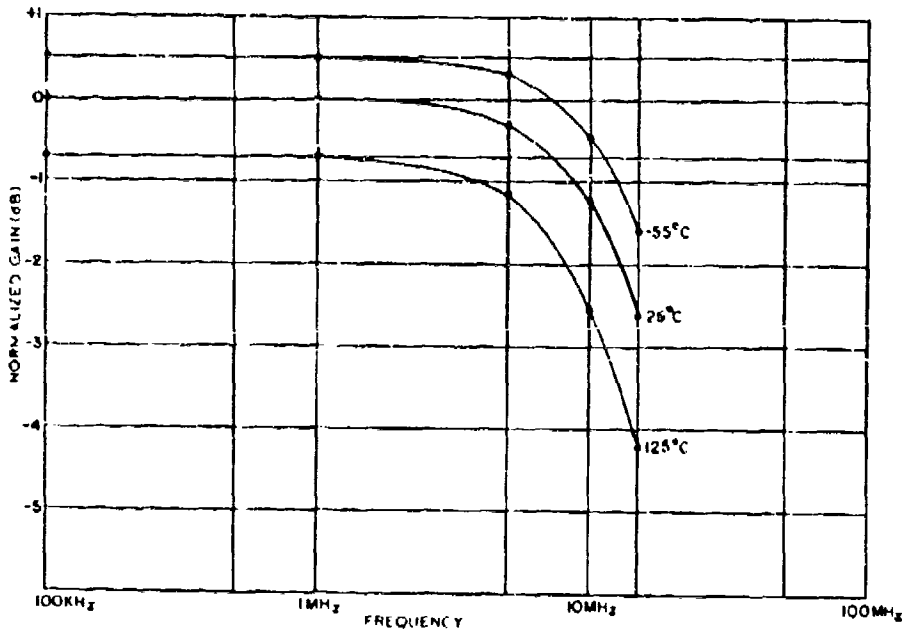


FIGURE 6 TYPICAL VOLTAGE GAIN VARIATION OF VIDEO AMPLIFIER WITH TEMPERATURE

RADIATION RESISTANCE OF COS/MOS CIRCUITS MADE WITH Al_2O_3:SiO_2 GATE DIELECTRICS*

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COS/MOS Logic Circuitry with its low power requirements, high noise immunity and high reliability is of special interest in satellite electronics. This is even more true if COS/MOS circuitry can be made immune to extremely hostile radiation environments.

A major effort at RCA was devoted to obtain this goal (1) (2) (3) (4) (5) (6). Standard COS/MOS devices under 10V bias irradiation tests show degradation at doses approximating 10^4 rads (Si)(3). The observed shift in threshold voltage and degradation of device characteristics is the result of two effects: (a) the build-up of a positive space charge in the oxide due to capture of holes in pre-existing traps in oxide near the oxide-silicon interface, and (b) the filling of interface states that were generated by the impinging radiation (5). But with the RCA developed technique for achieving a high quality oxide-silicon interface for the COS/MOS process, effect (a) dominates. To prevent the build-up of states at silicon-oxide interface, a modification of the oxide layer is required. The following approaches were investigated to obtain improved radiation resistance:

a) Doping the SiO_2 layer with chromium (7)
b) Replacing the SiO_2 layer with Si_3N_4 (6)
c) Using a composite gate structure
P_2O_5 (SiO_2) - SiO_2 (6)

d) Replacing the SiO_2 layer with Al_2O_3 (6) (8)

- The first approach is not applicable for COS/MOS devices since irradiation with positive bias causes large threshold shifts

- Si_3N_4 directly on silicon suffers from severe interface instability problems (6)(6) and as of today these devices are not useful.

- P_2O_5 (SiO_2)-SiO_2 layers are used to reduce bias temperature instabilities but their radiation hardness is rather low e.g. at 4 x 10^4 rads (Si) and ±10V bias the threshold shift is V_t= -2V (6)

*Work performed in part under the sponsorship of the NASA M.S.F.C. (NAS8-26311)

An all Al_2O_3 gate dielectric shows the highest degree of hardness to ionizing radiation potentially reaching into several megarad range (8). But to achieve reproducibility in megarad hardness, several problem areas have to be considered.

Included are:

a) Soft source-drain breakdown and source-drain leakage.

b) Gate-leakage

Work in these areas has been very encouraging, [9] but an interim solution a sandwich structure SiO_2-Al_2O_3 was investigated. Radiation-resistant COS/MOS devices operating in an environment having a gamma exposure of 10^5 rads (Si) with a bias of ±10V were accomplished. This investigation of SiO_2-Al_2O_3 sandwich dielectrics was pursued with:

a) Phase One: Al_2O_3 - SiO_2 - Si studies.

A technique for growing reproducible, thin silicon silicon dioxide layers in the range of 150Å to 500Å was investigated using the C-V technique, the optimized structure was developed and tested.

b) Phase Two: CD-4007 Device Fabrication and Testing

Based on the results of the first phase, the optimized gate sandwich structure was selected and CD-4007 devices were fabricated and computer tested. Immediately after irradiation the devices were again computer tested and the test results were analyzed.

Si - SiO_2 - Al_2O_3 Capacitors

Oxides were grown and annealed under standard RCA conditions but with growth times reduced. The thickness of the thin SiO_2 layers was measured by ellipsometry. The average SiO_2 thickness was 170, 310 and 490Å respectively with an accuracy ±10Å. The wafers were each etched immediately before Al_2O_3 deposition. Aluminum oxide layers were obtained by hydrolysis of aluminum chloride ($AlCl_3$). Aluminum was used for metalization of the capacitors.

The C-V curves were recorded before and immediately after each irradiation dose. Selected samples were biased for times equal to irradiation time, but without exposure to irradiation. This was performed to confirm that the shifts in the C-V curves were due to irradiation. Radiation testing was performed at the Cobalt 60 facilities of the Industrial Reactor Laboratories in Plainsboro, New Jersey. The dose rate at the site of the devices was measured with calibrated air ionization chambers. The time of exposure of the devices was monitored and the accumulated dose was calculated by using the known dose rate. The flat band voltage of the MIS capacitors obtained from the C-V plot was in good agreement with the calculated value (11). Table I shows test results.

Based on these results, gate structures of samples 32 and 35, 170Å or 310Å of SiO_2 and 450Å of Al_2O_3 constituted the basis for the device fabrication investigations of phase-two.

The RCA CD4007 was selected as a radiation-hardening test vehicle. This integrated circuit is composed of three n-channel and three p-channel enhancement-type MOS transistors on a single monolithic chip. The transistor elements are accessible through the package terminals, providing a convenient means to construct such logic circuits as inverters, three-input NOR gate, three-input NAND gate, etc. This broad range of applications, and availability of multiple independent pairs of transistors, which enable simultaneous irradiations under different biases (e.g., 0 volts and 10 volts for n-channel and -10 volts and 0 volts for p-channel), were the main reasons for its selection as the test vehicle. Figure 1 is a schematic diagram of the CD4007. Figure 2 shows a topological view of a completed CD4007 integrated circuit.

The gate structure composed of 170Å of SiO_2 and 500Å of Al_2O_3 showed no reasonable yield in meeting the CD4007 specification and it was discarded. Two lots #6 and #7 having 310Å of SiO_2 on 500Å of Al_2O_3 were processed and irradiation tested. The initial n-channel V_{TN} was + 1.1 to + 1.6V and p-channel threshold V_{TP} was -.8 to -1.25V. All devices met standard product specification requirements for leakage and breakdown.

Table II summarizes the effectiveness of the Al_2O_3/SiO_2 dielectric structure in enhancing the radiation resistance of COS/MOS devices. As anticipated, the smallest shifts occurred under zero bias and the greatest shifts occurred under the highest bias. All shifts on the p-channel unit were in the enhancement (turn-off) direction. The n-channel units moved in the depletion (turn-on) direction at zero and ten volts but shifted in the enhancement direction at five volts. The data represent an improvement in the radiation tolerance ofCOS/MOS devices of almost two orders of magnitude.

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TABLE I

IRRADIATION TEST RESULTS OF SiO_2-Al_2O_3 MIS CAPACITORS

SAMPLE NO.	Thickness SiO_2 Å	Thickness Al_2O_3 Å	Flatband Voltage VFB Calculated (V)	Flatband Voltage VFB Measured (V)	IRRADIATION CONDITIONS Dose Rads (Si)	IRRADIATION CONDITIONS Bias (V)	VFB (V)
25	310	1084	-	-2.4	6×10^4 1×10^5 2×10^5	+ 10 + 10 + 10	- 1.0 - 1.6 - 3.1
28	490	445	-2.25	-2.8	6×10 1×10^5 2×10^5	+ 10 + 10 + 10	- 1.2 - 1.9 - 3.7
32	170	445	-.635	-1.7	1×10^5 2×10^5	+ 10 + 10	- 0.3 - 0.9
33	170	900	-1.65	-1.6	1×10^5 2×10^5 1×10^5	+ 10 + 10 - 10	- 2.4 - 4.0 + 2.2
35	310	445	-1.34	-2.3	1×10^5 2×10^5 1×10^5	+ 10 + 10 - 10	- 0.7 - 1.1 - 1.1
36	310	900	-	-2.4	1×10^5 2×10^5 1×10^5	+ 10 + 10 - 10	- 1.8 - 3.8 - 0.4

TABLE II

	Dose (Rads (Si) Bias (volts)	Threshold Voltage Change V_T 5×10^4 (V)	1×10^5 (V)	2×10^5 (V)
N-Type Channel	0	0	(-.1) (-.2)	(- .1)
	+5	+ .1	+ .15	+ .25
	+10	(-.13)	(-.15)-(-.5)	(-.3)
P-Type Channel	0	(-.25)	(-.50)	(-.7)
	-5	(-.40)	(-.75)	(-1.35)
	-10	(-.35)	(-.65)	(-1.30)

SUMMARY OF TEST RESULTS

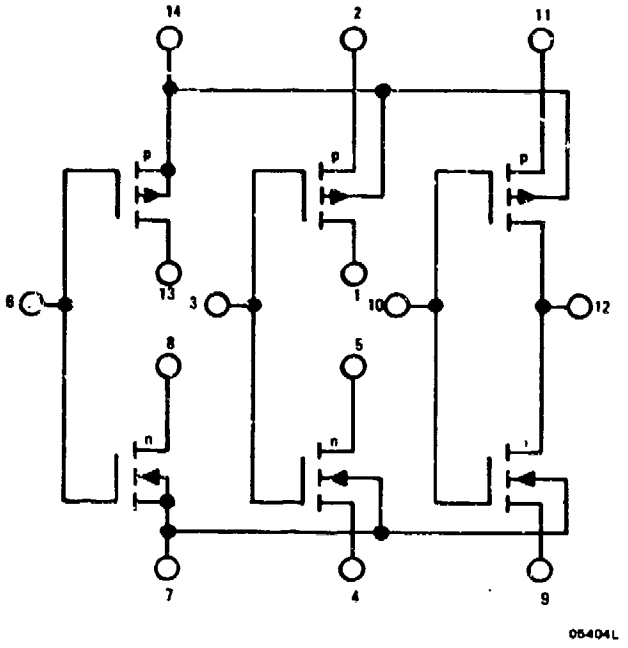

Figure 1. RCA CD4007, Schematic Diagram

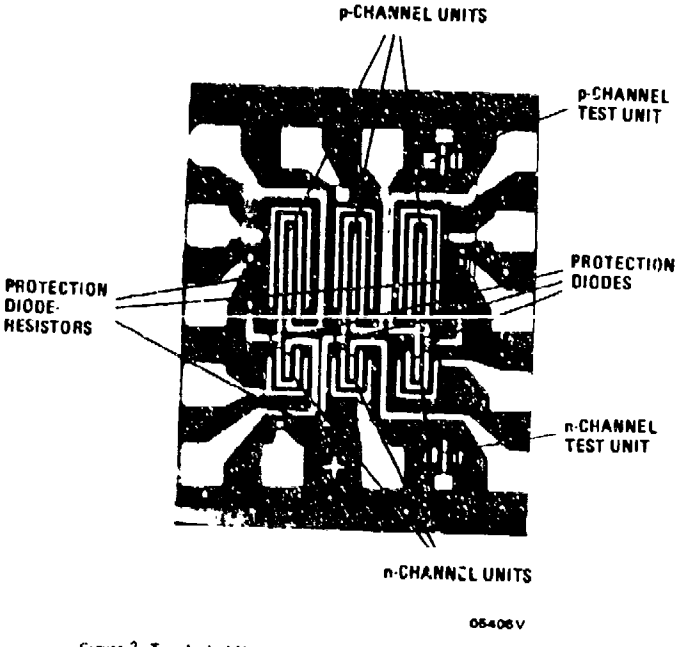

Figure 2. Topological View of Completed RCA CD4007 Integrated Circuit

LOW FREQUENCY NOISE CHARACTERISTICS OF GaAs JFETs FOR CRYOGENIC OPERATION

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ABSTRACT

Gallium arsenide junction FETs were developed for use in low noise audio frequency preamplifier circuits at cryogenic temperatures. The effects of variations in geometry, processing techniques and material parameters were investigated to reduce low frequency noise and maintain high input impedance.

INTRODUCTION

This paper describes the design and performance of GaAs JFETs which were developed for use as low noise audio frequency preamplifiers at reduced temperatures. The GaAs JFET is well suited for this application because, first, the JFET has inherently low noise, limited basically by the thermal noise of the conducting channel. Second, GaAs devices perform well at temperatures down to that of liquid helium because of the low ionization energies of commonly used n-type impurities. The input resistance, while generally not as large as an insulated gate device, will be high enough for most applications.

DESIGN CONSIDERATIONS

The design criteria in this application are primarily determined by the limit on power dissipation, nominally one milliwatt, and the necessity of keeping the preamplifier input capacitance sufficiently small. The devices are designed for use in a source follower configuration to take advantage of impedance transformation and the reduction in input

capacitance. The input capacitance is given by

$$C_{in} = C_{gd} + C_{gs}(1-G_v) + C_{stray} \tag{1}$$

where C_{gd} and C_{gs} are the gate-drain and gate-source capacitances and G_v is the circuit voltage gain. A convenient figure of merit in high impedance circuitry is the product of the equivalent input noise voltage, e_n, and the input capacitance. The gate-source capacitance is given by[1]

$$C_{gs} = \frac{3}{2}\frac{aNqLW}{V_o} F(V_{gs}, V_o) \tag{2}$$

where L and W are the gate length and width, a is the channel height and V_o is the pinch-off potential. The function $F(V_{gs}, V_o)$ is approximately 0.2 to 0.4 in the bias range of interest. A value of 0.3 is used for ease in calculation, and it is assumed that C_{gd} is approximately a constant determined by packaging. With C_{gs} proportional to area and e_n^2 inversely proportional to area[2,3], the $e_n C_{in}$ product has a broad minimum with respect to C_{gs}. Taking into account material properties, the restrictions on power and area lead to acceptable ranges of device geometry, maximum current and pinch-off voltage resulting in devices with rather small channel width to length ratios. Calculations were made for a nominal circuit voltage gain of 0.9. Typical values are a transconductance of 500 μmhos, operating current of 300 μA, C_{gs} of 3 to 5 pF and gate width to length ratios of 2 to 5. Figure 1 shows the surface configuration of one of these devices.

DEVICE FABRICATION

The devices were fabricated from vapor epitaxy material of 1 μm nominal thickness on compensated chromium doped semi-insulating substrates. Carrier concentrations are in the range of 1 to 6 x $10^{16}/cm^3$. The gate is formed by zinc diffusion to a typical depth of 0.5 μm. The source and drain metallization consists of alloyed gold-germanium.

EXPERIMENTAL RESULTS

Measurements were conducted to determine input impedance and to isolate major physical sources of low frequency noise. A current-voltage characteristic at liquid helium temperature is shown in Figure 2. Input capacitance of the preamplifier circuit alone with a voltage gain

of 0.9 is typically 1.0 pF or less for test devices mounted in TO-18 packages. Input resistance larger than 1×10^{13} ohms has been measured for temperatures near that of liquid helium. the low frequency equivalent input noise voltage spectra generally consist of an approximately 1/f region which turns into a flat region in the frequency range of 1 to 10 kHz. The flat region is presumed to be the plateau of a generation-recombination (g-r) term of the form constant/$(1 + \omega^2\tau^2)$, having a value typically two decades above the calculated thermal noise level. The magnitude of the 1/f noise at liquid helium temperature has been measured to be as low as 50 $nV/Hz^{1/2}$ at 300 Hz. Figure 3 illustrates noise spectra measured at room temperature and at liquid nitrogen and liquid helium temperatures.

Measurements were carried out to investigate the effects of variations in processing and material properties such as surface etching, annealing, contact resistance and substrate effects. Surface etching reduces noise if there is an initial significant surface leakage current. Excessive gate current which increases noise and degrades input impedance can also result from diffusion spreading which may be aided by etching. A major source of low frequency noise is found to be associated with the region near the epitaxy-substrate interface. This is illustrated in Figure 4 which shows the effect of substrate to source bias on the noise magnitude at 300 Hz and 10 kHz. The g-r noise as well as the 1/f noise appears to be associated with the interface/substrate since carrier fluctuations within the channel usually will not be significant at room temperature. At lower temperatures there may be a contribution from partially ionized impurity levels.

It is concluded from this initial development program that GaAs JFETs are useful as low noise, low frequency preamplifiers extending down to very low temperatures, and are competitive with other devices used in such applications. An additional feature of the JFET is that it is relatively resistant to radiation. Further work is concerned with better characterization of noise sources in relation to geometry and material parameters.

ACKNOWLEDGMENTS

The contributions of P. E. Friebertshauser, A. F. Behle,

S. K. Watanabe and D. T. Dion are acknowledged for material growth and device fabrication. Acknowledged also are discussions with R. Zuleeg concerning device design and analysis.

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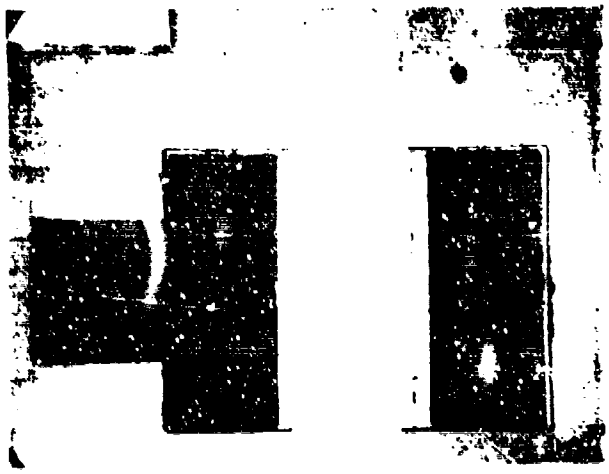

Figure 1. Photograph of surface geometry of GaAs JFET with gate dimensions of 3.5 x 8 mils.

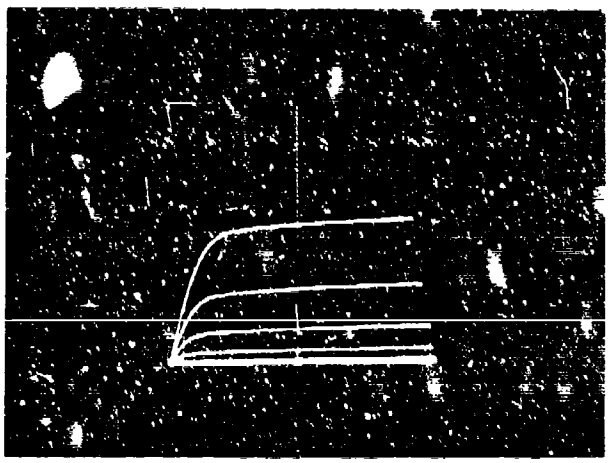

Figure 2. Current-voltage characteristics of GaAs JFET at liquid helium temperature. Horizontal scale, 1 v/div.; vertical scale, 100 μA/div.; 0.5 v/step.

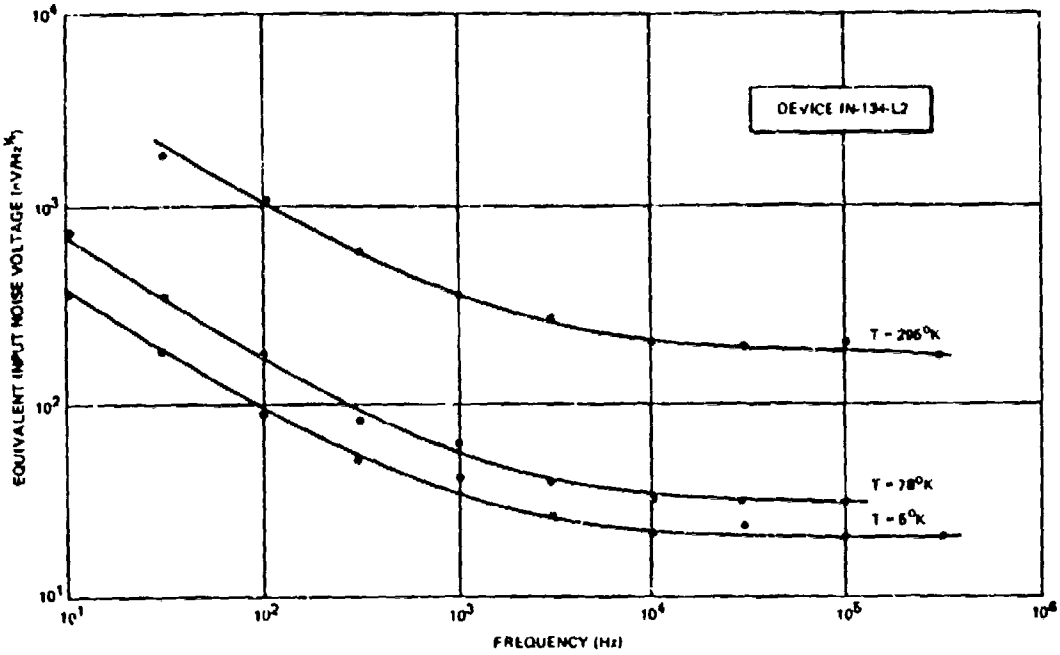

Figure 3. GaAs JFET equivalent input noise voltage spectra from room temperature to liquid helium temperature.

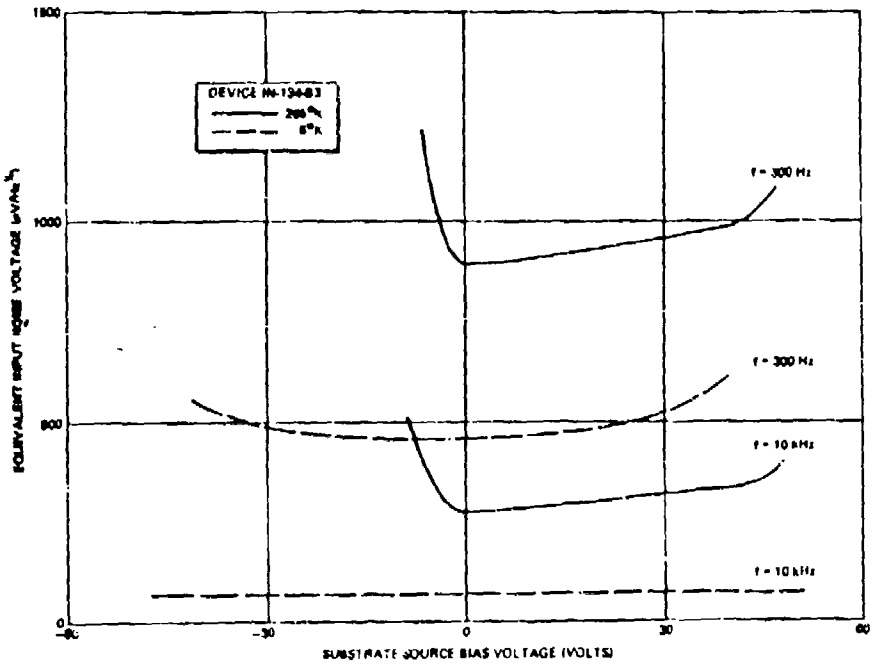

Figure 4. Effect of substrate to source bias on low frequency noise of GaAs JFET at room temperature and liquid helium temperature.

MONOLITHIC HIGH POWER MODULATOR

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ABSTRACT

The application of silicon integrated circuits to high voltage, high current drivers for GaAs Laser Diodes and microwave phase shifters has been investigated. An integrated circuit having dielectrically isolated circuits capable of shaping and timing high speed pulses with an 80 volt swing and a peak current of 10 amperes was constructed. This paper summarizes the design and results achieved with the device.

INTRODUCTION

The majority of the modulators presently used for GaAs Laser Diodes and ferrite phase shifters are either of a hybrid or discrete type. Under direction of the U.S. Army, Electronics Command, a development program to apply integrated circuit technology in the area of high voltage, high current modulation was conducted. Figure 1 is a photograph of the chip developed during this program. The goals of this development effort and the results obtained are summarized in Table I.

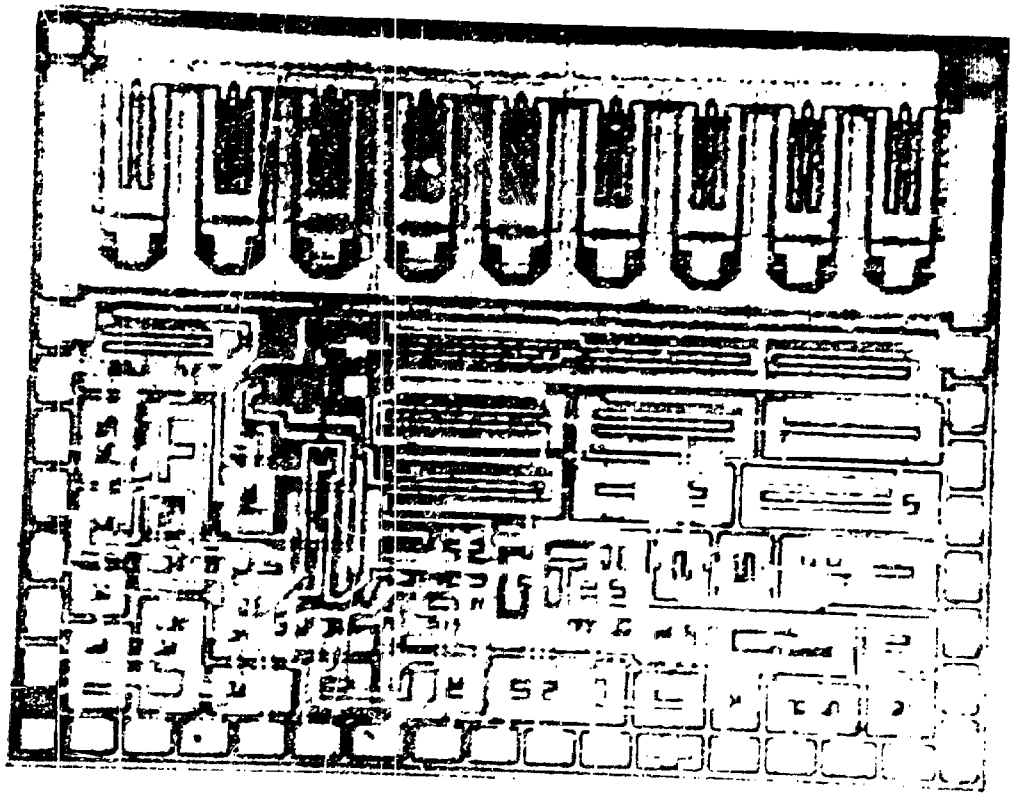


Figure 1. TA6177 Photomicrograph

TABLE I

TA6177 CHARACTERISTICS

OUTPUT CHARACTERISTICS	OBJECTIVE	ACTUAL PERFORMANCE
Output Pulse Voltage:	80 volts maximum	80-120+ volts max.
Output Pulse Current:	10 amperes max. (adjustable from 3 to 10 amperes)	10 amperes (adjustable from <1 to 10 amperes)
Output Pulse Rise and Fall Time:	Less than 40 nanoseconds	40 nanoseconds (7 ampere pulse)
Duty Cycle:	0.02 to 2.0 percent	0 to 2.0 percent
Pulse Width:	100 nanosecond to 1 microsecond	100 nanosecond to 1 microsecond
Leakage:	0.3 milliamperes	0.3 milliamperes max.
Amplitude:	Compatible with 5 volt logic	5 volt pulse
ADDITIONAL FUNCTIONS AND REQUIREMENTS		
Monostable		
Pulse Width:	Externally adjustable from 100 nanoseconds to 2 microseconds	Externally adjustable from 100 nanoseconds to 2 microseconds
Pulse Input:	A strobe compatible with 5 volt logic	5 volt strobe input

Clearly the objectives in Table I call for a monolithic design capable of simultaneous high speed, high voltage, and high current. In addition to the objectives in Table I, it was determined that maintaining low power consumption would be essential for potential applications. To meet this additional constraint, all circuits should be in the "off" state until an input pulse is received. The design developed during this program represents a unique, all monolithic, approach which maintains all circuits in the normally "off" state while meeting the performance goals.

CIRCUIT DESIGN

The final circuit configuration is shown in Figure 2. Though description of the entire circuit is lengthy, the overall pulse response and several unique circuits can be highlighted.

The circuit shown in Figure 2 responds to an input pulse by shaping it to form a constant current, high resolution pulse output. The control circuits shown also provide regulation of the output current level and isolation of the output current pulse from the power supply. To circumvent the problem of processing high resolution pulses with low performance lateral PNP transistors, a unique, though more complex, pulse processing chain was designed. In this approach, the critical PNP's are pulsed on before the required output signal is to be generated. This allows the critical PNP's to reach their full current level before their current is routed to the load device.

Transistor Q26 in Figure 2 is the critical PNP which supplies the output drive current. To obtain high resolution pulses, Q26's current is amplified by Q28 whose output is shunted to ground by Q37. Q37 continues to shunt this current to ground until the two level detectors composed of Q29, Q30, Q17, Q18, Q31, and Q32 time out. When both level detectors have switched, Q37 is driven off by Q33 allowing the current from Q28 to drive Q45 and Q46.

Transistors Q45 and Q46 are configured in a Distributed Darlington Array. This patented structure has been used successfully in several other high current integrated circuits. This structure makes extensive use of interdigitation, and ballasting to attain good current distribution. For use in this high voltage process, field plates, deep diffusions, and rounded corners were added to assure the highest breakdown voltage possible.

Another function available on this integrated circuit is a zero quiscent power consumption monostable exhibiting high speed rise and fall times. Transistors Q11, Q12, Q13 and Q14

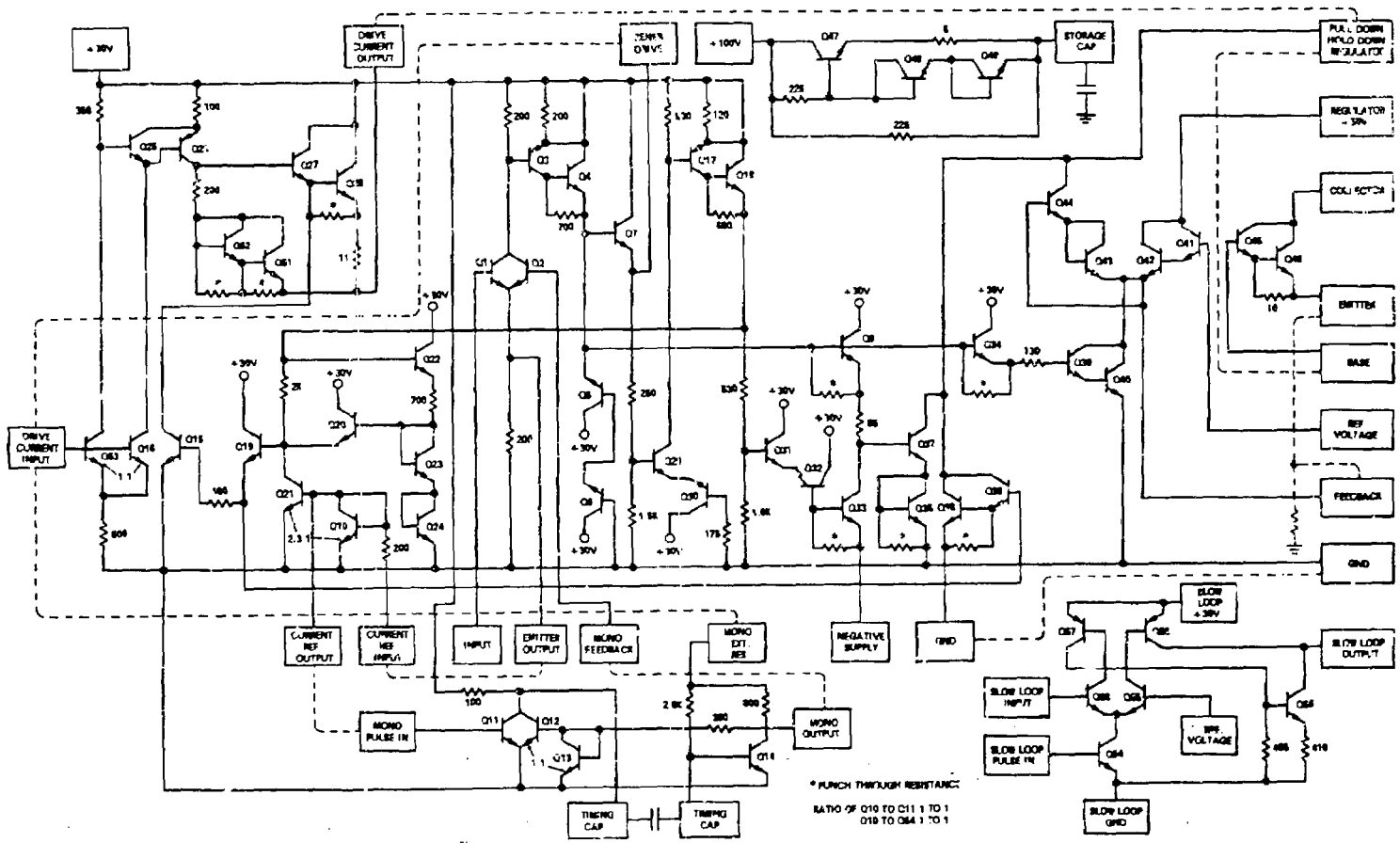


Figure 2. TA6177 Schematic Diagram

make up this unique monostable. The modulator may be configured so that either the input pulse or the monostable determines the output pulse width.

The remaining control circuits provide current regulation and isolation from the power supply. Transistors Q44, Q43,Q42,Q41,Q40 and Q39 are configured as a high current differential amplifier. With the collector of Q44 connected to the base of Q45 and the base of Q44 connected to the emitter of Q46, wide band, closed loop control over the Darlington Array collector current is obtained. Because this wide band system may be subject to oscillation, an alternate open loop regulator is provided. This configuration has both the collector and base of Q44 connected to the base of Q45. To give this open loop system the long term stability of the closed loop system, a pumped AGC network composed of Q54,Q55,Q56,Q57,Q58 and Q59 can be used to control the Reference Voltage input. Variation of the Reference Voltage to maintain constant voltage at the emitter of the Darlington Array will maintain constant collector current.

To isolate the 10 ampere constant current output from the power supply, a line isolator is provided. This circuit, composed of transistors Q47,Q48 and Q49, is essentially a constant current source. This circuit forces the Darlington Array to obtain its pulsed current from a storage capacitor and allows the power supply to supply essentially a constant lower value recharge current.

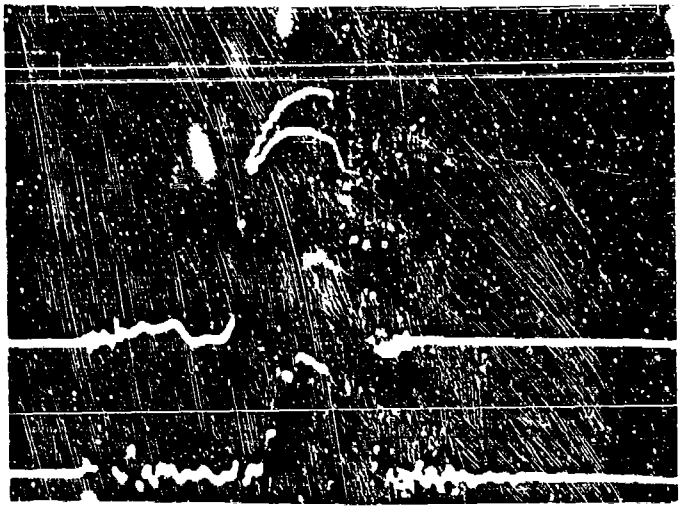
CIRCUIT PERFORMANCE

The circuit outlined above was processed by using deep pocket dielectric isolation technology. As shown in Table I all of the significant objectives of the program were obtained. The control circuit provided an internally timed 200 milliampere pulse characterized by a 35 nanosecond rise time and a 10 nanosecond fall time. The output stage exhibited a 40 nanosecond rise and fall time for a 7 ampere pulse.

The modulator system was configured with the monostable determining the pulse width, the output stage driving a resistive load, and the regulator providing open loop current control. Figure 3 is a photograph of the output current for five different Reference Voltage settings. The resistive load was then replaced by a TA 7606 Laser Diode. This particular diode had a threshold of 4 amperes and a peak forward current of 10 amperes. Figure 4 shows the detected light output for two Reference Voltage settings. Clearly, Figure 3 indicates that control over the output current level has been obtained. Figure 4 demonstrates that this current control can be translated into control over the transmitted light intensity.

Scales:
Vertical - 10 volts/cm (2 amperes/cm)
Time - 100 nanoseconds/cm
Load - 5 ohms
Reference Voltage Settings 16, 14, 12, 10 and 5 volts

Figure 3. Darlington Array Output Current for Varing Reference Voltage



Top - Current - 2 amperes/cm
Bottom - Light Output - .005 volts/cm
Time:- 100 nanoseconds/cm

Reference Voltage - 16.5 and 14.5 volts

Figure 4. Laser Current and Light Output for Varing Reference Voltages

CONCLUSION

The development program summarized in this paper leads to several significant conclusions. First, the performance obtained indicates that monolithic technology can be used for modulation of Laser Diode, microwave ferrite phase shifters, and microwave diodes, requiring high current, high voltage, and high speed. Second, the modulator developed is a compact unit which makes phase shifter arrays practical and miniature microwave or laser sources workable. Third, the ability to control the amplitude of a high resolution pulse allows both compensation and control of the drive signal as required by a potential system.

AN INTEGRATED S-BAND SOLID STATE FRONT END

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ABSTRACT

The application of microwave integrated circuit technology to radar receiver design has resulted in a compact, lightweight front end module. The unit, measuring 1.0" x 2.5" x 4.5", operates from 2.3 GHz to 2.7 GHz with a 5.5 dB noise figure and 28 dB gain.

INTRODUCTION

This paper describes a microwave integrated circuit front end that was developed as part of a modification program for an S-band radar. It represents a 60:1 improvement in system reliability compared with the discrete component device that it replaces. The size and weight have been reduced by an order of magnitude. The module features a low overall noise figure combined with the additional advantage of built-in receiver protection against high power transmitter leakage pulses. It consists of a diode limiter followed by a single-pole double-throw PIN diode switch, a 20 dB directional coupler, and a low-noise transistor amplifier. All of the components are integrated within a single housing with the limiter forming an integral part of the overall package.

Except for the limiter, which is a coaxial device, microstrip fabrication techniques are used throughout. Transmission line patterns are defined by screening high conductivity thick film gold ink onto a 0.025 inch thick, 99.5% alumina substrate. Bias resistors and transmission line terminations are formed with resistive inks in a similar fashion and then laser trimmed to within their appropriate tolerance range. Other circuit components, such as chip capacitors and semiconductor devices, are attached to the substrate either by soldering or by welding with a parallel gap welder.

BLOCK DIAGRAM AND DESIGN OBJECTIVES

A block diagram of the front end showing its individual components is illustrated in Figure 1. The module is required to work in either of two states determined by the polarity of the switch control voltage: one of these is the normal receive function and the other is a test mode that was included to permit receiver measurements to be conveniently made at the radar site. When in the test mode, isolation between the amplifier and the module's input signal terminal is accomplished by the switch, which is used to terminate the main arm of the coupler, and by applying bias to the shunt mounted limiter diodes. Including the contribution of the switch, a total isolation of 60 dB is achieved with this scheme.

Tables 1 and 2 present a summary of the principal design specifications for the module and its respective components. Throughout the design, major emphasis was placed on achieving the best reproducible noise figure possible. As a consequence, losses in front of the amplifier had to be minimized. In addition, selected low-noise transistors were specified for the first two amplifier stages. The transistors chosen for this application exhibit a maximum noise figure of 4.0 dB at 3.0 GHz. Final optimization of noise figure was accomplished by amplifier input matching.

Since the device would be produced in quantity for a military application, high reliability, low cost, reproducibility and ease of repair were essential design objectives.

The high reliability objective was attained through the use of fully qualified MIL parts. All semiconductors were JAN TX rated. Chip capacitors and resistors were tested under the environmental conditions required for the equipment as a whole. Extensive environmental testing at all levels of the design helped eliminate any defects.

The cost objective was met by the use of microstrip fabrication techniques and an emphasis on layout procedures that enabled ease of fabrication and assembly.

Since reproducibility is directly related to the quality of the design and fabrication as well as the tolerance control established, particular attention was devoted to these areas. Extensive evaluations were conducted which established standards for the thick film fabrication process. Rigid quality control criteria were established. In addition, testing at all levels of the design allowed specification of the tolerances required to yield a reproducible design.

In order to achieve the repairability objective, all substrates are clamped in place instead of using a permanent mounting method, thus allowing quick removal. Initial problems associated with substrate shifting and the connector-module interface were successfully solved.

DESCRIPTION OF INDIVIDUAL COMPONENTS

A. Receiver Protector

The limiter has to protect against a leakage pulse of 3 KW peak power with a 6 us pulsewidth and a duty cycle of 0.002. The first stage provides most of the required protection by using two high-power PIN diodes mounted in shunt across the RF line. When a high level pulse is applied at the input port, these diodes eventually bias on and act to reflect the bulk of the incident energy. Spike leakage occurring at the beginning of the pulse is significantly reduced by two pairs of quick-acting varactor diodes added behind the input stage.

All of the diodes are mounted from the inner to the outer conductor of a coaxial transmission line, with the outer conductor being the module housing. This provides an excellent heat sinking capability and also makes diode removal relatively easy. Both the spacing of the diodes and the impedance of the transmission line are regulated to provide a good match.

Measured data for the limiter is presented in Figure 2. The entire module was field tested to 3.3 KW with no apparent degradation to small signal performance.

B. SPDT Switch and Directional Coupler

Both of these components, including biasing networks for the switch, are fabricated on a single substrate that is 1 inch long by 2 inches wide. Low level PIN diodes are used to provide the switching function. Obtained in a beam lead configuration, they are attached to the microstrip circuit through the application of parallel gap welding techniques. Those located in the signal arm of the switch were chosen for their low series resistance and package lead inductance in order to minimize transmission loss. The directional coupler is a conventional microstrip design employing a parallel section of coupled line which is a quarter-wavelength at the design center frequency.

Typical performance curves for the switch-coupler combination are given in Figure 3. The units typically exhibit an insertion loss of less than 0.7 dB across the band.

C. RF Amplifier

A cascade arrangement of five common emitter transistor stages is used to achieve 27 dB minimum gain and a typical noise figure of 4.2 dB. This circuit, with attendant biasing and matching networks, is contained on a 2 inch by 2 inch substrate. The transistors are housed in a small, hermetically sealed stripline package and mounted in a hole through the substrate. The first two stages are biased for low-noise operation and the next two for maximum power gain. Together, these four stages are used to determine amplifier performance with the last stage serving as a buffer to provide load isolation and the required output match.

The first step in the development was an approximate Smith Chart design carried out from data supplied by transistor two-port scattering parameter measurements. Computer-aided design techniques were then applied to optimize the matching networks of the resulting circuit. A flat gain response is obtained by designing the matching structures to provide a low VSWR at the highest operating frequency, and then roll off in match at lower frequencies where transistor gain is higher. During the design procedure, it was determined that the amplifier is unconditionally stable throughout its operating band, but becomes unstable for frequencies lying in the UHF region. Appropriate circuitry was, therefore, added to the design to remedy the problem. The modification produced stable transistor loading conditions at lower frequencies, yet had a negligible effect at S-band. Slight changes to the matching networks were made during breadboarding and subsequent testing to arrive at a final mask design. The gain and noise figure of a typical amplifier are given in Figure 4.

MODULE RESULTS

The prototype version of the integrated front end (Figure 5) met all the design requirements presented earlier. The final test results for a sample of fifteen production units is given in Table 3. All of the specifications have been met. The reliability record accumulated under actual field operating conditions has been impressive. To date, over 15,000 hours of operation have been logged without a failure. The uniformity experienced during the initial production run demonstrates the effectiveness of the approach used to attain this level of reproducibility.

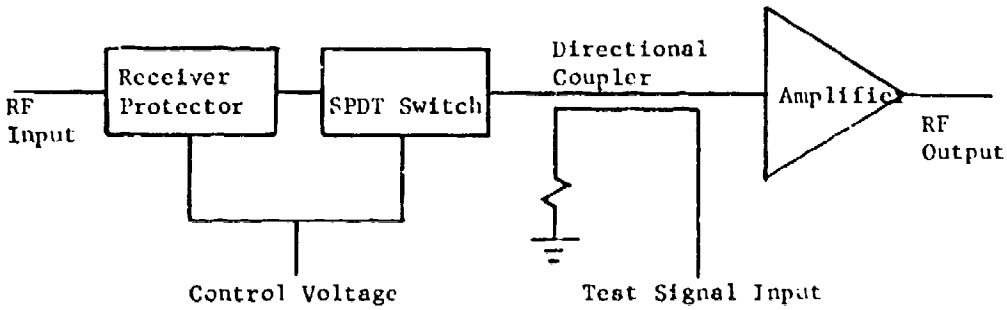


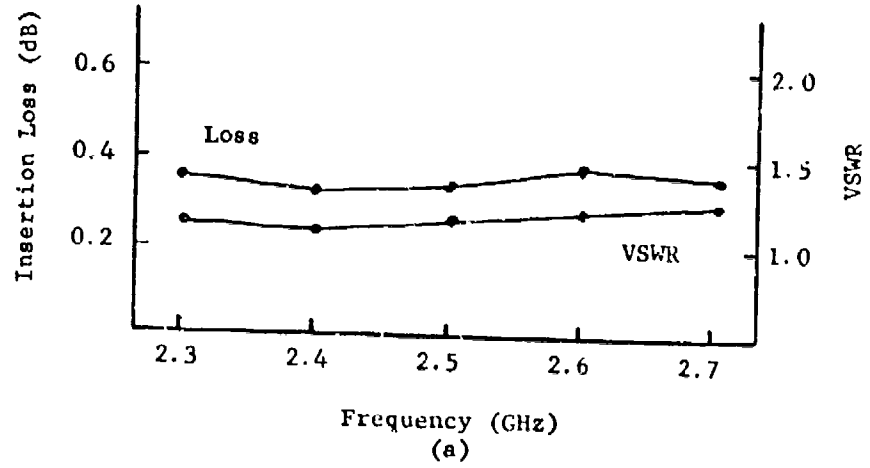
FIGURE 1: Module Block Diagram

Characteristic	Specificat.
Frequency (GHz)	2.3 to 2.7
Gain (dB), min.	25
Gain Flatness (dB)	±0.5
Noise Figure (dB), max.	5.5
VSWR	
Input	Noise Matched
Output, nominal	2.5:1
RF Input, max.	3 KW peak, 6 W ave.
Test Mode Isolation	
Amplifier to RF	
Input Port (dB)	60
Temperature (°C)	-10 to +52

TABLE 1: Module Specifications

Characteristic	Specificat.
Receiver Protector	
Ins. Loss (dB), max.	0.3
Limiting Threshold (dBm)	+10
Switch	
Ins. Loss (dB), max.	0.4
Isolation (dB), min.	25
Coupler	
Ins. Loss (dB), max.	0.2
Coupling (dB)	20
Amplifier	
Gain (dB), min.	27
Noise Figure (dB), max.	4.5

TABLE 2: Component Specifications



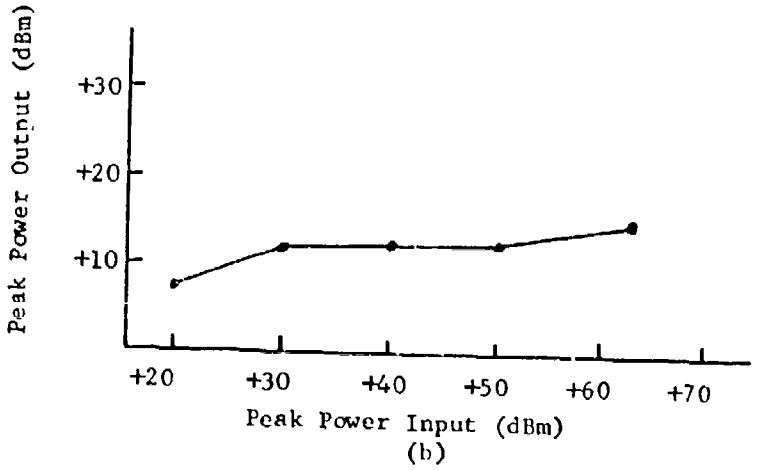


FIGURE 2: Limiter Response

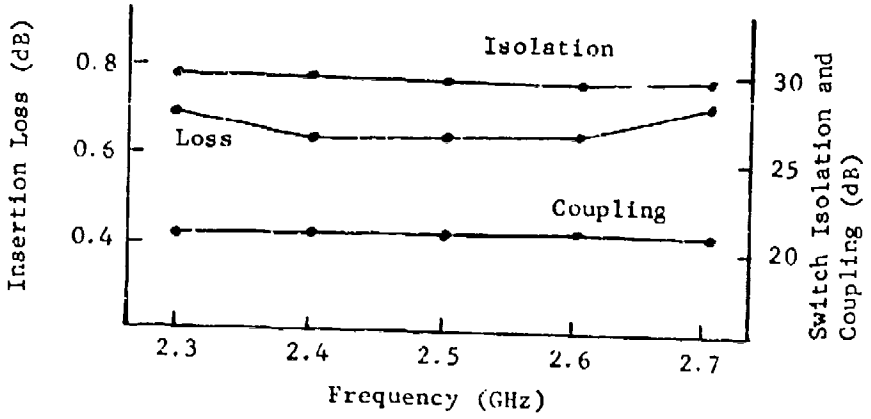


FIGURE 3: Switch-Coupler Response

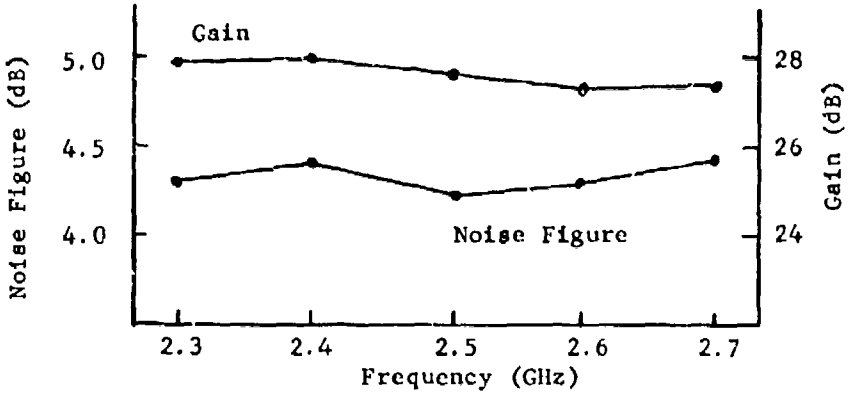


FIGURE 4: RF Amplifier Response

Characteristics	Minimum	Maximum
Gain (dB)	27.0	28.8
Gain Flatness	±0.2	±0.5
Noise Figure (dB)		
2.3 GHz	4.9	5.2
2.5 GHz	5.0	5.4
2.7 GHz	5.1	5.5
Output VSWR	1.7	2.5
Isolation of Switch and Limiter (dB)	61.6	67.0

TABLE 3: Performance of Production Modules

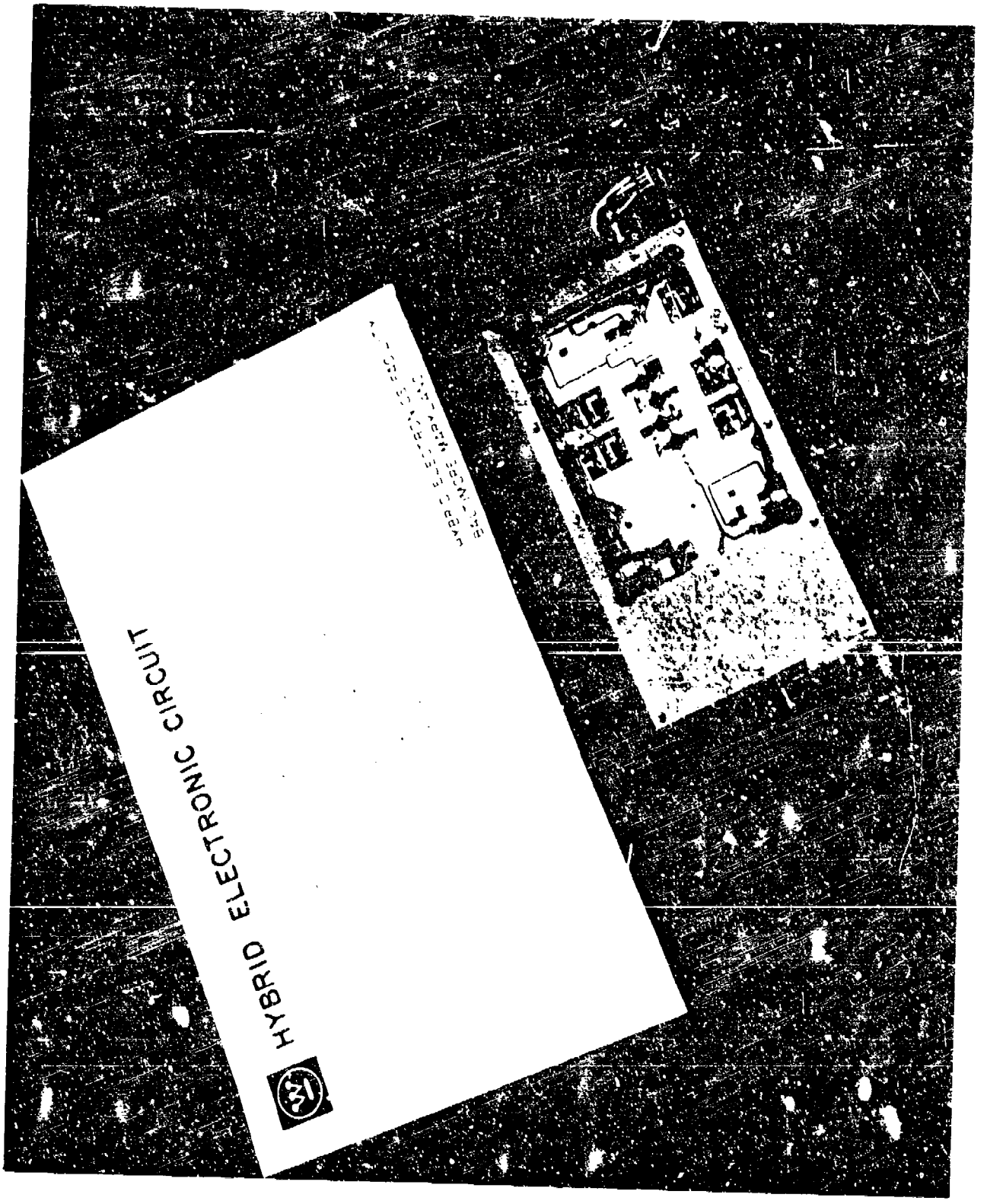


Figure 5. Prototype Integrated Module

APPLICATION OF MIC TECHNOLOGY TO WIDEBAND MICROWAVE RECEIVERS*

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ABSTRACT

A variety of microwave integrated circuit components are described which are suitable for application to wideband, high-performance receiving systems. In particular, a 4 to 12 GHz interferometer receiver consisting entirely of integrated modules is presented as an example of the current technology.

I. INTRODUCTION

This paper describes some recent advances in the application of microwave integrated circuit (MIC) techniques to the realization of complex wideband receiving systems. The current level of technology is best illustrated by describing a recently developed 4 to 12 GHz double-superheterodyne interferometer receiver. A number of new MIC components and modules used in this receiver are described, including:

- S, C, and X-band step-scanned local oscillators
- Half-octave, C- and X-band tunnel-diode amplifiers
- Octave-wide PIN-diode attenuators
- Half-octave mixers with 1 to 2-GHz IF outputs
- Phase-tracked limiters,
- A wide variety of band-pass and low-pass filters in microstrip and alumina sandwich line

II. WIDEBAND RECEIVER

Figure 1 shows the block diagram of a recently developed laboratory interferometer receiver for the 4 to 12 GHz range. This receiver takes equal-amplitude RF inputs and, after double downconversion, compares their phase in a 0.7 to 0.9 GHz (second IF) phase comparator.

The RF input of each of two channels is split into three bands by means of a triplexer which feeds 4 to 6, 6 to 8, and 8 to 12 GHz receiver modules. These modules perform the two frequency converstions. Each of the two sets of three receiver module outputs are recombined in a pre-encoder channel which provides IF gain and serves to hard limit the RF input's 40-dB dynamic range to a level within 1 dB. Each pre-encoder channel provides an output to the phase comparator. Finally, the 0.7 to 0.9 GHz IF is further resolved into 15 frequency slots, each 13.3 MHz wide in the frequency channelizer module.

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* This work was supported in part by the Air Force Avionics Laboratory under Contract F33615-69-C-1859. H.C. Okean was with AIL, a division of Cutler-Hammer. He is now with LNR Communications, Inc., Farmingdale, N.Y. 11735.

Two local oscillator assemblies supply the step-tuned signals which are required for the frequency conversions.

The components contained in each of these modules are now described.

A. Triplexer

The triplexer serves to split the 4 to 12 GHz input into three bands. It consists of three band-pass filters which are sequentially switched as indicated in Figure 2. Two SPDT PIN-diode switch modules mounted in microstrip provide band selection. The filters are constructed in alumina sandwich line of 0.1-inch ground plane spacing and provide greater rejection than could be obtained in microstrip.

B. Receiver Modules

Figure 3 is a block diagram of a typical receiver module. A variety of receiver functions are contained in this module, including:

- Crystal video detector for high level signal reception
- Main channel double-superheterodyne downconversion
- Independently tunable monitor receiver

The components of special note are the circulators, tunnel-diode amplifiers, PIN-diode attenuator, and the balanced mixers. They represent considerably wider band designs than had previously existed in alumina microstrip.

C. Local Oscillator Assemblies

Local oscillator signals from 6 to 13 GHz are supplied by a bank of six Gunn oscillators. Also contained in the first LO assembly are PIN-diode switches and power dividers for signal distribution.

The second LO is supplied by a PIN-diode step-tuned transistor oscillator for 1.9 to 2.7 GHz. This assembly also contains power dividers and switches which direct oscillator power to the proper mixers.

D. Other Modules

All other modules consist of 0.7 to 0.9 GHz IF components. The pre-encoder contains transistor amplifiers and diode limiters. The phase comparator module has low-pass filters, rat-race and quadrature hybrids, and detector-video amplifiers. The frequency channelizer consists of a bank of 15 single-pole band-pass filters each coupled to a detector-video amplifier.

III. CONCLUSIONS

A number of recently developed receiver components have been briefly described. By using them as building blocks, a fairly complex receiving system has been configured. Undoubtedly other receiving systems using the components described herein will suggest themselves to the reader.

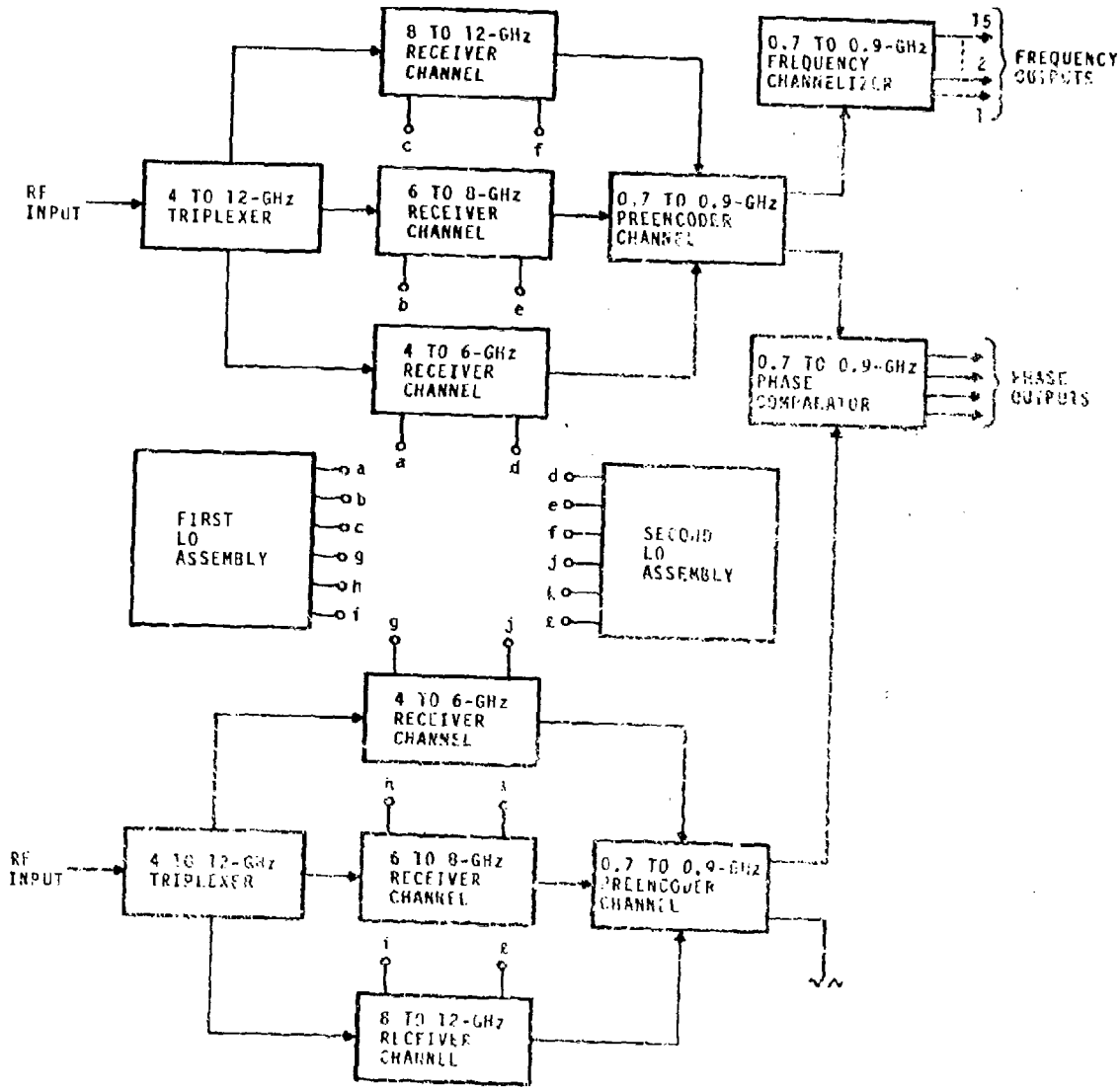

FIGURE 1. BLOCK DIAGRAM OF WIDEBAND MIC INTERFEROMETER RECEIVER

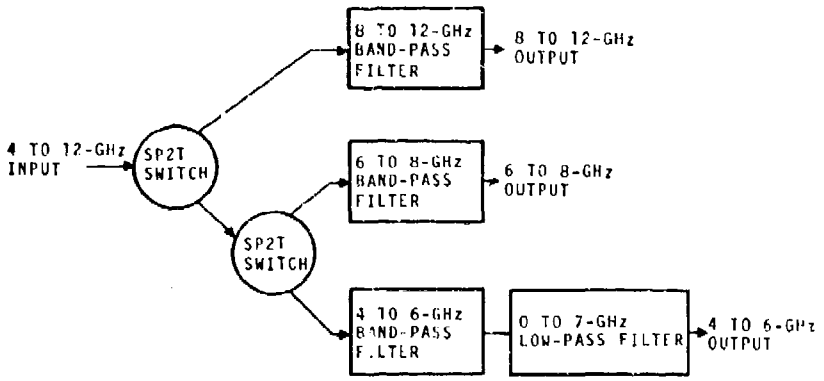

FIGURE 2. SWITCHED TRIFLEXER

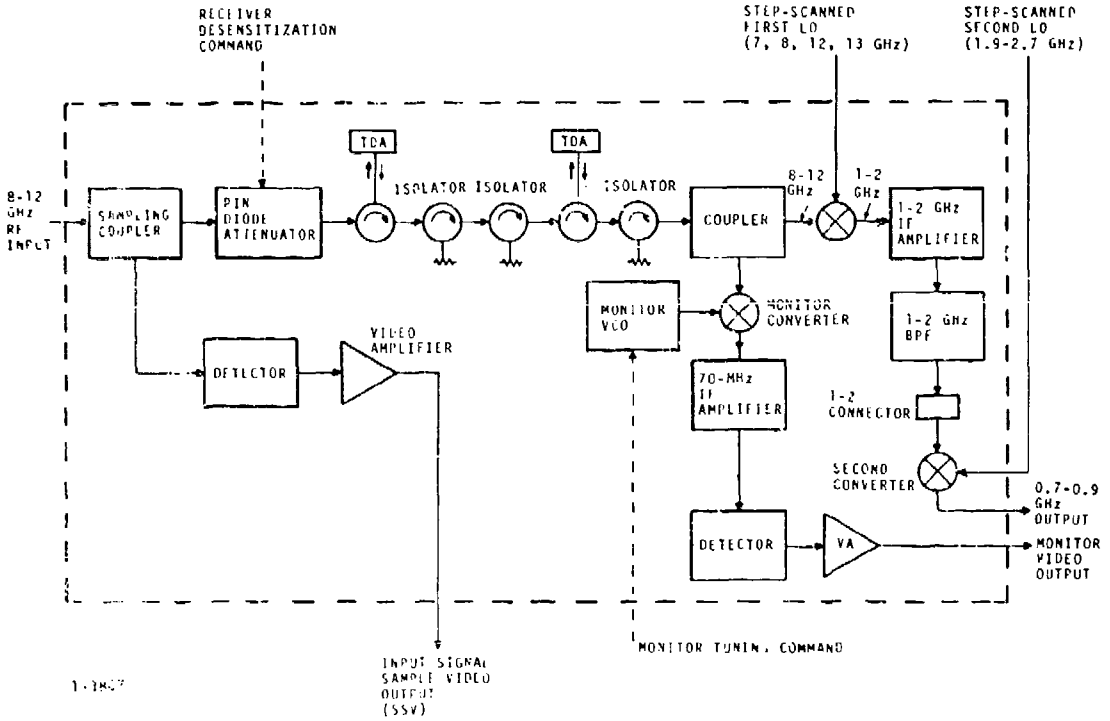

FIGURE 3. BLOCK DIAGRAM OF 8 TO 12 GHz RECEIVER CHANNEL

UHF HYBRID INTEGRATED 45-WATT TWO-STAGE AMPLIFIER WITH OCTAVE BANDWIDTH

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Semiconductor Products Division
Motorola Inc.
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ABSTRACT

Design and realization of a hybrid integrated 45-watt two-stage UHF amplifier with 12-16 dB gain over an octave bandwidth are described. Emphasis is on computer-aided design and on layout and assembly contributing to low-cost production.

INTRODUCTION

Requirements of the emerging generation of communications equipment in the 225-400 MHz band impose need for an efficient solid state high-power CW amplifier at ever-increasing output levels in a design which is adapted to low-cost quantity production. To meet the present need, a 45-watt amplifier with 12 dB minimum gain, ± 2 dB gain variation, 1.4:1 maximum VSWR, and 30% minimum efficiency across the band was developed. Operating temperature range is -55°C to +72°C, and the amplifier remains stable at all output levels and when driving a load having 3:1 VSWR at any angle. Hybrid integrated circuitry is utilized throughout, and the amplifier is constructed in a dual-channel balanced amplifier configuration as block diagrammed in Figure 1. Each channel consists of two stages, and the channels are combined using overlay quadrature hybrid couplers at input and output. The amplifier housing is hermetically sealed, and its dimensions are 2.8 x 1.8 x 0.75 inches exclusive of connectors. The design procedure and amplifier realization are described.

DESIGN

It was determined at the outset that design requirements would best be met using a balanced amplifier configuration. This permits a low VSWR across the band at the amplifier input (into the hybrid coupler) while the exped-

ient of mis-matching each amplifier channel at low frequencies is used for gain leveling. It also provides a reliability bonus in that open-circuit failure of one channel results in reduction in output rather than catastrophic failure. The quadrature hybrid couplers used are of conventional $\frac{\lambda}{4}$ stripline construction having less than .25 dB insertion loss.

Each of the two identical amplifier channels uses two common emitter stages both operating class C. The transistors selected are the Motorola RF164 and RF416 for the driver and power stages, respectively. Both are 28V silicon npn devices which are rated at 20W output for the RF164 and 30W for the RF416 at 400 MHz. A newly-designed microstrip-compatible carrier for high-power UHF transistors, which is sketched in Figure 2, was used for both transistors. It consists of a metallized beryllia substrate with a symmetrical grounded bridge to which the emitter is wire bonded. It provides good thermal conduction to a heat sink and minimum series inductance in the grounded emitter.

It has been observed that gain characteristics of a UHF common emitter large signal transistor can be optimized by augmenting the base-to-emitter capacitance with a selected external capacitor located closely as possible to the chip. The effects of various capacitance values on the RF164 at 8.5W output across the band are shown in Figure 3 for matched operation. A 6 dB per octave roll-off with no capacitance is reduced to 1.5 dB gain spread, gain at 400 MHz is increased 2 dB, and efficiency is improved using a 71 pF augmenting capacitor.

Gain and efficiency of the RF416 transistor, which was operated without an augmenting capacitor, are plotted in Figure 4.

To simplify the input and output matching networks, the 50-ohm source and load impedances were reduced by a factor of 4 using transmission-line transformers. However, it was found that transformers constructed of a bifilar winding on a toroidal core as discussed by Ruthroff[1] had non-uniform transfer functions resulting from varying parasitic inductances caused by slight variations in windings. This problem was eliminated by design of an equivalent transmission-line transformer using parallel-strip transmission lines[2] formed by etching both sides of a chrome-gold metallized 10-mil thick alumina wafer. Transformer construction is sketched in Figure 5. The wrap-around metallization on one edge constitutes the ground terminal as well as the surface which is soldered to the circuit ground plane for vertical mounting of the transformer as shown in Figure 6. Figure 7 shows impedance measured at the low-impedance terminal with a flat 50-ohm load on the high-impedance terminal for three

transformers having different developed lengths of transmission line. Line length of 1.1 inch was used for this amplifier. Measured insertion loss is less than .25 dB, and the temperature coefficient is 1°C/W at 400 MHz.

Two computer programs were used in designing the coupling networks. One incorporates an optimization subroutine and is used in the selection and optimization of a simple broadband network configuration and constants. Using the second program, circuit parasitics are introduced, and the selection of constants is refined.

Objectives of the coupling circuit design are to develop an amplifier having constant transducer gain across the 225-400 MHz band in a 50-ohm system and to provide good impedance match at outputs of both stages for maximized efficiency. This was accomplished using the following procedure. The drive levels into the power (output) stage to compensate for the composite gain roll-offs indicated by Figures 3 and 4 were determined. Input impedances of the driver stage then were measured under matched conditions at these output levels, and an input network for the driver stage was designed which provided good impedance match at the upper end of the band with progressively greater mismatch at lower frequencies as calculated to compensate for gain roll-off. Output impedance was measured across the band for an RF164 equipped with the designed input network. A broadband interstage network then was designed for optimal match between this impedance and measured input impedance of the RF416 under matched conditions at rated output power (30W) across the band. This network and an RF416 then were added to the driver stage, and output impedance was measured. The output network then was designed to match this impedance across the band to the transformed 50-ohm load.

Lumped constants were used for convenience in initial design and breadboarding. Where feasible, these constants later were converted to equivalent microstrip transmission line segments.

AMPLIFIER REALIZATION

Primary objectives in design of the amplifier structure and housing are to achieve maximum producibility and to develop the required manufacturing technology while maintaining design performance and reliability.

Each channel assembly of the amplifier consists of seven small microstrip circuit boards, two transistor carriers, and two ceramic transformers. All inductances and RF chokes are realized as equivalent transmission line sections, capacitors are discrete ceramic chips, and resistors are evaporated thin film on SiO_2. Figure 8 shows

the circuit layout used in production units.

Before assembly of the amplifier, each circuit board is prepared as a sub-assembly on which are mounted discrete components and coupling ribbons using high-temperature (300°C) solder. After test and inspection of transistors and sub-assemblies, they are fitted into the housing with lower temperature solder preforms and furnace soldered at a temperature of 200°C. This process of assembling pre-tested sub-assemblies is capable of producing high yields of acceptable amplifiers in production. In addition to this advantage, metallized small ceramic boards can be soldered successfully directly to a plated aluminum housing whereas a larger ceramic board may crack due to thermal stresses during the cooling cycle.

All circuit boards are 50-mil thick 99.5% alumina with chrome-gold metallization. This board thickness is used because it provides reasonably high impedance lines (72Ω) with sufficient width (20 mils) to keep I^2R losses within acceptable limits. Uniform board thickness contributes to ease of attaching interconnecting ribbons.

The amplifier package permits assembly of each channel into a separate housing such that only pre-tested channels are assembled into a dual-channel amplifier; again, a yield-improving expedient relative to use of a single dual-channel housing. Figure 9 is an exploded view of the amplifier package showing the method of installing the quadrature hybrid couplers and the hermetic feed-throughs to the couplers and the external bias supply. The two channel housings are soldered together and to the base plate. After final test the hermetic seal is completed by soldering the cover plate in place with a lower-temperature solder. Figure 10 is a photograph of a prototype amplifier without cover plate.

TEST RESULTS

Test data measured on one typical production prototype amplifier and summarized here indicate that performance objectives stated at the outset have been met.

Transducer gain, collector efficiency, and VSWR at 45W constant output across the 225-400 MHz band at room temperature are plotted in Figure 11. Minimum gain is 12.5W with total gain spread of 2.3 dB. Minimum efficiency is 30%, and maximum VSWR is 1.45:1.

Transducer gain and efficiency measured at 45W constant output are plotted against frequency in Figure 12 for the two temperature extremes of -55°C and +72°C. Performance data for intermediate temperatures are encompassed by these curves. Rated 45W output power capability with minor variations in gain and efficiency are shown at all temperatures

within this range.

Power delivered to the load and efficiency of the amplifier operating into a 3:1 VSWR load are summarized in Table I for band-end frequencies of 225 and 400 MHz. At each frequency and load angle the amplifier was operated either at 45W output or at an output obtained with a supply current not to exceed 3.0 amp in either single channel. Minimum output power was 33.1W, and minimum gain was 11.89 dB.

The amplifier output was monitored with a spectrum analyzer in all tests. In no case, including operation into 3:1 VSWR load, was there instability or generation of spurious frequencies at any combination of frequency, temperature, or signal level, nor was there device damage. The second harmonic remained more than 15 dB below the fundamental.

Capability of operating continuously and stably at output levels down to 0.5W at all frequencies and temperatures was verified.

The work reported in this paper was supported in part by the Manufacturing Technology Division, Air Force Materials Lab, WPAFB, Contract F33615-70-C-1828.

Freq. MHz	P_o W	G dB	Eff. %	ρ_v Angle deg
225	45.0	12.20	31.2	0°
225	45.0	12.25	30.7	90°
225	37.2	11.89	31.3	180°
225	45.0	12.38	31.3	270°
400	40.7	13.57	26.4	0°
400	42.2	14.16	26.3	90°
400	33.6	14.89	25.9	180°
400	33.1	14.67	21.6	270°

Table I

Operation into 3:1 VSWR Load at all Angles at Band-End Frequencies

REFERENCES

(1) C. L. Ruthroff, "Some Broad-Band Transformers", Proc. IRE, August 1959, p. 1337-1342.

(2) H. A. Wheeler, "Transmission-Line Properties of Parallel Strips Separated by a Dielectric Sheet", IEEE Trans. on Microwave Theory and Techniques, March 1965, p. 172-185.

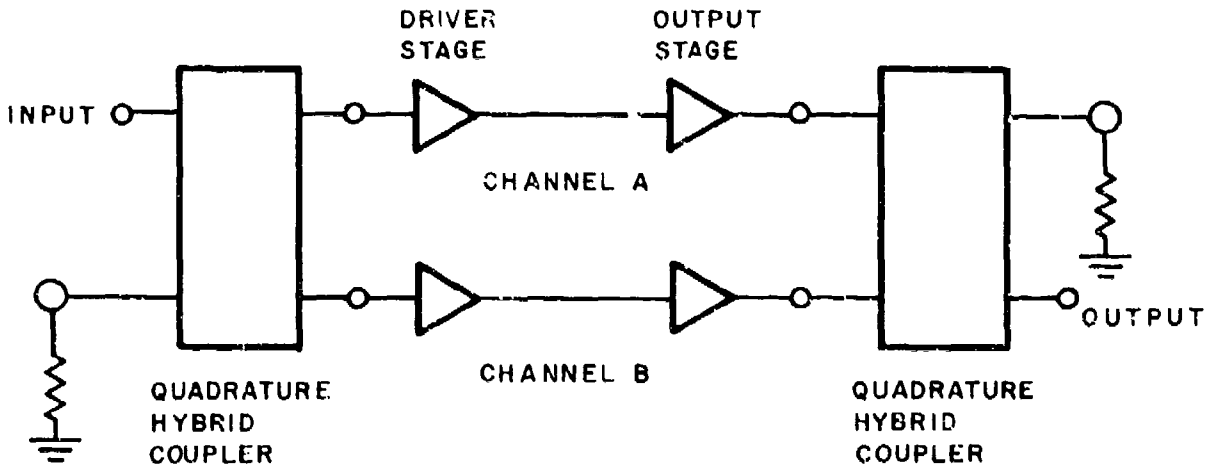

Figure 1. Balanced Amplifier Configuration

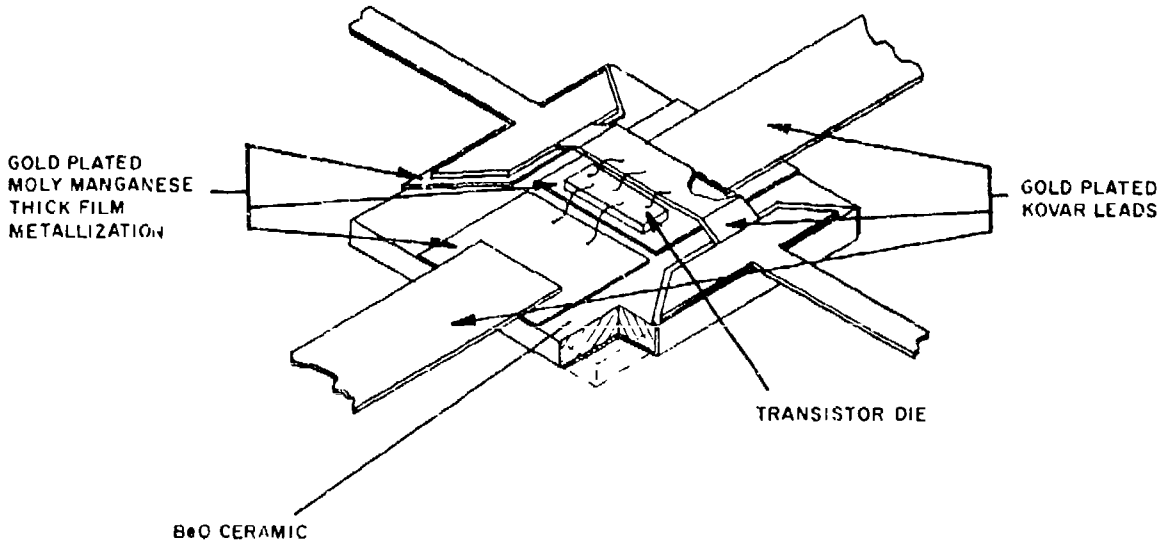

Figure 2. Microstrip-Compatible Carrier for UHF Power Transistor

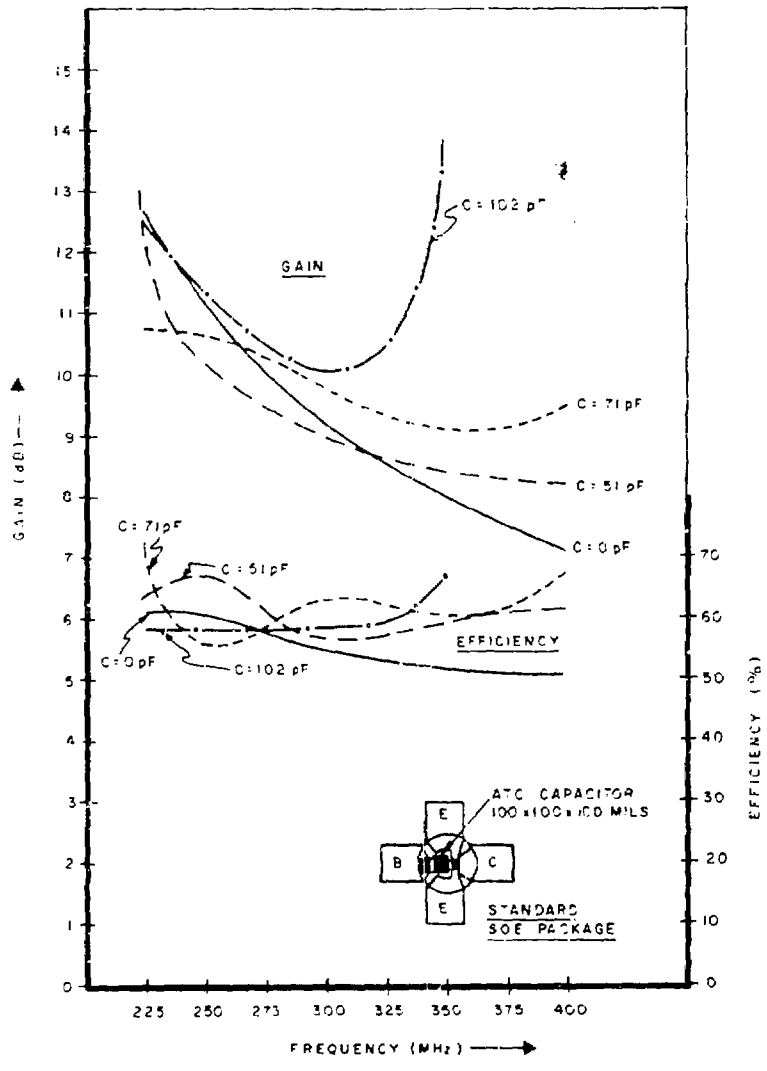

Figure 3. Gain and Efficiency of RF164 With Various Augmenting Base-to-Emitter Capacitors at 8.5W Output

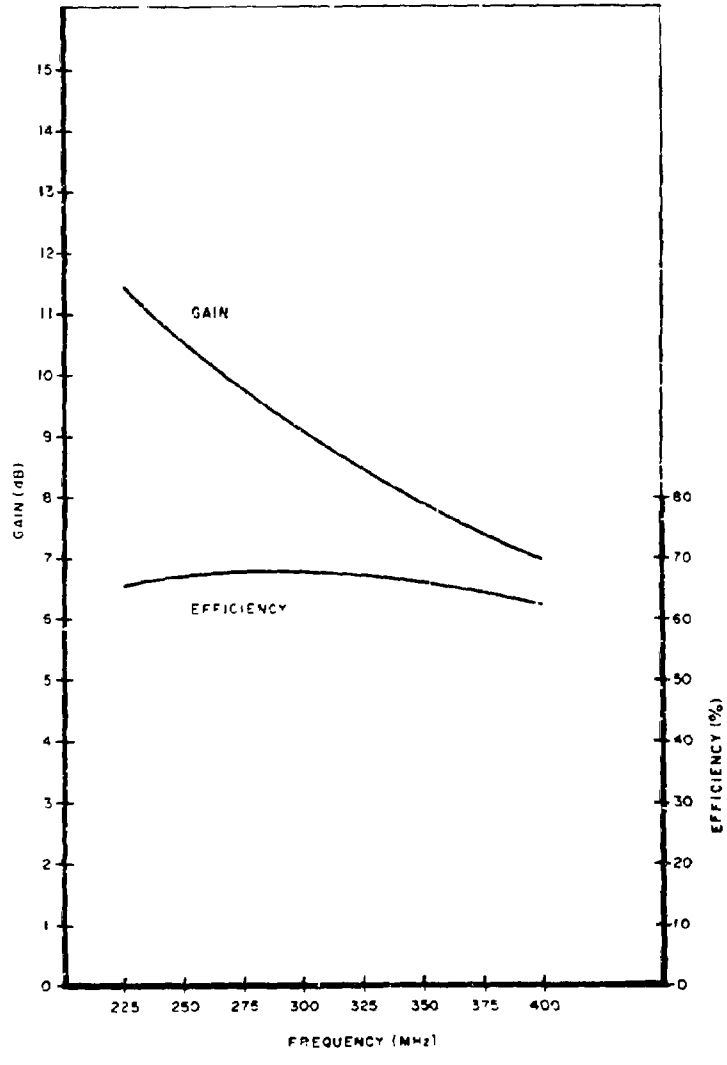

Figure 4. Gain and Efficiency for Typical RF416 at 30W Output

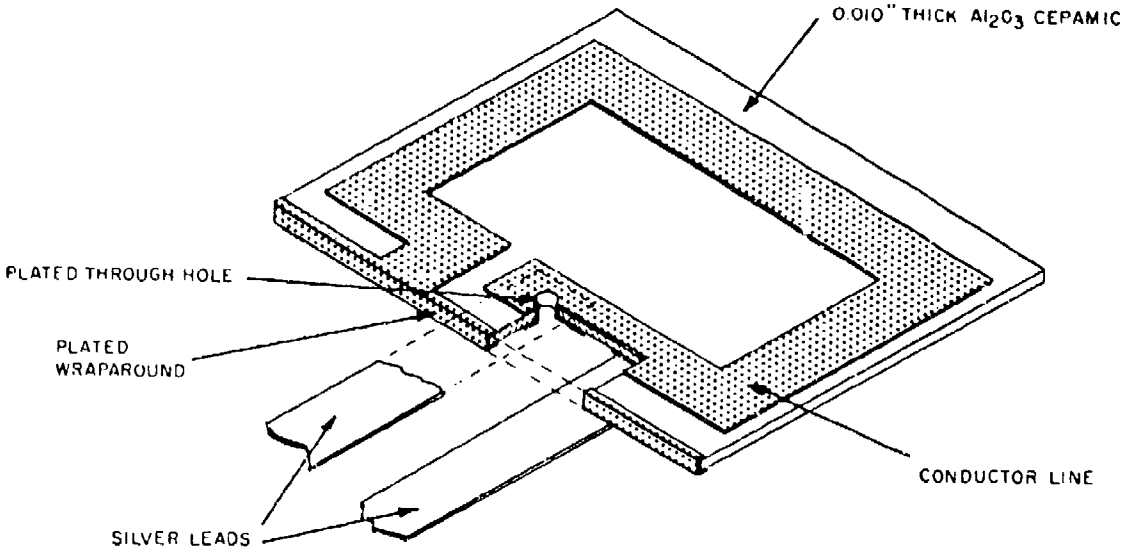

Figure 5. Ceramic Transmission Line 4 : 1 Impedance Transformer

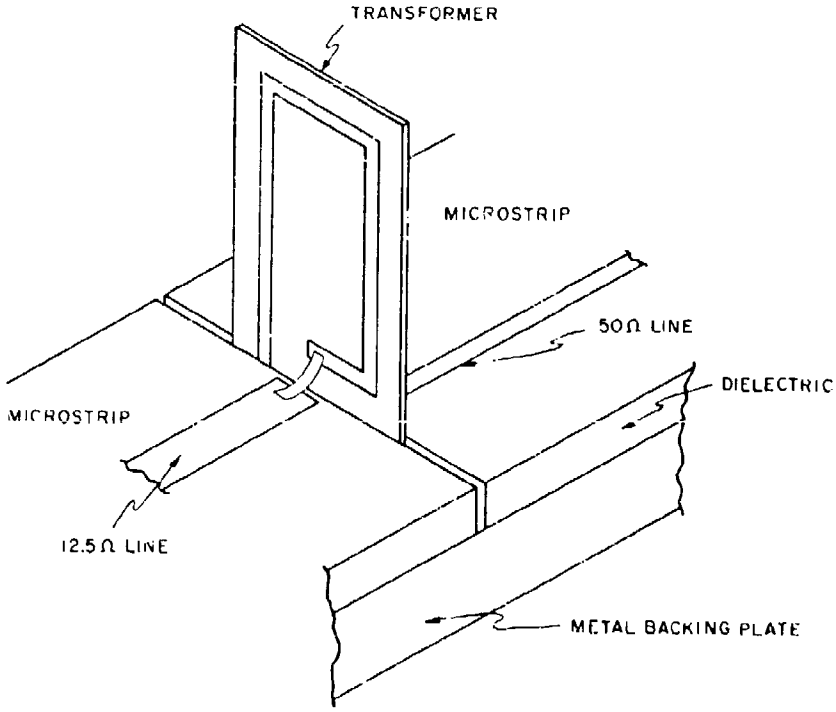

Figure 6. Installation of Ceramic Transformer

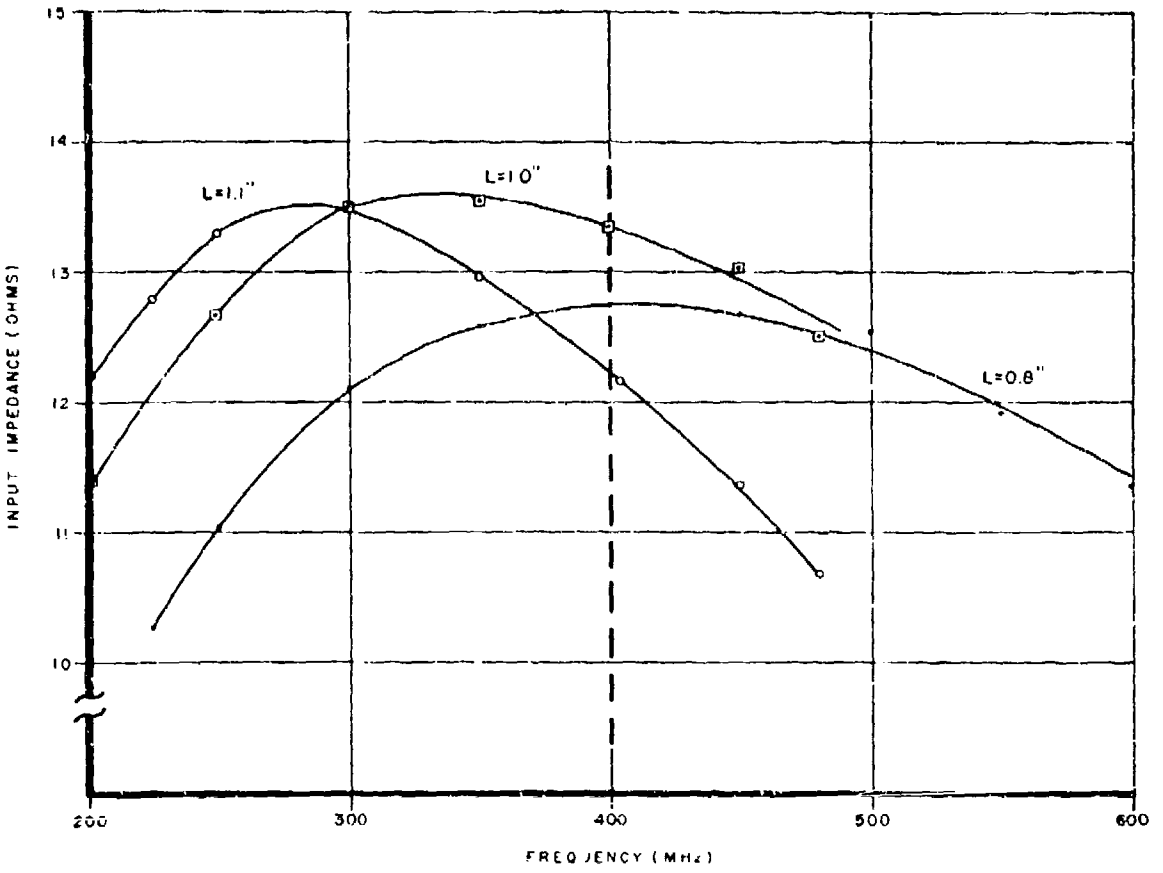

Figure 7. Amplitude of Input Impedance for Three 50 - 12.5-Ohm Ceramic Transmission Line 4 - 1 Impedance Transformers Terminated in 50 Ohms and Having Line Lengths of 0.8", 1.0", and 1.1"

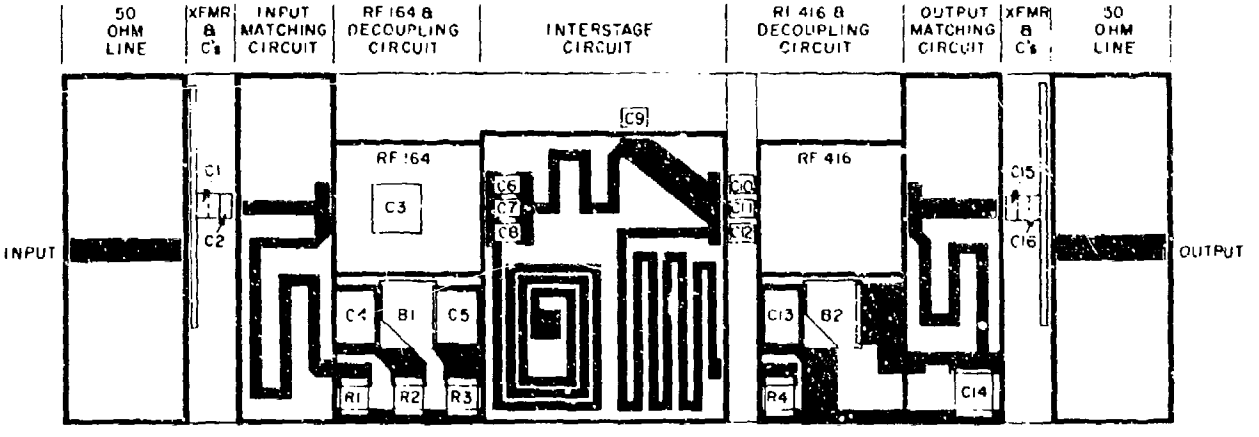

Figure 8. Hybrid I.C. Layout for One Amplifier Channel

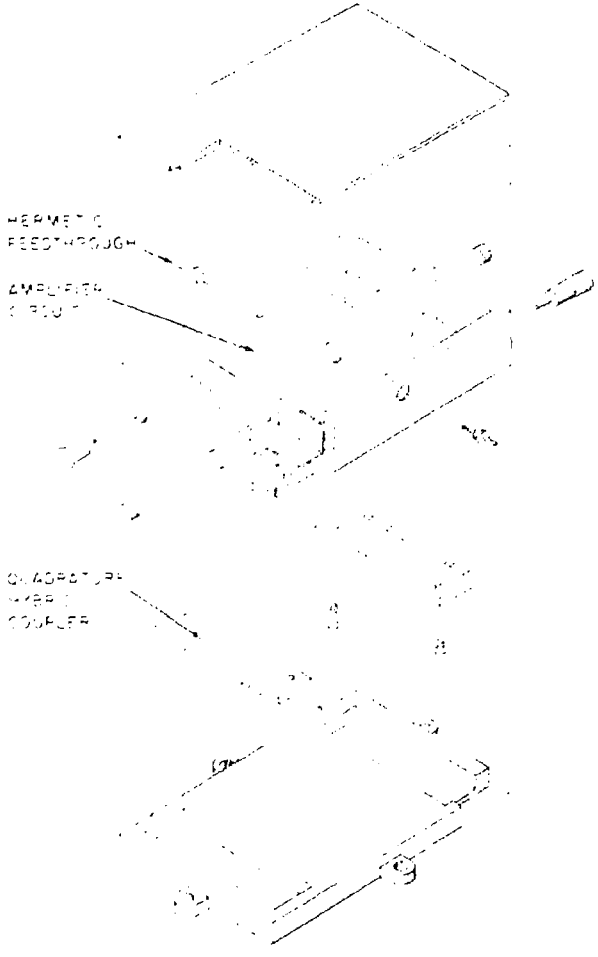

Figure [illegible] Amplifier Hermetic Assembly Drawing

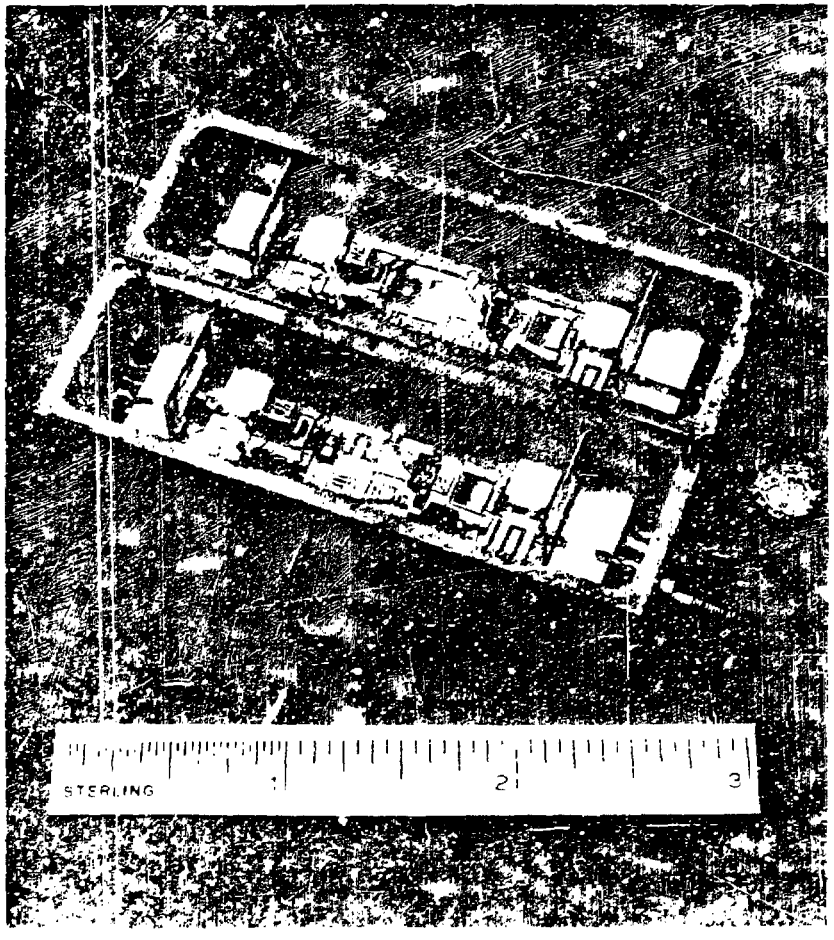

Figure 30. Prototype Amplifier with Cover Removed

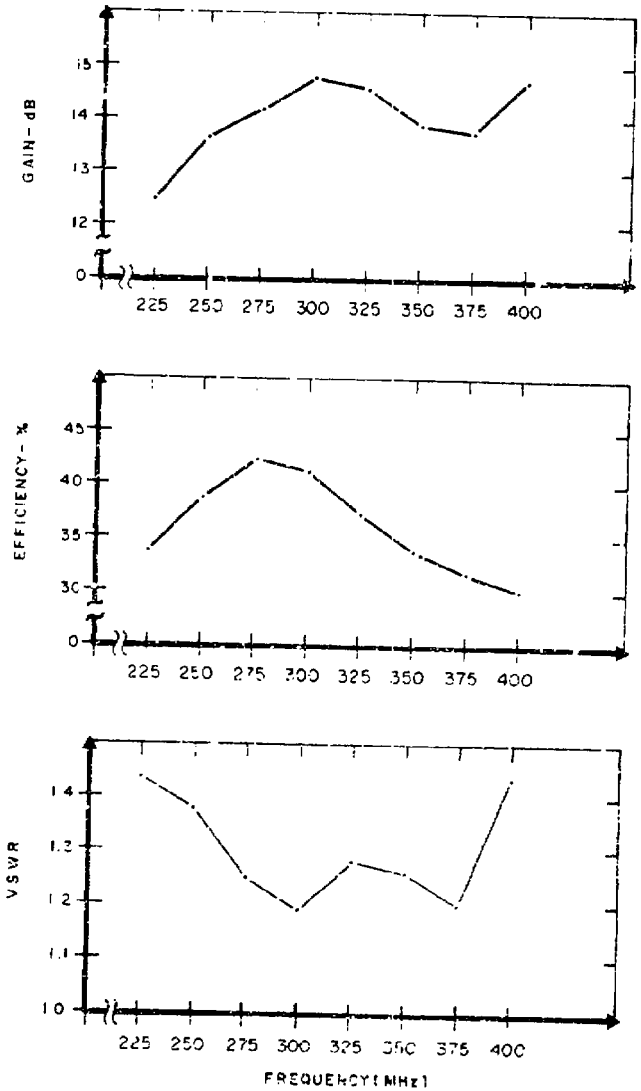

Figure 11. Transducer Gain, Efficiency and VSWR at 45W Output

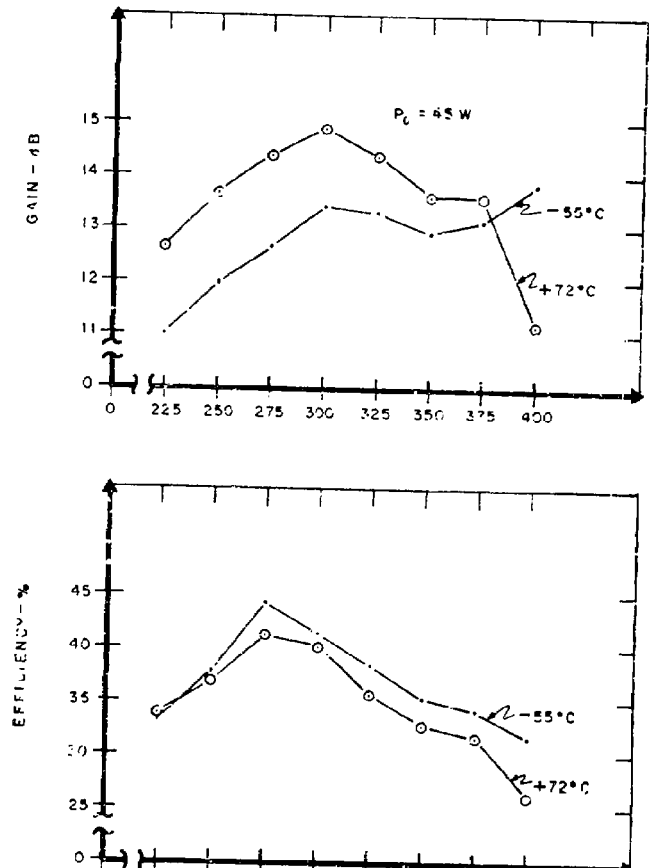

Figure 12. Transducer Gain and Efficiency at 45W Output for -55°C and +72°C

AN INTEGRATED INTERMEDIATE-FREQUENCY AMPLIFIER-LIMITER*

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ABSTRACT

The design and fabrication of an integrated intermediate-frequency amplifier-limiter is described. The low power consumption and amplitude-to-phase conversion characteristics make the circuit ideally suited for use as part of a communications satellite F-M repeater. Experimental results are presented.

*This work was sponsored by the Department of the Air Force.

BACKGROUND

This paper describes an intermediate-frequency amplifier-limiter designed for use in the Lincoln Experimental Satellite series of communications satellites. This circuit is used to amplify received frequency-modulated signals (converted to a 3 MHz center frequency) to a standard amplitude prior to retransmission by the satellite. Primary design objectives include low-power operation, low amplitude-to-phase shift conversion to minimize distortion of the F-M signals, and fabrication in a small, reliable form. It was also necessary to convert the initial breadboard circuit to final form quickly in order to meet satellite assembly schedules.

CIRCUIT DESIGN

The configuration chosen for the amplifier-limiter consists of an emitter-coupled amplifier driving an emitter follower included to provide low output impedance. The emitter-coupled pair provides wideband small-signal response and limits the output at a predictable level determined by the magnitudes of the operating current and the load resistor of the amplifier. Preliminary analytic and experimental investigations indicated that the only effective way to reduce amplitude-to-phase conversion for this circuit was to increase its small-signal bandwidth well above 3 MHz. Furthermore, it was necessary to increase the bandwidth by reducing the r-c time constant at the output node of the emitter-coupled amplifier (the dominant time constant for this configuration), since attempts at inductively peaking the amplifier response resulted in disastrous amplitude-to-phase characteristics. The low-capacitance requirement dictated that the final circuit be fabricated in hybrid rather than monolithic integrated circuit form since the collector-to-substrate capacitance associated with monolithic designs would deteriorate performance.

The circuit schematic is shown in Fig. 1. The quiescent bias current of the emitter follower is repeated by the Q_4-Q_5 pair to set the bias level of the emitter-coupled pair. This technique permits low voltage operation of the current source so that a 5-volt supply is sufficient. Since the bias current of the output transistor is repeated, no additional supply current is necessary to bias the current source.

Some operating point stability is obtained because of negative feedback, although the gain around this loop is quite low. A more important source of small-signal gain stability arises because of the temperature characteristics of the diode and the base-to-emitter junctions of Q_1 and Q_5. As temperature increases, the forward voltages of these three junctions decrease, and thus I_1 increases. The voltage gain of the emitter-coupled pair is approximately

$$\frac{g_m}{2} \times 1.5\ K = \frac{q}{2kT} \times \frac{I_2}{2} \times 1.5\ K \qquad (1)$$

where g_m is the transconductance of either Q_2 or Q_3. The increase in I_2 with temperature (since this current is equal to I_1) offsets the

decrease in transconductance with temperature which results if a bipolar transistor is operated at constant current.

Since transistors Q_2 and Q_3 are biased at approximately 0.25 mA each, their transconductances are 10 m mho, and the small-signal voltage gain of the circuit is approximately 7.5. The maximum peak-to-peak output signal swing is 0.5 mA x 1.5 K = 0.75 volt, and the power consumption of the circuit is 5 mW.

CIRCUIT FABRICATION

The layout of the 3 MHz amplifier-limiter circuit was initiated by applying an equation that we have found useful in predicting the substrate area required for components and interconnection metalization. The parameters required for the equation are: the number of internal substrate and input-output connections, total substrate area required for active devices, resistors, capacitors and other component pads, number of resistors whose areas are determined by power considerations rather than sheet resistivity, and number of total components. Experience has indicated that the equation predicts a substrate area within 5-10 percent of the area actually required for the layout.

After the package and related substrate size were chosen based on the area predicted, the circuit layout was drawn to scale. This drawing was then digitized using a Calma machine where sets of coordinate numbers for each component bonding pad and conductor lines were recorded on magnetic tape.

After digitizing, the magnetic tape was placed on an IBM 360 computer where programs called "DIGITIZE" and "MANNPLOT" were used to scale, edit, and provide a visual display of the layout. At this time any corrections in component placement or line routing may be made. When the layout was accepted as correct, a paper tape was punched with the edited data. This tape was then used to make the masks for the substrates.

The masks were made on a David Mann computer-controlled pattern generator. The pattern generator exposed a glass plate in such a manner that a mask of the circuit was produced. After chemical developing of the plate, the finished mask was ready for final processing of the substrate.

The amount of time from layout to final glass masks was 2-1/2 days. This was followed by a day for substrate metalization and etching resulting in a total time of 3-1/2 days from layout to availability of a prototype substrate.

Fabrication of the circuit was completed using chip resistors, capacitors and transistors. The passive elements were attached to the substrate with a conductive adhesive, while semiconductor devices were eutectically mounted. Conventional ultrasonic wire bonding was employed for the pin-to-substrate connections.

In-process testing was performed on the circuit during

fabrication. The testing consisted of matching critical transistor pairs for current gain and base-to-emitter voltage before bonding and a functional test of the circuit after bonding, but before sealing of the package. This testing provided an opportunity of repairing any defective component and resulted in a high yield after sealing.

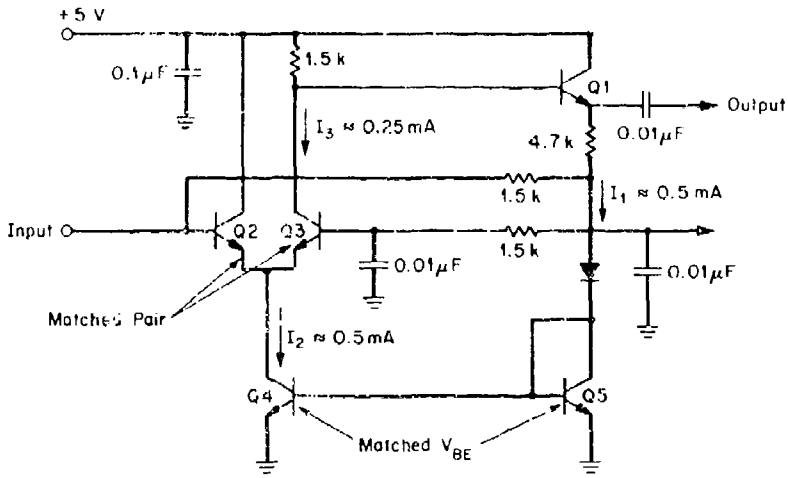
Since the circuit was for a space flight application, rigorous environmental testing was performed. This included mechanical shock and vibration, centrifuging, thermal shock and a burn in. The prototype circuit has met or exceeded all the original specifications and bids are now out for production units.

The layout used for this circuit is shown in Fig. 2, while Fig. 3 illustrates the complete circuit.

PERFORMANCE

Figure 4 shows the output and relative phase change of three cascaded amplifier-limiter stages as a function of input-signal level. For small input signals the voltage gain per stage is 18 dB, consistant with the predicted value. The amplitude-to-phase conversion characteristics indicate a peak-to-peak phase change of less than 25° for a 120 dB change in input-signal level. This value insures that the distortion of the frequency-modulated signals will be negligible for anticipated amplitude-change rates.

The frequency response of each individual stage is flat within +0, -3 dB over the 20 kHz to 10 MHz range, and this wide bandwidth is responsible for the excellent amplitude-to-phase shift conversion characteristics. The change in linear-region gain with temperature is less than 0.1 percent per degree centigrade.



Note: Transistors are 2 N2484 type

AMPLIFIER - LIMITER SCHEMATIC

Figure 1 3 MHz Limiter

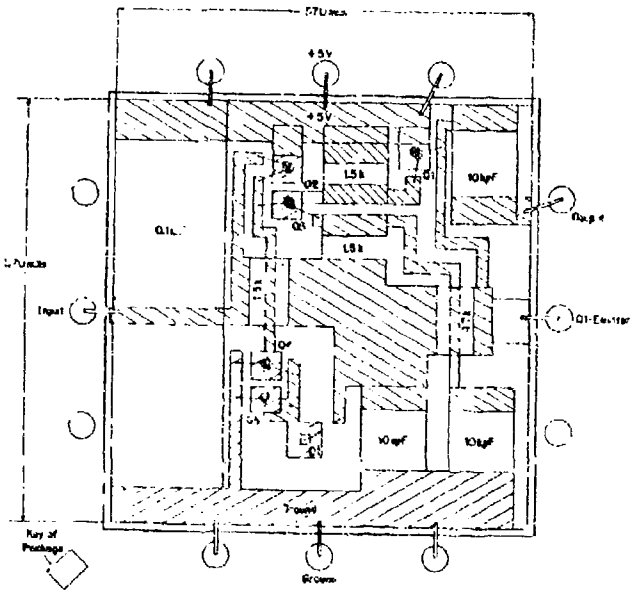


Figure 2 Substrate Layout

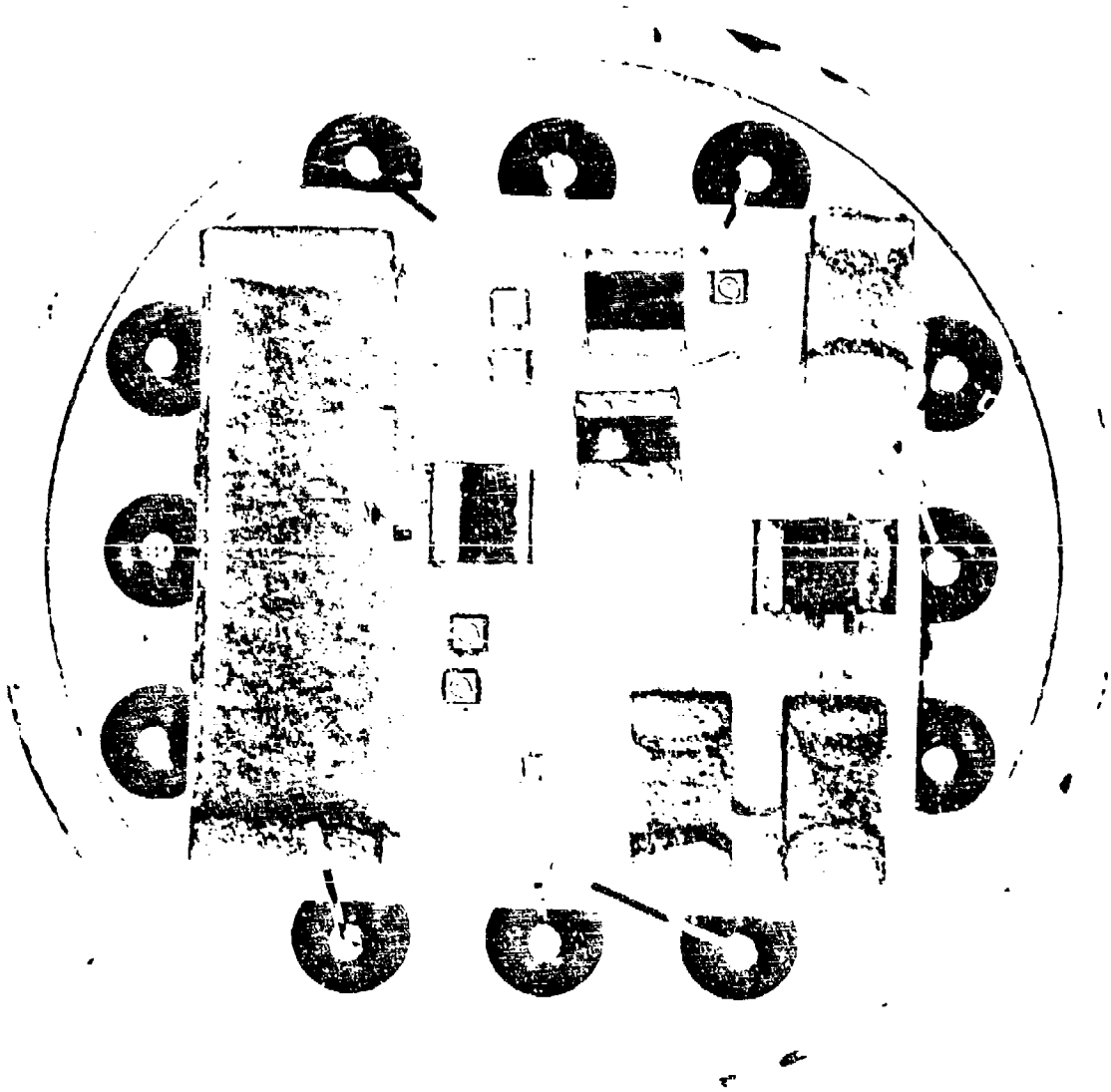
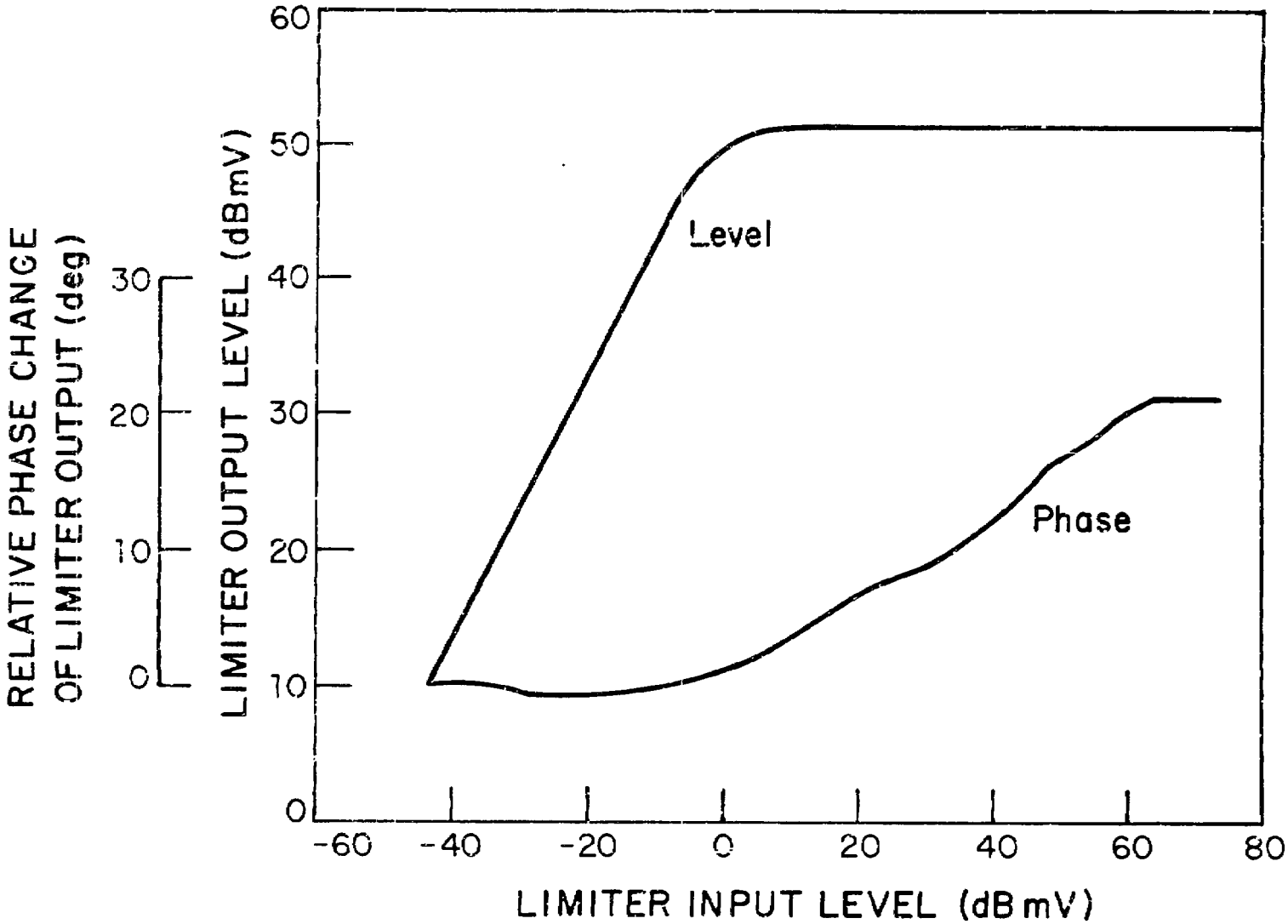


Figure 3 Final Assembly



OUTPUT-SIGNAL LEVEL AND RELATIVE PHASE SHIFT vs INPUT-SIGNAL LEVEL FOR THREE CASCADED STAGES

Figure 4 Output and Relative Phase Change vs. Input Signal

A HYBRID INTEGRATED FERRITE PHASE SHIFTER DRIVER FOR PHASED ARRAY RADAR APPLICATIONS*

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Abstract

A hybrid integrated driver circuit for latching ferrite phasers is described. Test data on prototype drivers demonstrates ability to control phase accurately over a wide temperature range, interchangeability, and small sensitivity to phaser parameter variations.

Introduction

A hybrid integrated version of a flux drive control circuit[1] for nonreciprocal toroidal latching waveguide ferrite phasers[2] is described. Test data on prototype drivers demonstrates ability to control phase accurately over a wide temperature range, interchangeability, and small sensitivity to phaser parameter variations.

The principle of the flux drive circuit is demonstrated in Fig. 1. Phase is changed by incrementing the phaser toroid flux from a reference remanence state on the major hysteresis loop. This is accomplished by applying a voltage step, v(t), to the control winding which threads the toroid. If the driver output impedance, leakage inductance and circuit losses are negligible, the incremented flux $\Delta\psi$ is proportional to a volt-time integral, i.e., $\Delta\psi = \int_0^t v(t)\,dt$. Ideally, if the applied voltage is a step function of amplitude V, the flux increment is simply proportional to time.

The driver delivers an initial RESET command to establish the reference state followed by a SET pulse to achieve the desired phase state. The reference point is taken to correspond to the long (μ^-) state, since the insertion phase of the long state is less temperature-sensitive than that of the short (μ^+) state. Assume that in the TRANSMIT mode of operation the reference is represented by state A of Fig. 1a. During the pulse the flux is incremented along path AB. When the driver is turned off the flux relaxes to the remanent point C. If C is on a minor loop for all phase settings, any shrinkage of the

*This work was sponsored by the Department of the Army.

hysteresis loop due to average power heating or ambient temperature fluctuations can be accommodated. In addition, phaser mechanical tolerances and toroid material tolerances become less critical.

The flux differential $\psi_B - \psi_C$ corresponds mainly to reversible domain wall motion. Energy must be supplied by the driver to sustain the reversible flux. This energy is not recovered, but is dissipated in the driver circuitry.

Due to the nonreciprocal nature of the phase shifter, the remanent induction must be inverted when changing between the TRANSMIT and RECEIVE modes of operation. Point D in Fig. 1a represents the new reference state for RECEIVE.

The differential phase-versus-time relationship is usually nonlinear. Linearization is accomplished within this particular driver by shaping the driver waveform (Fig. 1c). In addition, for operation with a digital steering control scheme, an auxiliary digital-to-analog converter is required.

Circuit Description

The phaser configuration utilized in this work is operated with single wire control. Hence, the driver must be capable of providing output waveforms of both positive and negative polarity. For the SET function a peak current of 3A is required. During the RESET operation, which is performed in about half the time taken for the SET function, the peak current is permitted to rise to a maximum value of 10A.

The driver block diagram is shown in Fig. 2. The driver comprises dual channel complementary amplifiers with low output impedance ($\approx$0.3 ohm) direct-coupled emitter-follower final stages. One channel processes the SET and RESET commands for the TRANSMIT mode. The other channel is active in the RECEIVE mode.

The waveform shaping required to linearize the phase-time relationship is performed in the small-signal amplifying stages. The rectangular input pulse from the control logic circuitry is amplified and is then accurately defined in amplitude by a temperature-stable reference voltage. In parallel the input pulse is also differentiated, amplified and then added to the accurately defined waveform. The shaped waveform then drives the class B push-pull output stage. The RESET command signal bypasses the waveform-shaping stages via a separate input, since linearity is not required for the RESET. Thus, additional gain can be provided to speed up the RESET operation.

The special ferrite phase shifter driver components were fabricated utilizing thick film hybrid microcircuit techniques. Screen printing techniques were used to form both the thick film conductor and resistor pattern on the alumina substrate, and the patterns were fired at elevated temperatures. The active devices and capacitors were attached to the substrate to form the hybrid circuit. The transistors were mounted using a gold silicon eutectic bond, and the capacitors

were mounted with a gold-tin solder. Gold wire was used for the interconnections.

The complete low level circuitry is contained within two 5/8" hermetically sealed flat packs. A modified TO-3 package is used for the emitter follower stages, which are separated from the small signal circuitry for thermal considerations. These microcircuit components are mounted with larger discrete components on a printed circuit board as illustrated in Fig. 3.

Each flat pack contains the components which comprise the low power section of one individual channel, including the components which define the reference voltage. The component layout is shown in Fig. 4. The flat packs are identical, with the exception of the transistor chips. The output stages of both channels and four other junctions to provide temperature compensation for base-emitter voltage variations in the output transistors are contained in the single TO-3 package, which is mounted on the heat sink. The component layout within the TO-3 package is shown in Fig. 5.

Large components, such as the necessary energy storage capacitors and potentiomenters, have been mounted directly onto the printed circuit board. In addition, to inhibit the output transistors from delivering excessive current when the phaser toroid saturates, a sensing resistor consisting of a small length of nichrome wire, having a resistance of less than 0.1 ohm, is externally connected in series with the output lead. The voltage developed across this resistor can operate control circuitry to limit the driver current at some predetermined maximum value, e.g., 10A.

Fifty integrated circuit drivers have been fabricated and tested. The objectives of making a small-quantity production run were to verify that the circuit is reproducible and to determine a large quantity (e.g., $\geq$ 10,000) production cost. These objectives have been met. The large quantity price is expected to be less than $50, for production lots of 50,000 or more.

Experimental Results

Experiments were performed with ten S-band latching waveguide phasers having the cross-section indicated in Table I, which also summarizes the performance of the driver-phaser assembly. The driver input pulse width was quantized to four bits (maximum phase increment = 337.5°). The phaser configuration utilizes a single garnet toroid ($4\pi M_S$= 550G) containing a high dielectric constant ceramic ($\epsilon' \approx 38$) insert.[3]

Important criteria for evaluating driver performance are (i) accuracy in setting differential phase shift (ii) effect of parameter tolerances and temperature variations on differential phase shift (iii) switching speed and switching energy. One driver connected in turn to each of the ten phasers exhibited no more than a 3° rms deviation in phase from the nominal setting, for any of the fifteen phase states. The range of the differential phase shift error for all sixteen phase

states for a single driver-phase shifter assembly was measured as a function of incident average power. The total error spread at low power was only 3°, and increased to 11° at 350W. An incident level of 350W corresponded to a phaser temperature rise of about 40°C above ambient. At this power level, the change in the reference insertion phase state was 20° from its value at low power.

The driver circuit itself is very temperature stable, by virtue of the temperature-compensating components. With the phaser operating at low power and maintained at room temperature, the driver temperature could be raised to 60°C without appreciable change in the driver output waveform.

The driver switching time is primarily determined by the time taken to reverse the remanent flux in the phaser toroid. At S-band the driver cycle time, comprising one SET and a RESET operation, is approximately 10 microseconds. The maximum PRF of 15 KHz is determined by the maximum dissipation of the output transistors. The quiescent dissipation is negligible.

Conclusion

An integrated transistor driver for providing analog control of a ferrite phaser has been described. The flux drive mode of operation provides relative freedom from temperature sensitivity and effects of tolerances. High PRF's, relatively fast switching speed and accurate phase setting have been demonstrated.

Acknowledgement

We wish to acknowledge the invaluable contributions of Max Cottrell and his colleagues at Fairchild Semiconductor Corporation in realizing the integrated circuit configuration described in this paper.

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2. W.J. Ince, and E. Stern, "Nonreciprocal Remanence Phase Shifters in Rectangular Waveguide," IEEE Transactions, MTT-15, pp.87-95 (1967).

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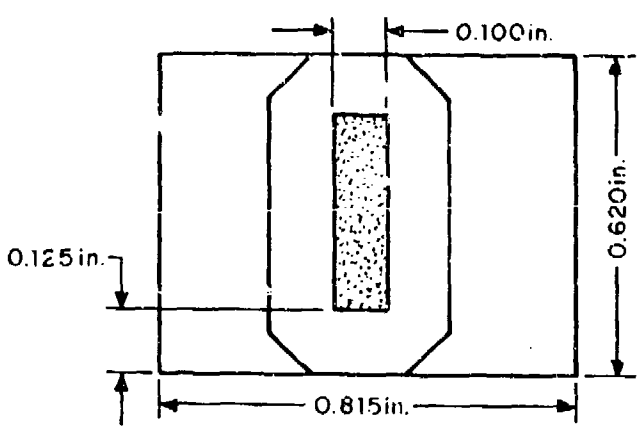
TABLE 1

S-BAND PERFORMANCE OF PHASER-DRIVER COMBINATION

Toroid Material	Mn-Doped Garnet ($4\pi M_s$ = 550 G)
Remanent Magnetization	415 G
Dielectric Constant of Insert	38
Figure of Merit	720 deg per dB
Maximum Peak Power (instability thre hold, f = 2.8 GHz)	7 KW
Maximum Average Power* (conduction-convection cooling)	500 W
Driver Cycle Time	10 μsecs
Maximum Driver PRF	15 kHz
R.M.S. Error of Any Bit Setting Using 4-Bit Digital Flux Drive*	< 3 deg
Switching Energy (total energy per cycle delivered by driver power supply)	630 μJ

* Frequency = 2.8 – 3.2 GHz



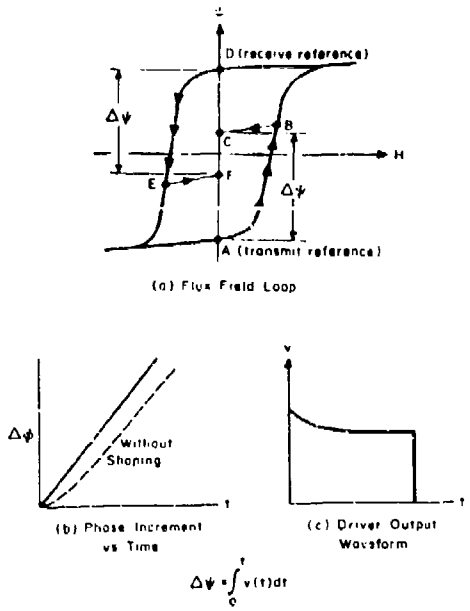


Fig. 1 Illustration of Flux Drive Principle (a) Hysteresis loop trajectory, (b) Phase-time characteristic, (c) Driver waveform for linearizing phase-time characteristic.

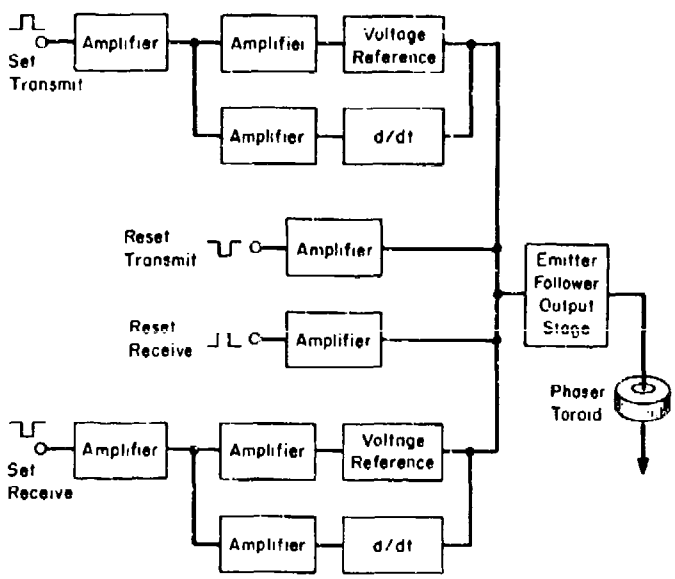


Fig. 2 Block Diagram of Driver Circuit.

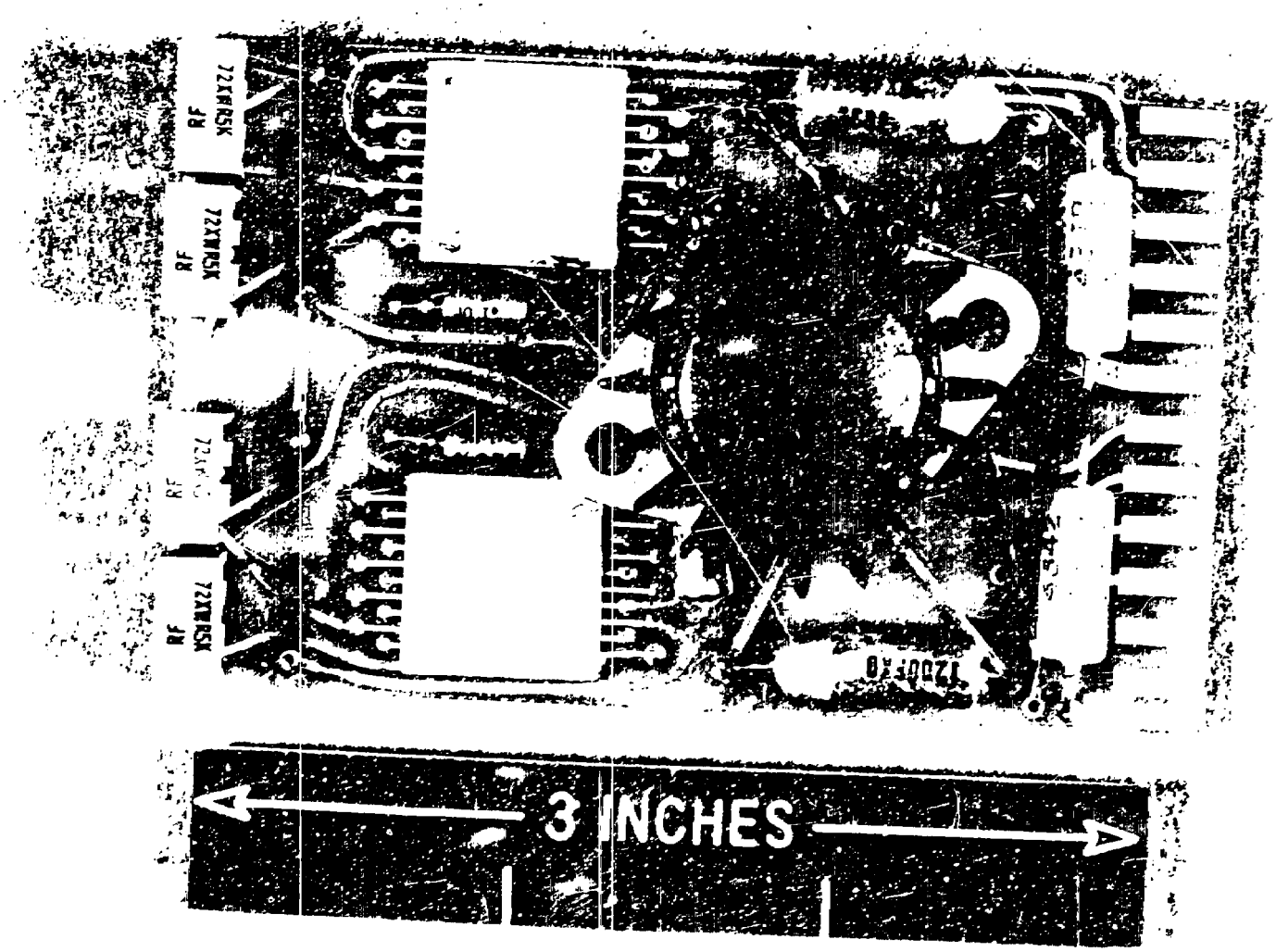
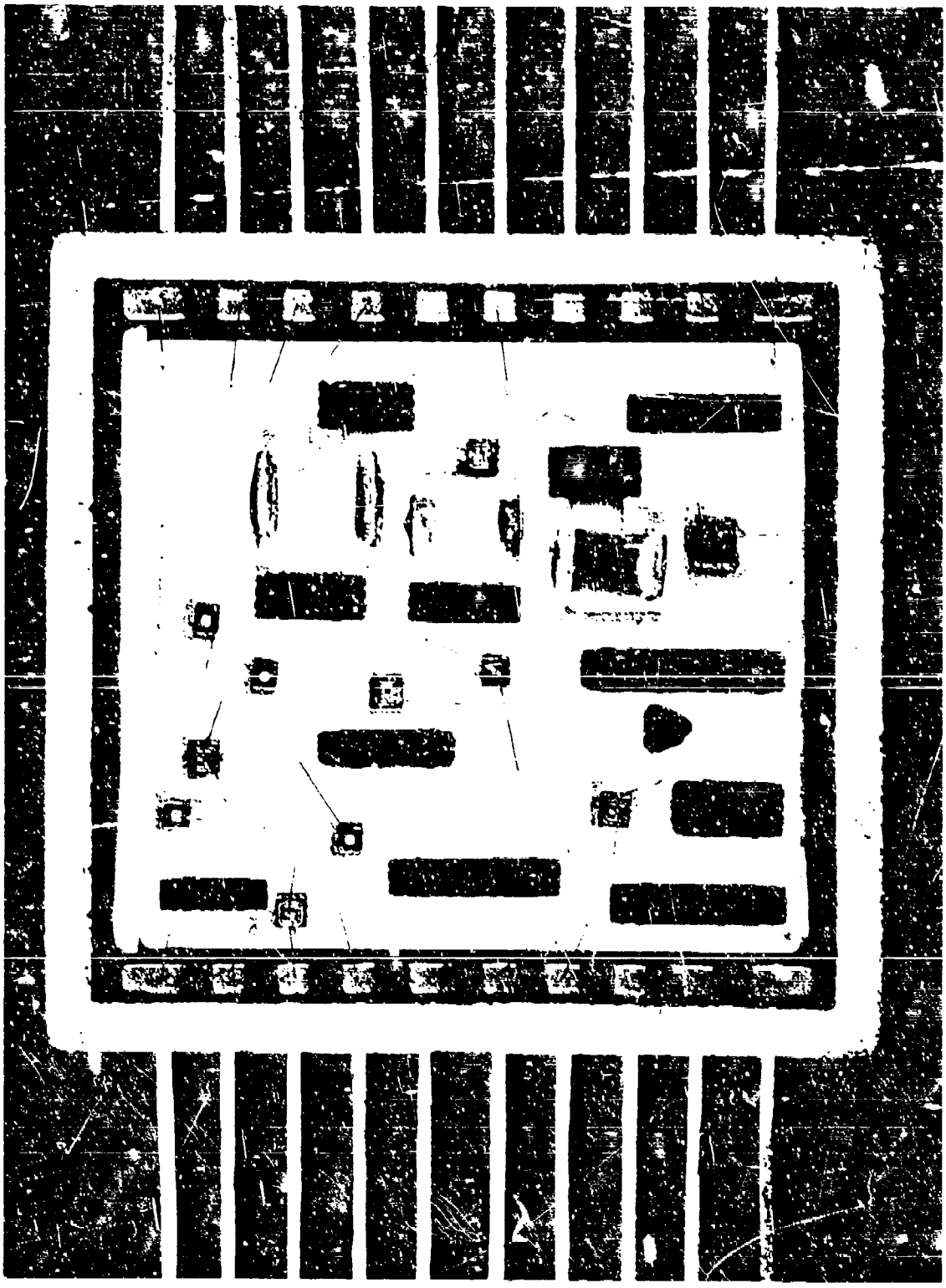


Fig. 3 Layout of Dr ver Circuit



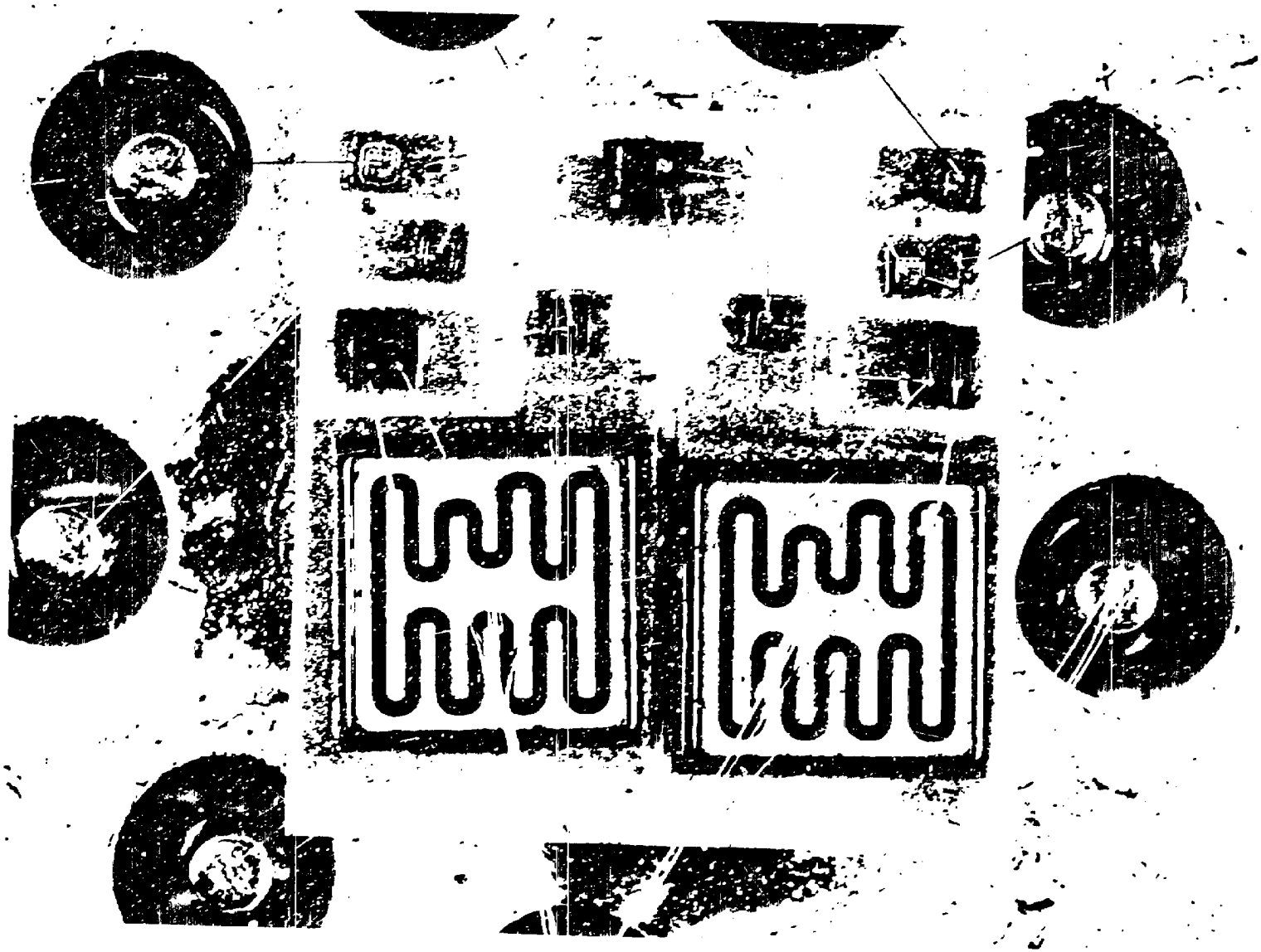


Fig. 5 Layout of Driver Output Stage.

DIAMOND: A New Approach to Microelectronic Circuit Design*
(Dielectrically Isolated Arrays of MONolithic Devices)

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ABSTRACT

DIAMOND is an approach to microelectronic circuit design which reduces many of the problems associated with the design and procurement of radiation-tolerant integrated circuits. Building block standardization is achieved while allowing special purpose circuits, when required.

INTRODUCTION

The development of radiation hardened semiconductor circuits is expensive and time consuming. DIAMOND is an approach to microelectronic circuit design which reduces many of the problems associated with the design and procurement of radiation-tolerant integrated circuits. In the past, a hardened circuit was first breadboarded using a collection of hardened discrete devices. These devices may have come from many different processes and many different vendors. The circuit was then subjected to the radiation environment and its performance evaluated. The breadboard allowed the designer to finalize the schematic diagram, but he was still faced with the problem of designing an integrated circuit of equal performance. Typically, the first integrated circuit did not perform correctly and various iterations were required. Once the circuit was performing properly, some general information about designing hardened IC's had been gained but most of the information pertained only to that particular circuit. When a new IC was required, the trial and error process was repeated.

In the DIAMOND approach, a group of standard discrete components is designed, developed, and characterized for all anticipated environments. These standard discretes are identical to the devices which will ultimately be used to build integrated circuits. Our standard list of devices is intended to be dynamic, and will change as the technology advances or the needs of the circuit designer change. Such an approach will preclude the problem of devices becoming obsolete before they

*This work was supported by the U. S. Atomic Energy Commission.

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appear on the list. Building block, or breadboard, integrated circuits have been constructed by other investigators. Some of these were for radiation hardened applications[1,5,6] and others were for more benign environments[2,3,4]. None featured individual device characterization.

DIAMOND APPROACH

The philosophy of the DIAMOND approach to circuit design is as follows: Given an electronic system, extract the process uniform, regionally located groups of discrete components and design integrated circuits to replace them. These two underlined concepts are defined below.

(a) Process Uniform: A group of electrical components whose important parameters are such that the components could all have resulted from the same sequence of manufacturing processes are process uniform. For example, all the components in any integrated circuit are process uniform. Two transistors of different current rating but of the same voltage rating are usually process uniform. Two transistors with widely different breakdown voltages would probably not be process uniform because different starting collector resistivities are required.

(b) Regionally Located: If one were to partition a schematic diagram into "proximity" groups, those components in one of these groups are regionally located. If a block diagram of the schematic is constructed, there is a high probability that all those components in any block are regionally located.

The DIAMOND approach provides a systematic way to fulfill circuit and system needs over a wide range of economic and environmental conditions (e.g., time scales, production quantities, design iterations, and adverse environments) and yet achieve highly reliable, radiation-tolerant parts at a reasonable cost. The components discussed are all designed to have gold beam leads for attachment. However, the approach is general and not limited to a particular attachment technique.

The initial step in the development of the DIAMOND approach is to divide the most frequently used portion of the current/breakdown voltage plane for transistors into rectangular regions. At least one transistor is developed which meets the I-V requirements of each region. The transistor types are developed in both the gold-doped and non-gold-doped versions. Zener (emitter-base) and signal diodes (base-collector and base-emitter) are realized by utilizing existing transistor junctions. Capacitors are either metal-oxide-semiconductor or reverse biased PN junctions. Schottky clamping diodes are provided for the NPN transistors. A full range of diffused and thin-film resistors have also been developed to be compatible with any of the process uniform groups.

Circuits with comparable performance can be obtained in three forms: (1) Discrete Hybrid, (2) Standard Layout DIAMOND, and (3) Custom Layout

DIAMOND. The choice is dictated by the design time allowed, quantity required, and the allowed circuit volume. The flow diagram followed in making the decision is shown in Figure 1.

The components developed are completely characterized in design handbooks and modeled over the environments of interest thus making circuit analysis accurate. These devices are stocked in beam lead chip form and in DIP packages and are readily available for building breadboards. In-house hybrid fabrication facilities and an interactive graphics system make possible the completion of initial circuit design to finished discrete hybrid in as short a time as one week.

DIAMOND DEVELOPMENT

The first portion of the DIAMOND development consists of twelve basic transistor types using beam lead and radiation-tolerant technologies. The twelve types include NPN and PNP transistor arrays with BV_{CEO}'s of 10 and 35 volts representing three separate operating current ranges. The twelve basic transistor types are expanded to twenty-four types by providing each basic device in both gold-doped and non-gold-doped versions. These transistors are provided in the form of quad transistor arrays. A small real estate penalty and negligible dollar cost allowed us to develop quads instead of single transistors. The quad form greatly enhances the amount of characterization data available. Singles can easily be fabricated if the larger area units prove to be undesirable. All four transistors in an array have the same current and voltage ranges. Each quad transistor array contains two gold-doped transistors and two non-gold-doped transistors. One non-gold-doped and one gold-doped transistor of each NPN array have Schottky diodes build into their collectors but not connected to the base. The PNP arrays contain regular PN junction diodes since useful Schottky diodes cannot be fabricated on the p-type collector material. A schematic representation of the NPN array is shown in Figure 2. The actual arrays contain fourteen gold beam leads and the silicon chip size is .040"x.050". In breadboarding, only one or two devices from each quad are normally used.

In order to gain the statistical confidence required for computer modeling, three different lots of each of the twelve transistor types have been processed. From each lot 400 arrays (14,400 total units) were obtained. Half of each group was packaged in dual-in-line packages. The dual-in-line units are useful in conventional breadboards and in device characterization by automatic testers.

The second portion of the DIAMOND development will consist of the Standard Layout DIAMOND (SLD). On this chip will be a collection of three current ranges of transistors, diffused resistors and cross-unders. These circuits will be stocked by the supplier with all the processing complete except the final metallization. If an integrated circuit can be realized using only components from this collection, interconnection instructions are sent to the supplier who then applies the appropriate metallization for the particular application. In this manner, small quantities of fully characterized integrated circuits may be obtained

quickly (approximately 4 weeks) and at low cost (a few thousand dollars).

A tentative drawing of the Standard Layout DIAMOND constructed on the Sandia interactive graphics facility is shown in Figure 3.

If the UDIC[5] and Sandia Video Amplifier[6] had been fabricated from DIAMOND-characterized discrete devices, they would be examples of Custom DIAMOND circuits. Development times for these types of circuits should be 16 to 20 weeks, and even though the cost will be more than that of SLD's, it will be considerably less than a conventional custom hardened circuit.

DEVICE PERFORMANCE

Table 1 shows typical device performance. The typical values given are the preradiation values of the non-gold-doped units. Although arrays of all of the types have not been received or irradiated at the time of this writing, Figures 4 and 5 show the performances of early prototype versions of the 10 volt NPN 2mA and 10mA transistors versus neutron dose.

ACKNOWLEDGMENTS

The devices for this portion of the DIAMOND development were fabricated by Texas Instruments. The authors especially acknowledge the efforts of Tim Smith, Walt Runyan and their staff in bringing the DIAMOND concept into reality.

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5. Gray, R. M. and D. G. Skogmo, "UDIC (Universal Digital Integrated Circuit)," This Publication.

6. Gray, R. M. and T. D. Petty, "Radiation Tolerant Gated Video Amplifier," This Publication.

TABLE I

Process Uniform Category	Array Number	Beta Peak Current	H_{FE} [V_{CE} = 5.0V, I_C = 8 peak current]	$V_{CE(SAT)}$ [β = 10, I_C = 8 peak current]	$V_{BE(SAT)}$ [β = 10, I_C = 8 peak current	BV_{EBO} [I_E = 10 uA]
D(NPN - 10 volt BV_{CEO})	D1	2 mA	50	.2V	.75V	6.5V
	D2	10 mA	50	.3V	.8V	6.5V
	D3	100 mA	50	.4V	1.0V	6.5V
E(NPN - 35 volt BV_{CEO})	E1	2 mA	50	.25V	.75V	6.5V
	E2	10 mA	50	.35V	.8V	6.5V
	E3	100 mA	50	.5V	1.0V	6.5V
F(PNP - 10 volt BV_{CEO})	F1	2 mA	50	.3V	.75V	7.3V
	F2	10 mA	50	.6V	.8V	7.3V
	F3	100 mA	50	2.0V	1.0V	7.3V
G(PNP - 35 volt BV_{CEO})	G1	2 mA	50	.4V	.75V	7.3V
	G2	10 mA	50	.9V	.8V	7.3V
	G3	100 mA	50	4.0V	1.0V	7.3V

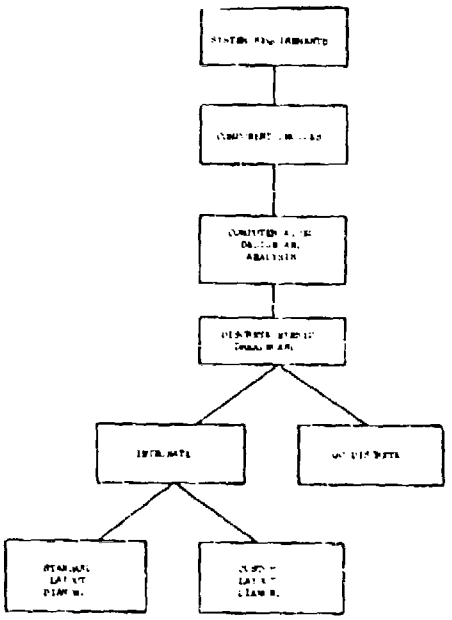


FIGURE 1

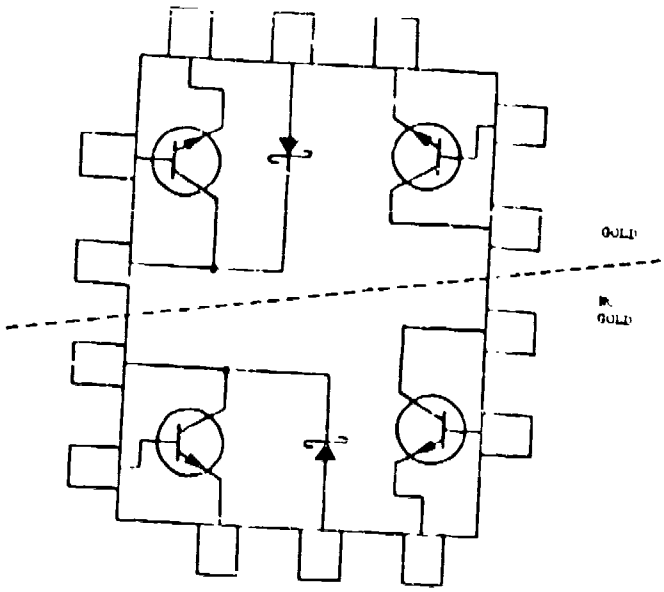
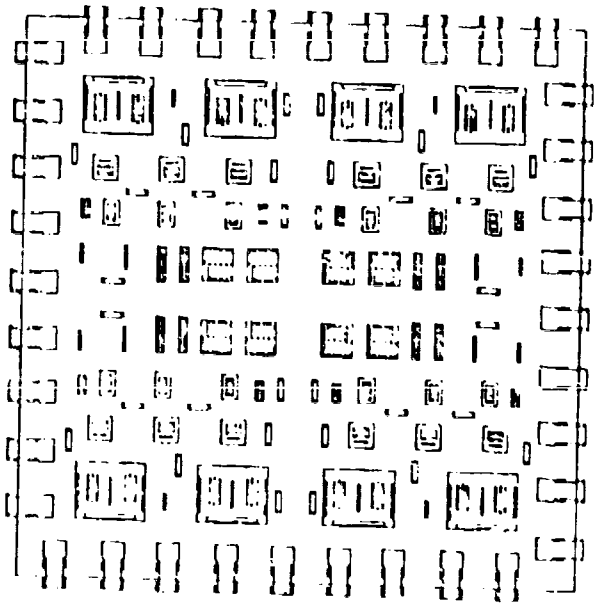
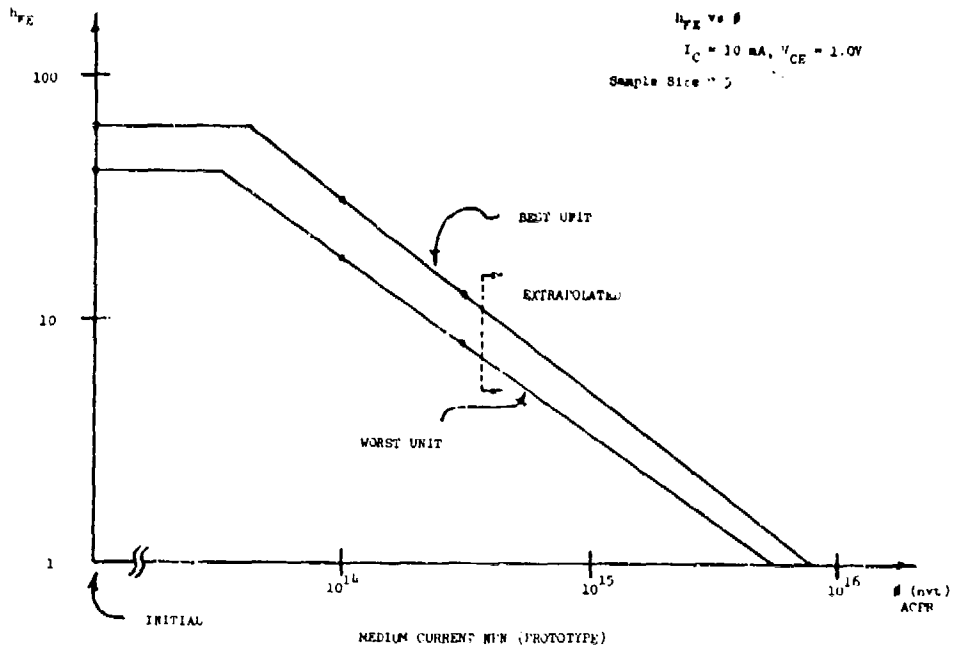


FIGURE 2

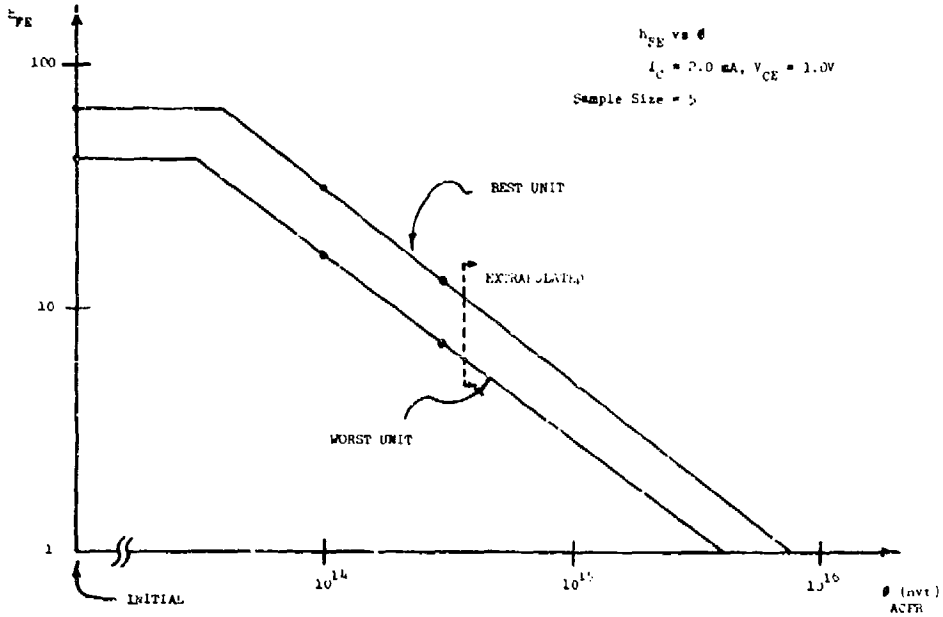


EXAMPLE OF STANDARD LAYOUT DIAMOND



MEDIUM CURRENT NPN (PROTOTYPE)

FIGURE 5



LOW CURRENT NPN (PROTOTYPE)

FIGURE 4

FLEXIBLE MULTILAYER INTERCONNECTION USING EVAPORATED ALUMINUM CANTILEVERED BEAMS

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Baltimore, Maryland

ABSTRACT

A compatible multilayer interconnection system including the formation of cantilevered aluminum beams for interconnection of standard chips or very large LSI wafers is described. This packaging technique has all the advantages of an all-aluminum system with the possibility of semiautomation.

INTRODUCTION

This paper describes a technique of interconnecting any type of off-the-shelf integrated circuit with aluminum cantilevered beams that is integral to the metallization on the two surfaces of a flexible film through the elimination of flying wire bonds. The technique is used before the integrated circuits are mounted backdown in intimate contact to a heat sinking substrate. This method of subsystem packaging, for military or commercial application, may utilize double-sided or three-layer construction. The beam lead and bumped flip-chip integrated circuits suffer from the disadvantage that the active surfaces of the I/C's are not visible for inspection and test, and are not effectively cooled.

DESIGN CONSIDERATIONS

General

New techniques for device attachment to flexible Kapton film were developed with provisions for backdown mounting of the interconnected devices. These techniques required etching of 0.005-inch Kapton, fabrication of cantilevered aluminum beams on Kapton, and mounting of the preconnected chip arrays to alumina substrates.

Beam-Leads on Kapton for Device Attachment

The requirement that devices be mounted face up on substrates while being interconnected by double-sided metallized Kapton film places certain restrictions on the geometry. The design of the carrier provides cantilevered beams extending over large etched windows in the Kapton film for attachment to the devices. This allows for device removal after all bonding is completed. The film is also attached to the substrate by bonding the aluminum on the lower side of the Kapton to the substrate so the beam leads are not stressed. The thick flexible film (0.005 inch) approximates the device thickness and the flexibility of the beams enables stress loops to be formed to accommodate any slight misalignment. Figure 1 illustrates the method used to connect to the devices.

Circuit Selection

A sense amplifier circuit was designed, breadboard tested, and fabricated in final form as part of the verification of the cantilevered beam for the multilayer hybrid packaging technique.

Conductor Deposition

The vacuum equipment used consisted of a 26-inch-diameter stainless-steel bell jar, a 10-inch-diameter oil diffusion pump, and a film thickness monitor. Figure 2 shows the electron beam evaporation system.

One of the primary goals was to produce aluminum films that have good adhesion to Kapton. The cleaning procedure which proved most effective consisted of outgassing the Kapton by placing it in the chamber and pumping to a pressure between 1×10^{-6} torr to 5×10^{-7} torr with 500 watts dissipated by heaters placed 2-1/2 inches above the Kapton film. Omitting the initial outgassing step invariably produced poor aluminum adhesion. After this outgassing, the sheet was removed for further cleaning, reinserted in the chamber, and pumped to a pressure somewhat higher than the initial outgassing pressure for the aluminum deposition.

In order to etch the through holes in Kapton film, both sides of a 10-inch sheet were deposited with about 0.004 inch of aluminum. After one side was coated, the sheet was removed from the vacuum chamber and to attach the lower aluminum layer on the Kapton to the gold layer on the ceramic substrate. Access holes were etched in the Kapton from the top down to the lower aluminum layer. These holes were etched when the rectangular chip access holes were etched from the bottom side up. The thermal compression bonds were made with a

wire bonder. The substrate was held at 200°C and the capillary was held at 350°C.

A SECOND APPLICATION

Another application for the technique of etching aluminum conductors on flexible film is interconnecting a 3-inch-diameter wafer or substrate to its package. The initial interconnection concept consisted of 0.001-inch-thick pure aluminum conductors cantilevered over both edges of the film for interconnection to the substrate at one edge and to the package pads at the other edge. This configuration yields repeatable tight tolerance (hence constant capacitance) of relatively long conductors which can be of considerable importance in high-speed applications. Part of figure 6 shows this initial design.

The second interconnection technique, which is rather unique, is called the removable carrier design. The deposition and etching processes are essentially the same as described in the first part of this paper. The difference is in the geometry of the finished aluminum beams and the Kapton. The aluminum leads are cantilevered over a window etched in the Kapton film. Once the part is in position, the bonds are made inside the window where the beams are hanging. The Kapton is then pulled away, leaving only aluminum beams as shown in figure 7. Note that the beams have separated outside the bond. The most obvious advantages of the removable film carrier design are that there is no Kapton in the final assembly and that the beams are better protected during handling since the ends of the beams are not free as in the initial design. Figure 8 shows the ultrasonic bonder with the tip in operation to interconnect the large modular package.

Cantilevered beam interconnections 0.010- x 0.001-inch in cross-section can attain a pull strength of between 80 and 82 grams. Compared to gold flying wire bonding, the advantage in specific strength is over four to one.

CONCLUSIONS/SUMMARY

The technique of using cantilevered aluminum beams was devised to provide multilayer capability with a reduced number of interconnections. This method of microcircuit packaging uses the two layers on the Kapton to replace gold wire connections. The face up mounting of the chips provides good heat transfer, ease of inspection and test, and in-process replacement capability.

The aluminum beam lead carrier used to connect a wafer or a substrate to a package was developed to provide a reliable, radiation-hardened, low-cost interconnection technique. The vapor deposited metal can be chosen to conform to other materials in the package and the photoetching techniques lend themselves to speed and accuracy.

ACKNOWLEDGEMENT

The development work described in this paper was sponsored jointly by Naval Air Development Center and the Naval Air Systems Command. We are thankful for their technical direction.

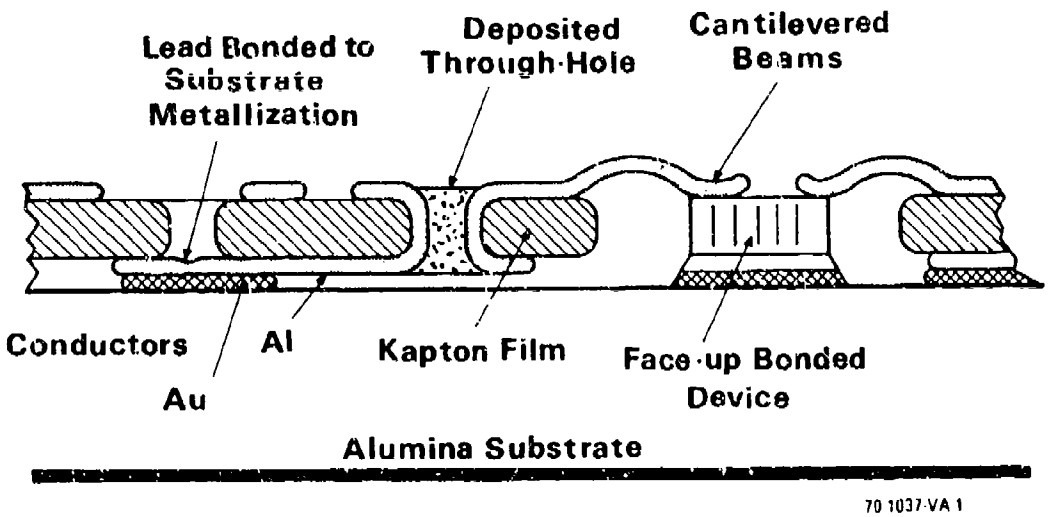

Figure 1. Cross-Section of Face-Up Device Bonding

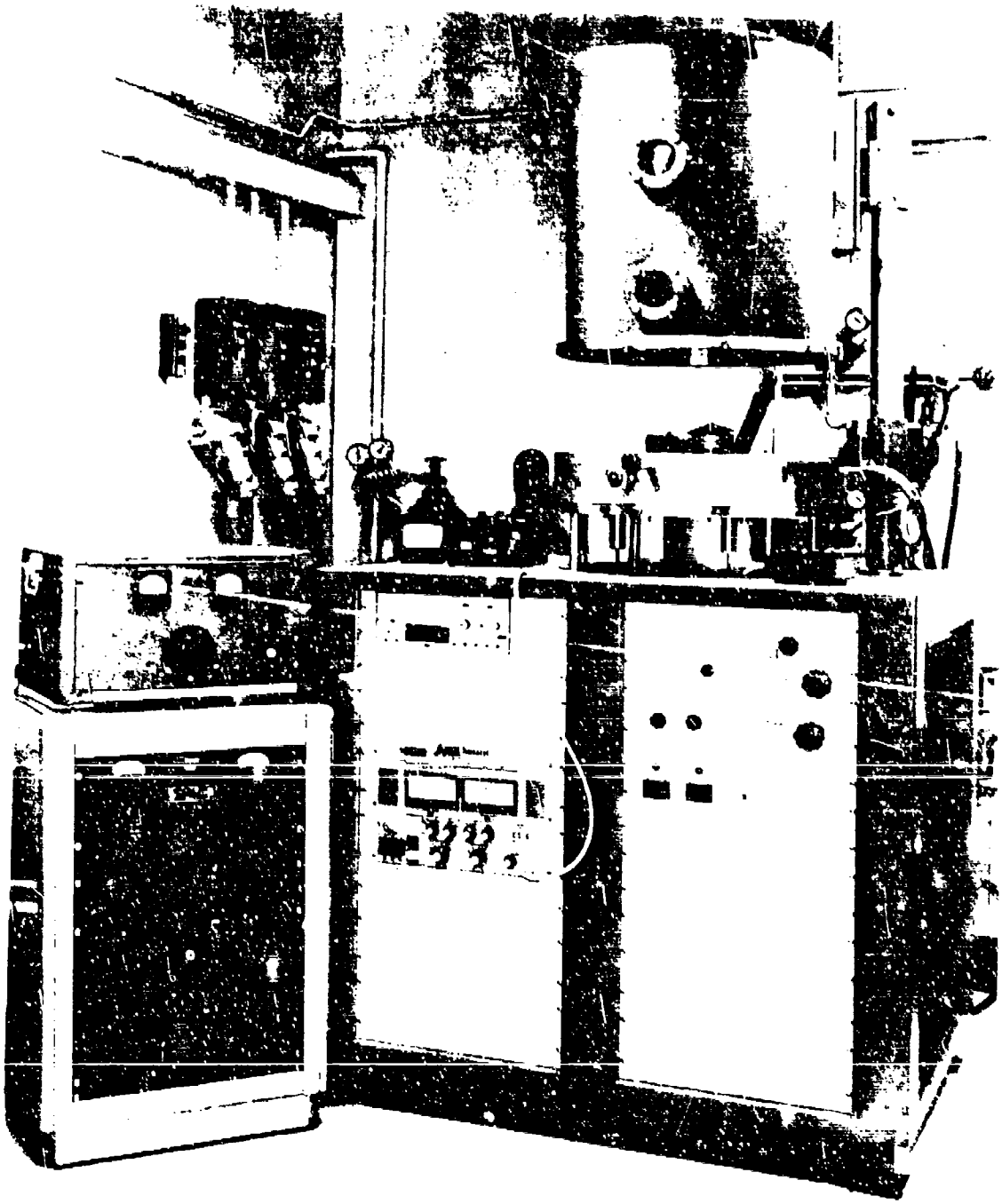

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Figure 2. Electron Beam Evaporation System

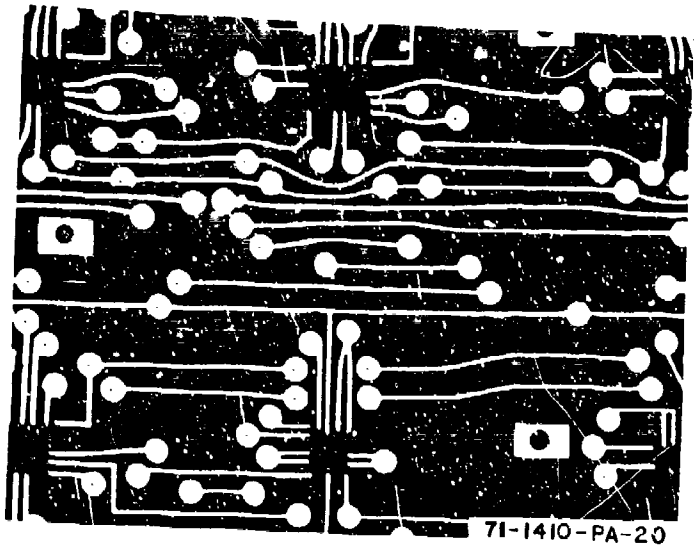

Figure 3. Etched Aluminum Circuit on Kapton

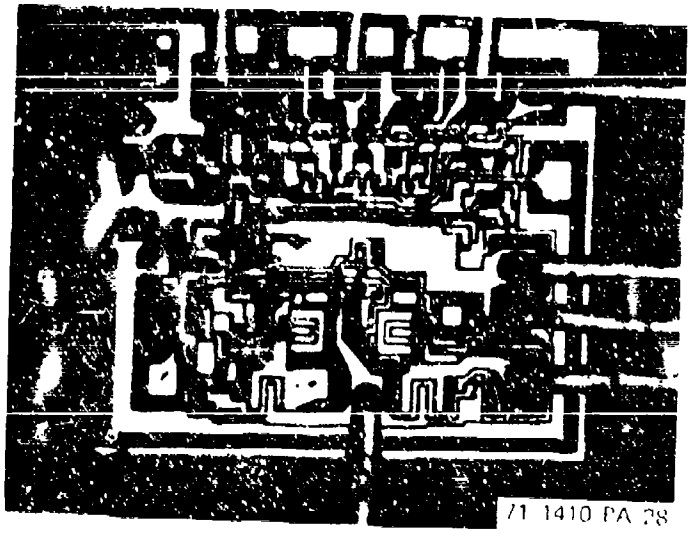

Figure 4. Closeup of Same Bonded Chip

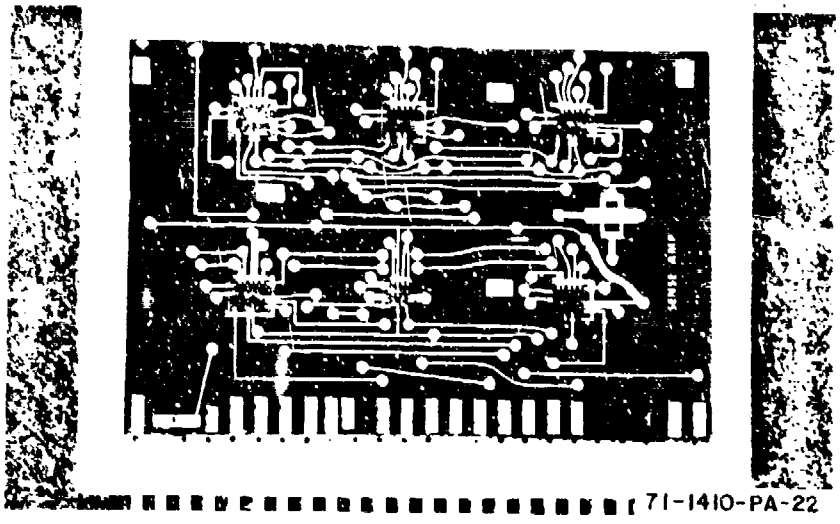

Figure 5. Assembled Sense Amplifier
Note: Cantilevered beams are 4 mils wide by 16 mils long

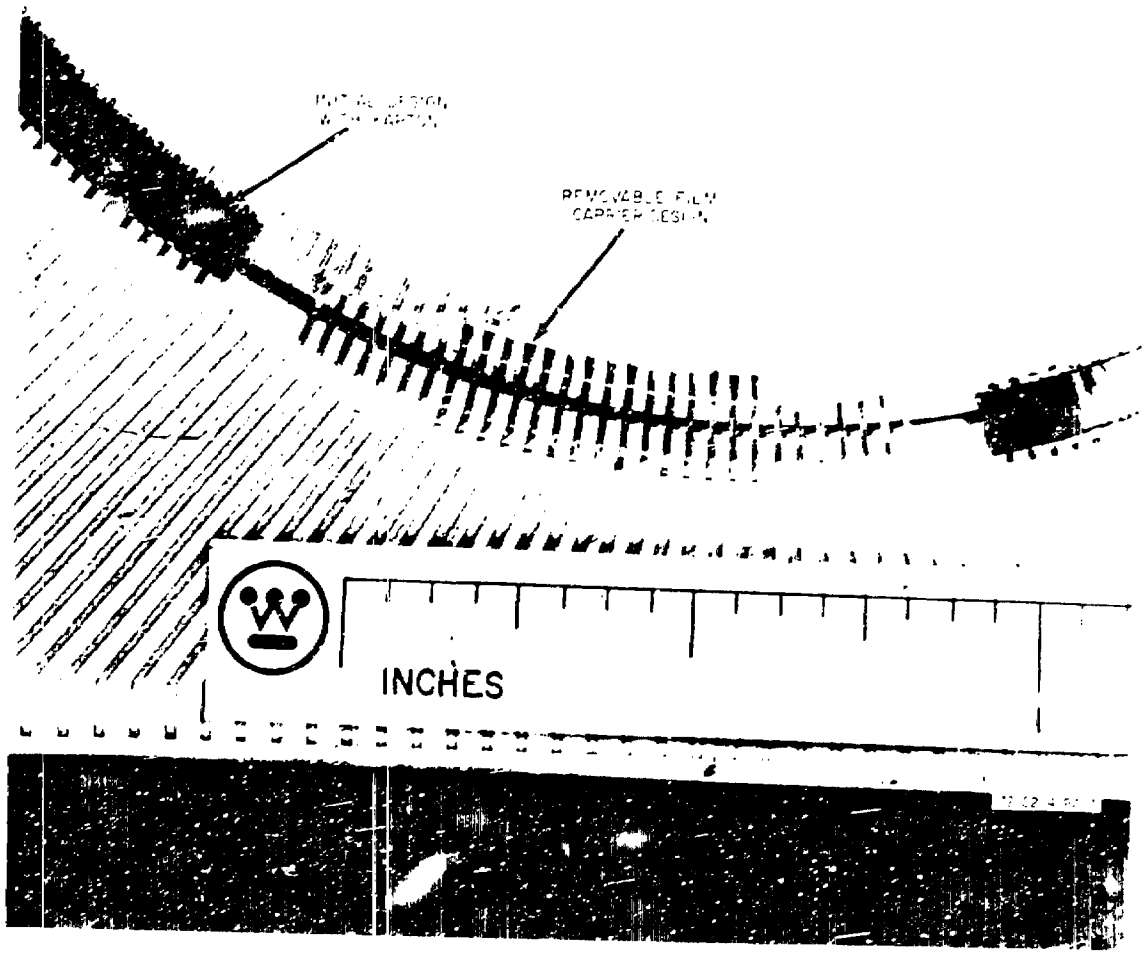

Figure 6. Comparison of Interconnection Designs

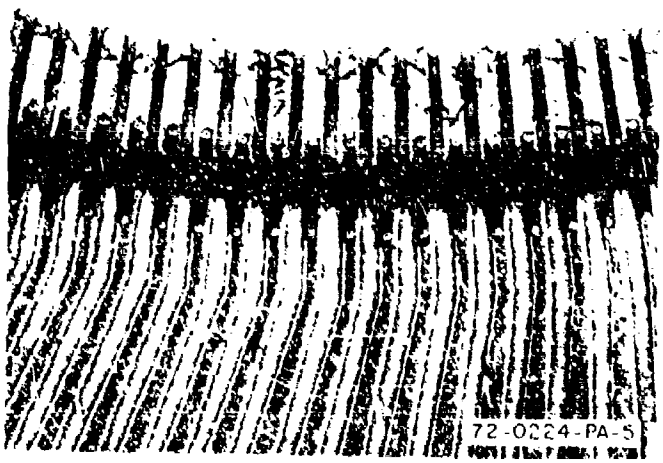

Figure 7. All-Aluminum Interconnections

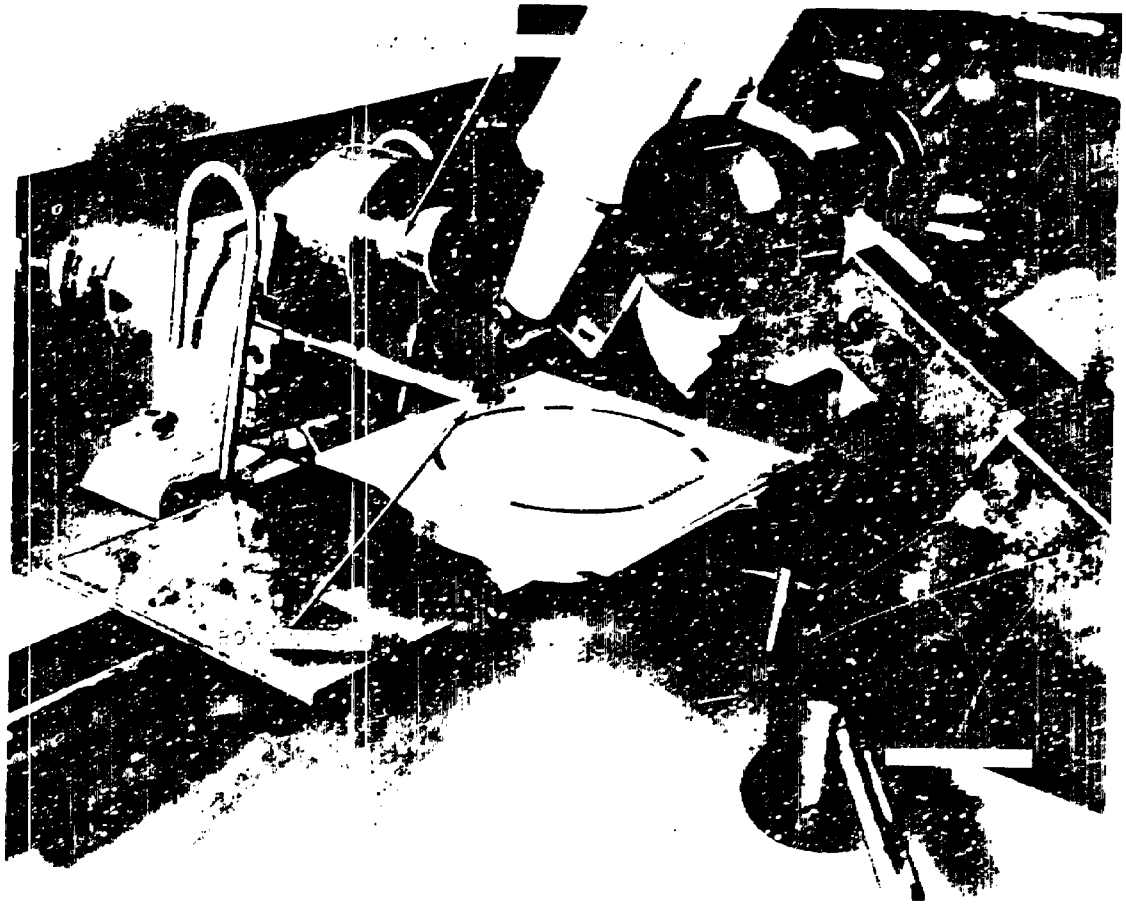

Figure 8. Closeup of Ultrasonic Bonder

TITLE: One-Mil Gold Wires in High Acceleration HMC Applications

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ABSTRACT

Results of an evaluation of one-mil gold wires as used for intraconnections in hybrid microcircuits for high acceleration artillery shell applications are reported. Wire orientation and length control are necessary for successful use in this environment.

INTRODUCTION

Since hybrid microcircuits were first produced in industry, one-mil (0.001 inch) gold wires have been favored for reasonably reliable intra-connections on hybrid microcircuit (HMC) substrates. They have been used for the electrical connections of nearly all types of applique devices such as chip capacitors, transistors, and even chip resistors.

Gold wires have been popular because of their ease of handling, their compatibility with the wide range of materials usually centered around a gold film system, and the non-critical nature of bonding parameters, especially when compared to other techniques. In addition, a level of gold wire bond integrity can be established by a high level centrifuge with forces in such a direction as to lift the wires from the substrate or components. Figure 1 depicts this force application.

The latter advantage is a disadvantage when the forces are in the wrong direction. For example, if the forces of the centrifuge were against the wire loop (Figure 2) the lack of bending strength in the gold could allow it to collapse to the substrate surface causing possible electrical shorting to substrate metallization or the component edge.

The same problem can occur with application of high level forces in other directions. Under these conditions, the wire loops can move to the side or end, causing possible shorting to other electrically conducting components.

Despite this movement that can be experienced, the wire bonds themselves can be expected to retain their original configuration through reasonably high force levels, i.e., in excess of 20,000 g. Thus, if gold wire movement could be controlled in high acceleration environments, their use in force levels in execess of that to bend the gold wire is possible.

To evaluate fully the gold wires in orientations where collapse is possible, a centrifuge test was established where controlled forces could be placed on the HMC's and the results monitored after each of the force steps.

CONCLUSIONS

This evaluation showed a definite difference in the gold wire capabilities in relation to its orientation. The one-mil gold wires, when controlled to 0.050 inch between bonds and a height of 0.015 inch can withstand side forces (Figure 3b) up to 14,000 g. The same wire with forces pushing down (Figure 3a) can be used to 16,000 g and when subjected to forces in its longitudinal direction (Figure 3c) up to 20,000g.

This report also investigates the effect of over all wire length on the ability of the wire to withstand forces in the various directions. As might be expected, wire length is a critical parameter. Wires 80-mils long deflected at only 10,000g.

The force level is also an important factor in the amount of deflection. The wire does not just collapse when it reaches its yield point. Instead, it moves a little at that force level and then a little more at the next force level. In few cases did the wire reach total collapse at the levels tested.

TEST PROCEDURE

Ninety 7/8 by 7/8 inch integral packages (leads attached directly to the substrate) with 105 one-mil gold wires bonded at each end with a natural loop between bonds and 180 5/8 by 5/8 inch integral packages with 50 one-mil gold wires bonded at each end with a natural loop between bonds were exposed to centrifugal forces (Figure 4). This provided a sample of 18,450 wires which were bonded at one end with a thermocompression ball bond and at the other end with a thermocompression wedge bond. Figure 5 shows a typical wire. The packages were obtained from a commercial supplier.

At the suppliers facility, all units were centrifuged at 20,000g in such a direction as to lift the wires from the substrate (such as shown in figure 1). Upon receipt, all units were tested for continuity. These tests confirmed the bond integrity of the wire strings.

Each size package was divided into three groups for centrifuge, corresponding to the centrifuge directions of Figure 3. Each group was then centrifuged in the corresponding orientation of the arrows (Figure 3) at levels of 10,000, 12,000, 14,000, 16,000, 20,000, and 25,000g.

After each increment of force, each package was x-rayed to allow usual examination. This should detect major wire movement that occurred during that level of centrifuging. In addition, to verify bond integrity, an electrical continuity check was made.

Prior to lidding the hybrid packages at the suppliers plant, photographs were made of each substrate. These, plus initial x-rays, were the basis for monitoring wire movement after each centrifuge step.

The contract for HMC packages specified 0.050 inch between bonds. However, not all bonded substrates fulfilled the specification as on many substrates, the bond centers were well beyond the 0.050 inch specified. These substrates were used anyway because the different length wires could provide useful information for comparison at one centrifuge level.

TEST RESULTS

The results of the centrifuge evaluation within the different orientation groups were much the same. Thus, only a representative sample will be discussed. The order of discussion will be for those with forces as shown in Figures 3b, then 3a, and finally 3c.

Figure 6 shows a typical package with the forces pushing to the side. The superimposed photographs are made by overlaying the x-ray negative before centrifuge with that after centrifuge. This particular HMC has

several long wires apparently formed when the original bonds were reworked. As shown by the superimposed x-rays, these longer wires deflected after the 10,000g centrifuge level. Minor movement of the shorter wires can be noted after 16,000g with a pronounced movement of some of the shorter wires noticably deflecting after 25,000g.

With forces pushing the wires toward the substrate, the gold wire capability is greater than with side forces. Figure 7 shows distortion in this direction only above 20,000g. Then, the occurance is only with the longer wires.

The effects of up to 25,000g imposed on the longitudinal direction of the wires produced no observable distortion in any of the units tested. This is true even with those units containing abnormally long wires.

Some care should be taken in assuming that little, if any, distortion of the gold wires occurred during the last two discussed directions, i.e., the forces pushing the wires down or endwise. The x-rays and photographs are all from a vertical direction and would show only a twisting or deflecting action of the wire. Wire movement only in the verticle plane would not be discernible. Such possible motion is depicted in Figure 2. This did in fact happen on some of the longer wires (Figure 8). It is interesting to note that, of those wires observed to have deformed in this fashion, there was still separation between the wire and the substrate surface. Samples were selected from the group after 16,000g and 20,000g for an open lid examination. The verticle motion of the wires with a force to push them to the substrate could not be observed at less than 20,000g. Motion of the wires with longitudinal forces were not observed below the 25,000g level.

A sample of three packages and 293 wires was taken on those units with forces pushing to the side. Each wire was straightened and measured for length. From the x-rays, it was then determined at what level the wire deflected. Figure 9 is a plot of the average values and the range at each level. The end points on each range can usually be related to an unusual shape or excessive loop height. At 12,000g, there is one wire at 55-mils long; the next shortest to be 4 at this level was 63-mils long. Discounting this one point, any wire less than 59-mils in total length should be capable of withstanding 14,000g side acceleration. Fifty-nine mils would typically be a wire 50-mils between bonds with a 15-mil loop height.

APPLICATION

The need for this evaluation arose due to a hybrid microcircuit application in an artillery shell. The setback forces during firing and the rotational forces due to projectile spin were extremely high. The evaluation showed that the wires would not withstand the worst case conditions of either the spin or setback forces when the forces were in a direction to push the wires to the side. To counter this problem, the hybrid microcircuits layouts were changed from a random array (Figure 10) to one where the one-mil gold wires were all oriented in the same direction (Figure 11). In conditions where this was not feasible or long wires were necessary, three-mil aluminum wires were used. This was

possible because of the lower mass and greater bending strength in comparison with gold. The single direction of the gold wires then allows an orientation within the artillery projectile so that side forces will not be experienced.

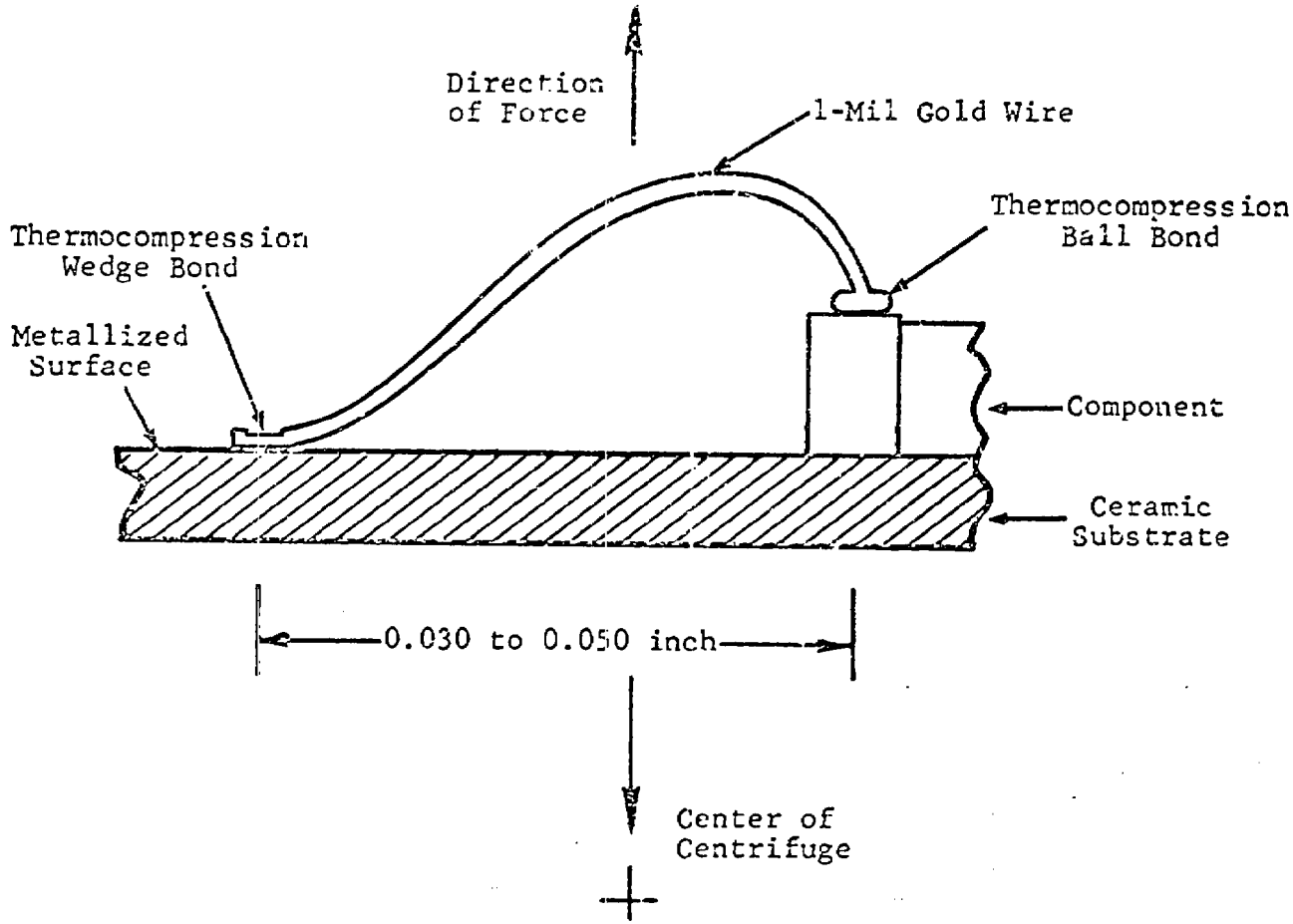


Figure 1. Direction of force to lift wire away from substrate

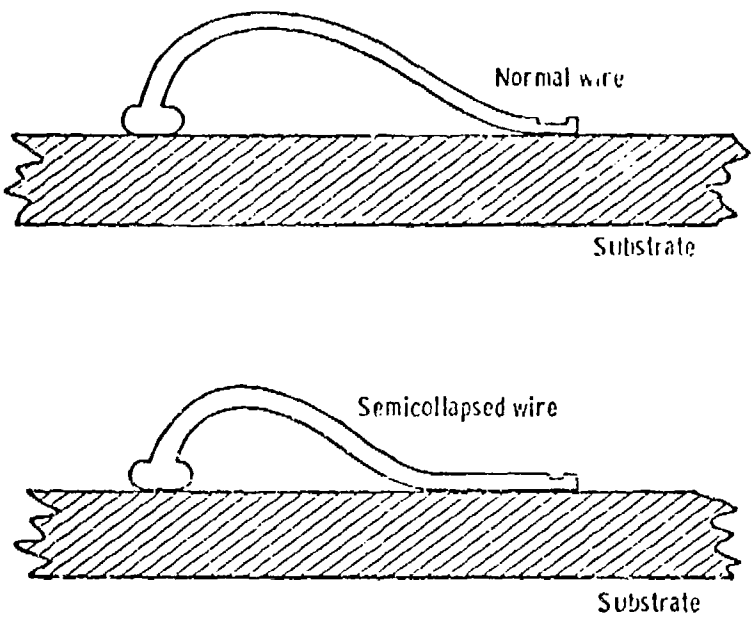
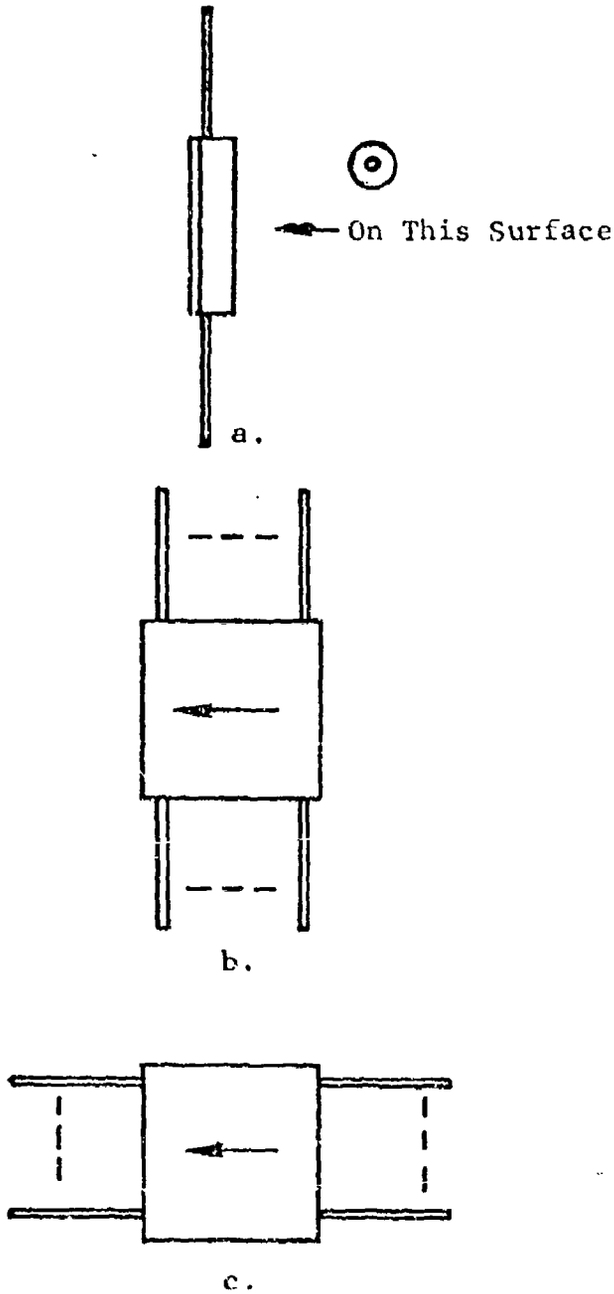
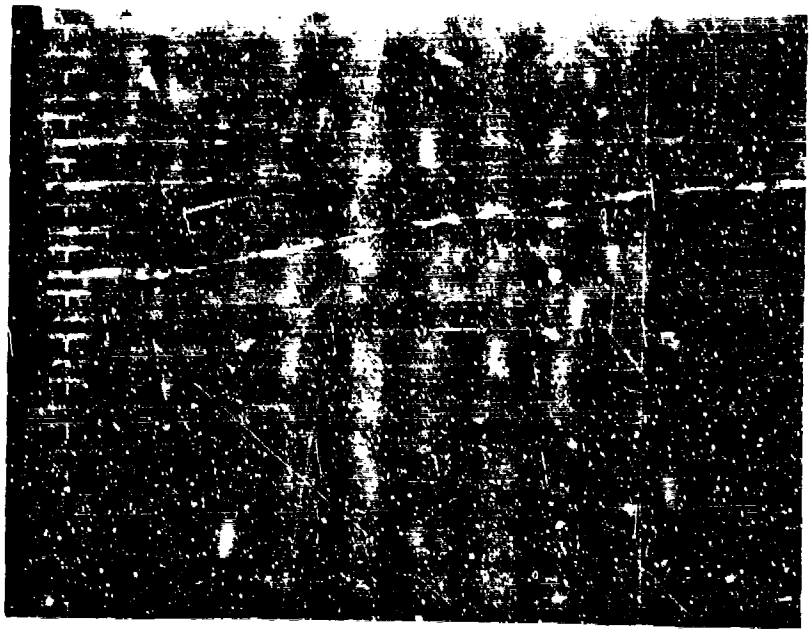


Figure 2. Possible nondiscernible wire motion

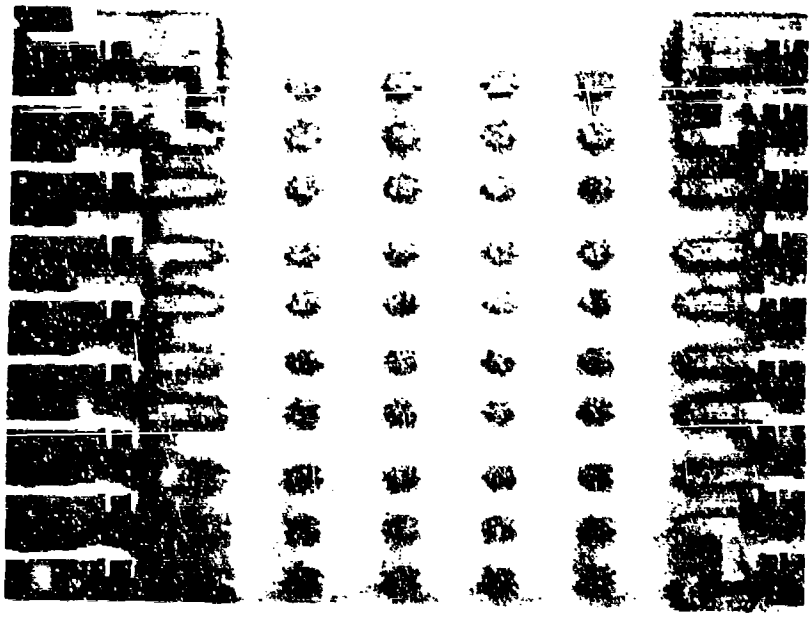


Direction of arrow points
to center of centrifuge

Figure 3. Centrifuge force directions

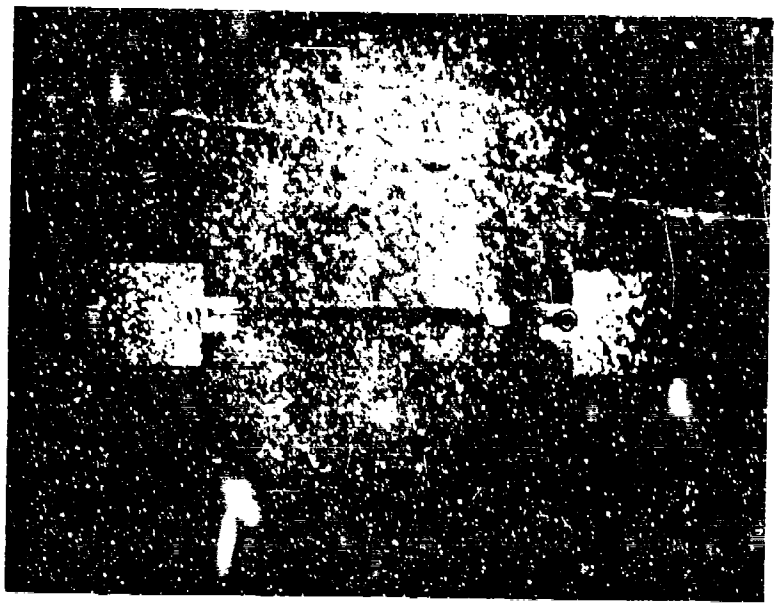


a. Typical 7/8" Square Package

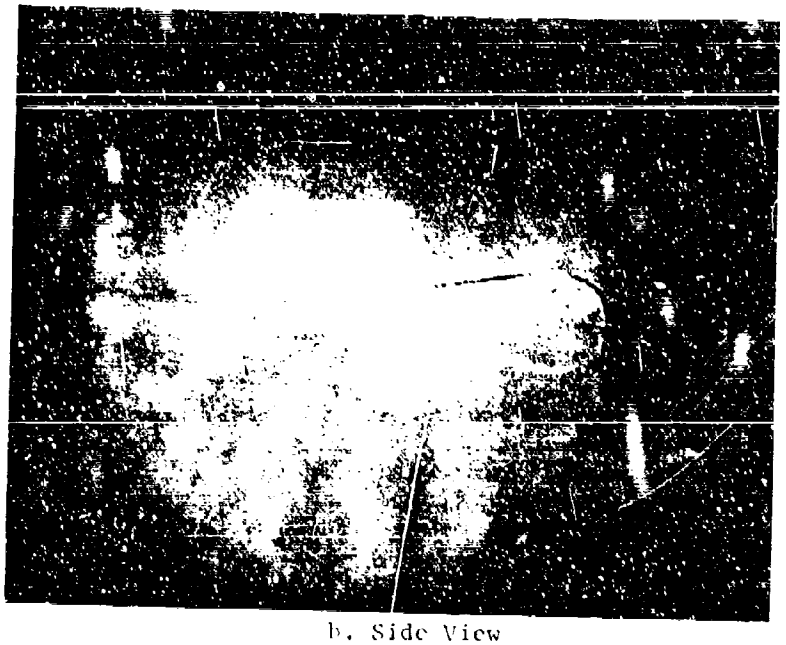


b. Typical 5/8" Square Package

Figure 4. Typical Centrifuged Packages

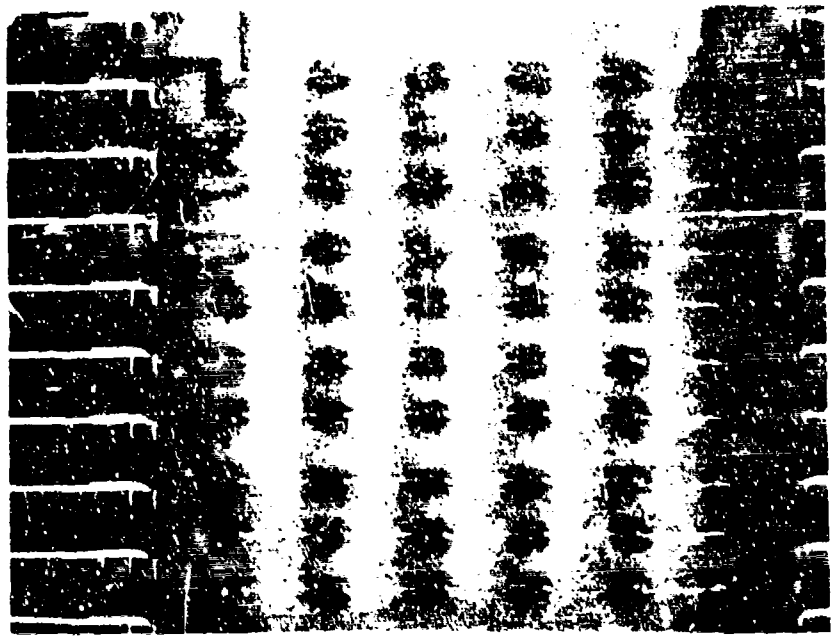


a. Top View

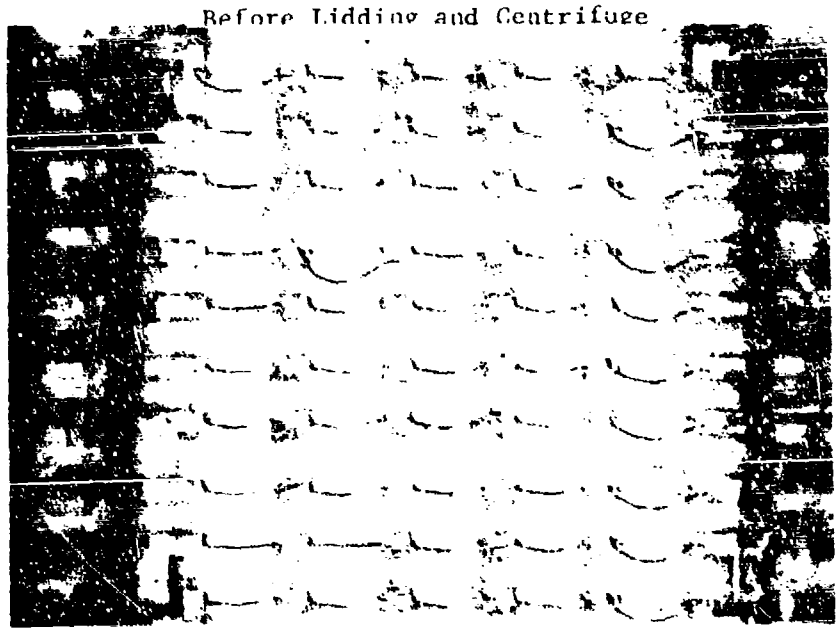


b. Side View

Figure 5. Typical Wire



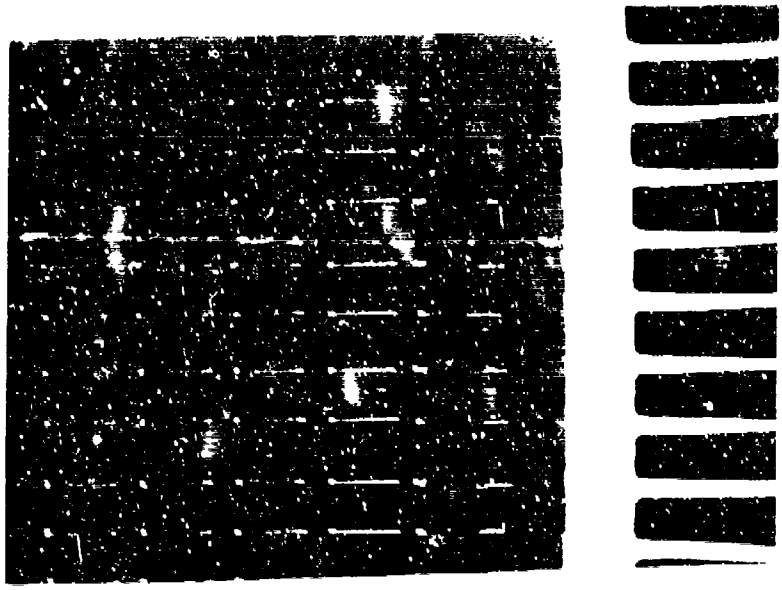
Before Lidding and Centrifuge



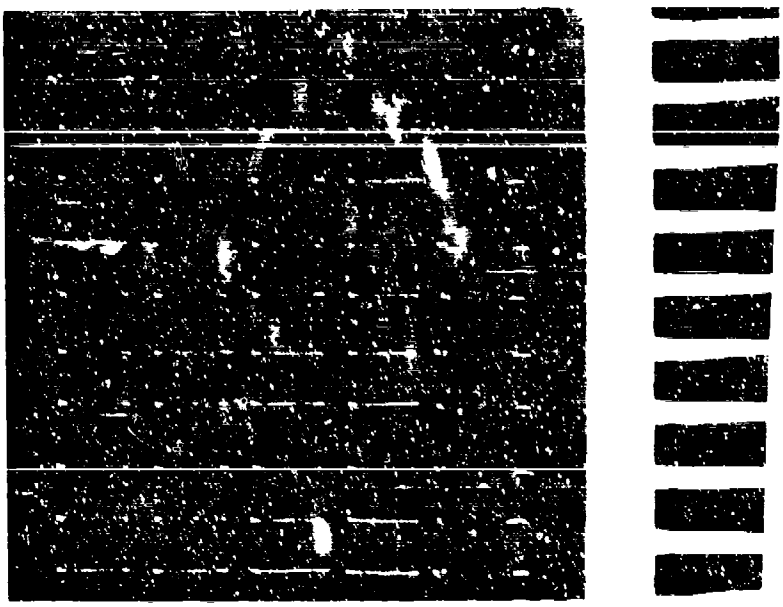
After 25,000g

a. Photographs before Centrifuge and after 25,000g. Forces to side.

Figure 6.

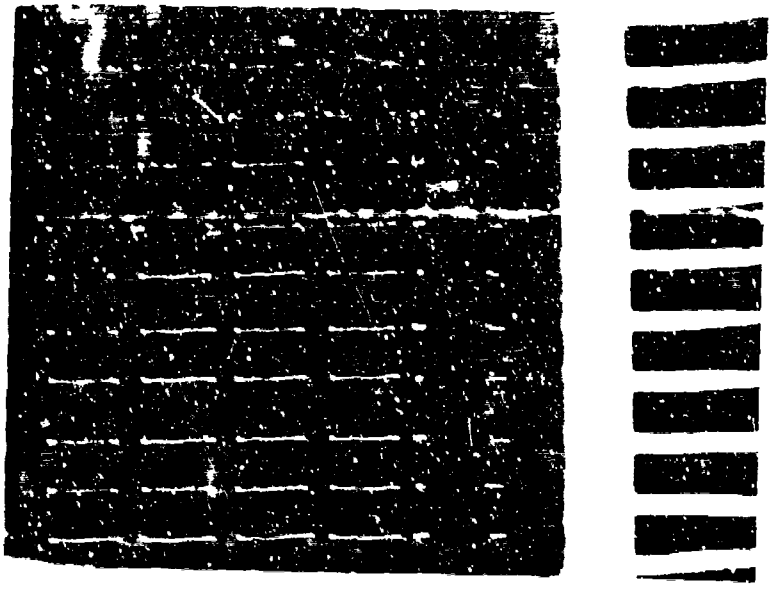


Before Centrifuge and after 10,000g, Superimposed

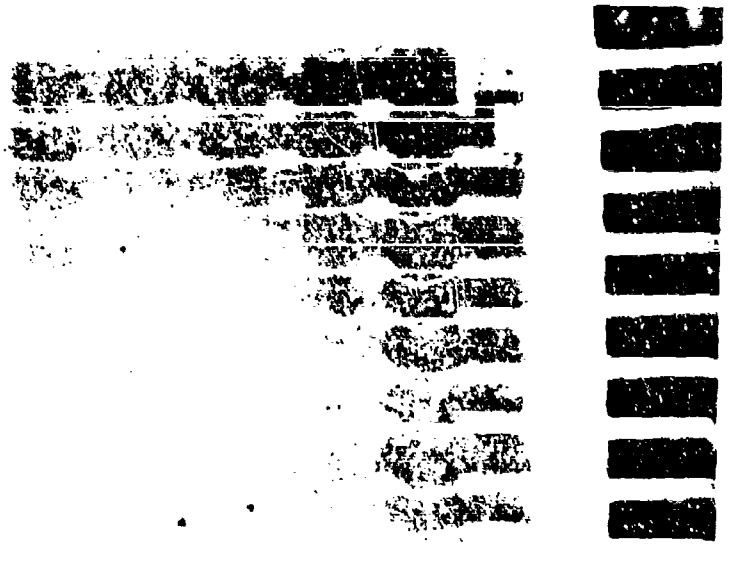


Before Centrifuge after 14,000g, Superimposed

Figure 6 (b) Superimposed X-rays

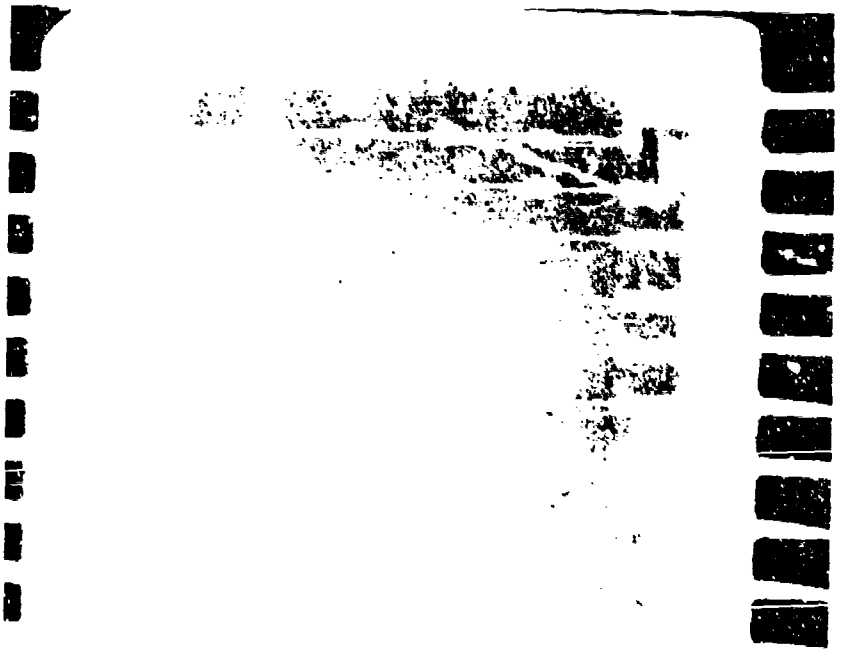


Before Centrifuge and after 16,000g, Superimposed



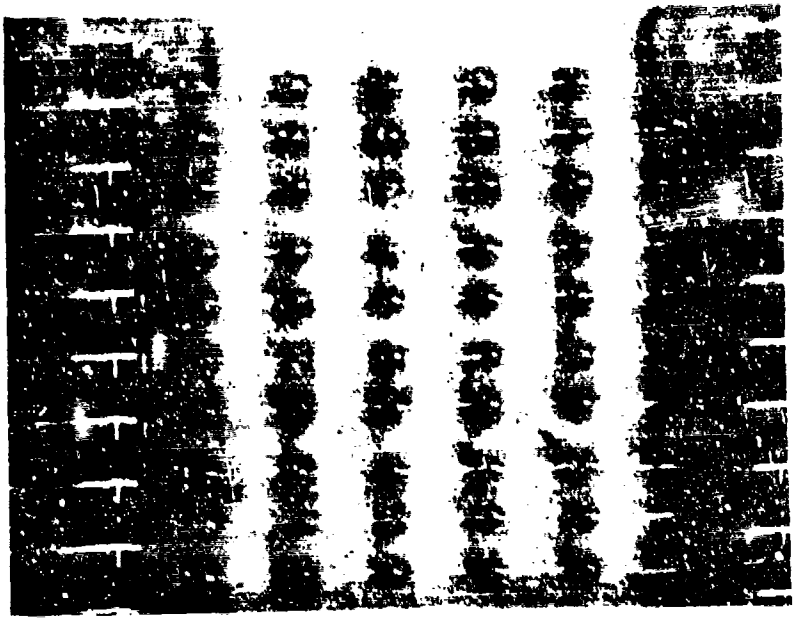
Before Centrifuge and after 20,000g, Superimposed

Figure 6 (c). Superimposed x-rays

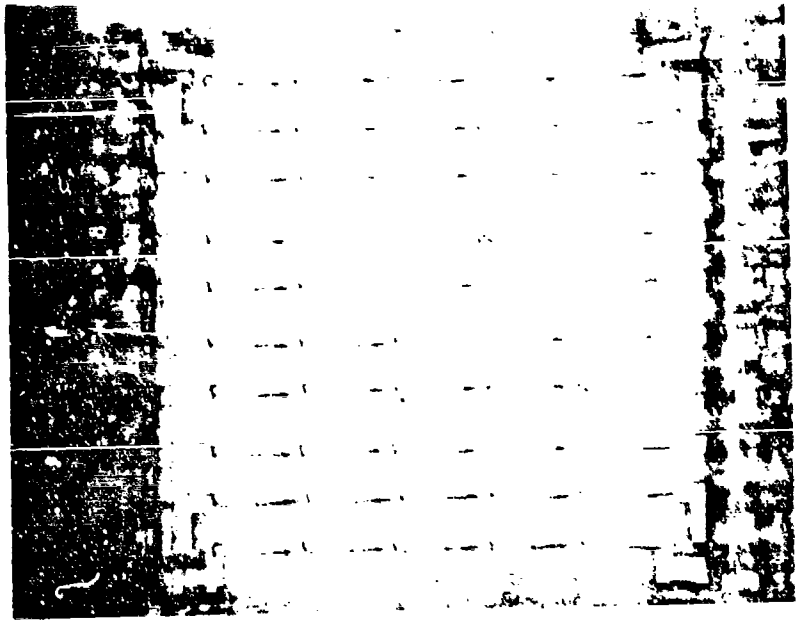


Before Centrifuge and after 25,000g, Superimposed

Figure 6 (d). Superimposed x-rays

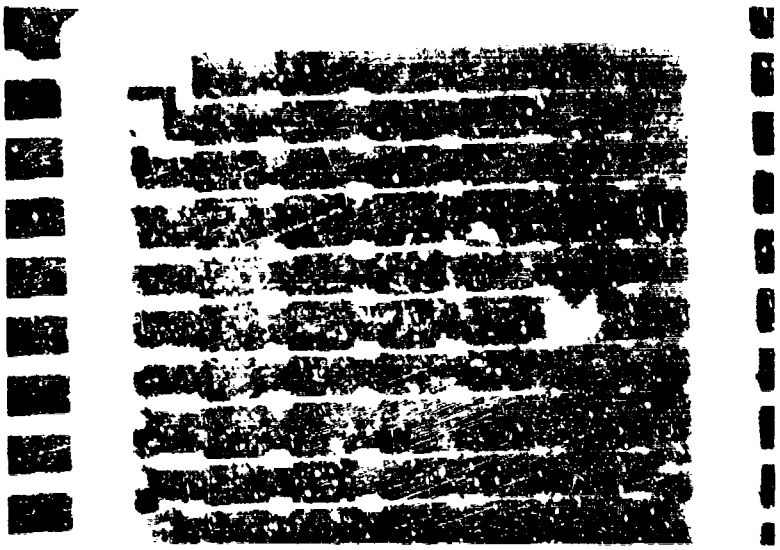


Before Lidding and Centrifuge



After 25,000g.

Figure 7 (a). Before and after Centrifuging.
Forces pushing wires down.



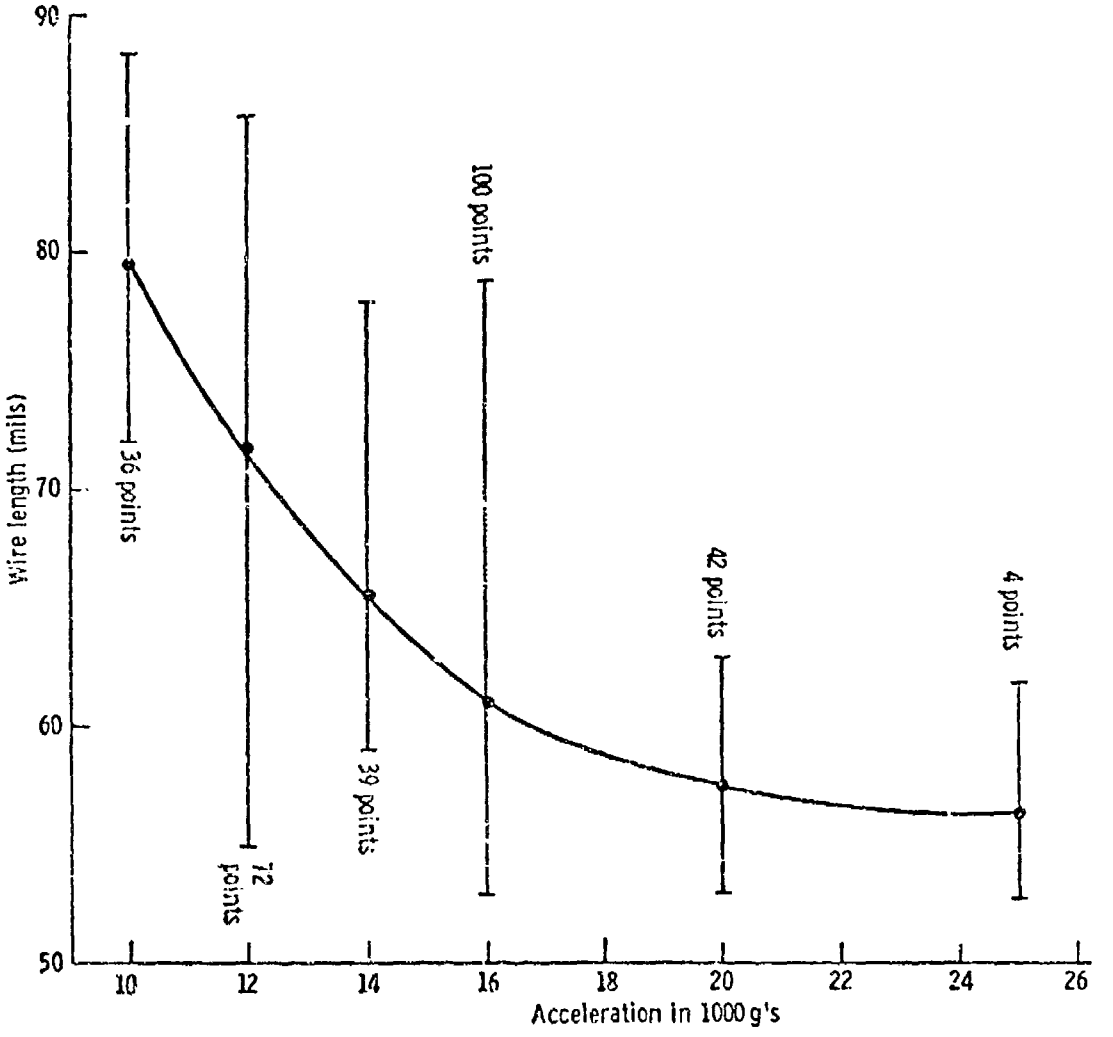
Before Centrifuge and after 20,000g, Superimposed.

Before Centrifuge and after 25,000g, Superimposed

Figure 7 (b). Superimposed x-rays

After 25,000g. Wire tends to lay down.
The substrate is touched only at the bonds.

Figure 8. Partial collapse of wire.



Wire length and bending acceleration

Figure 9

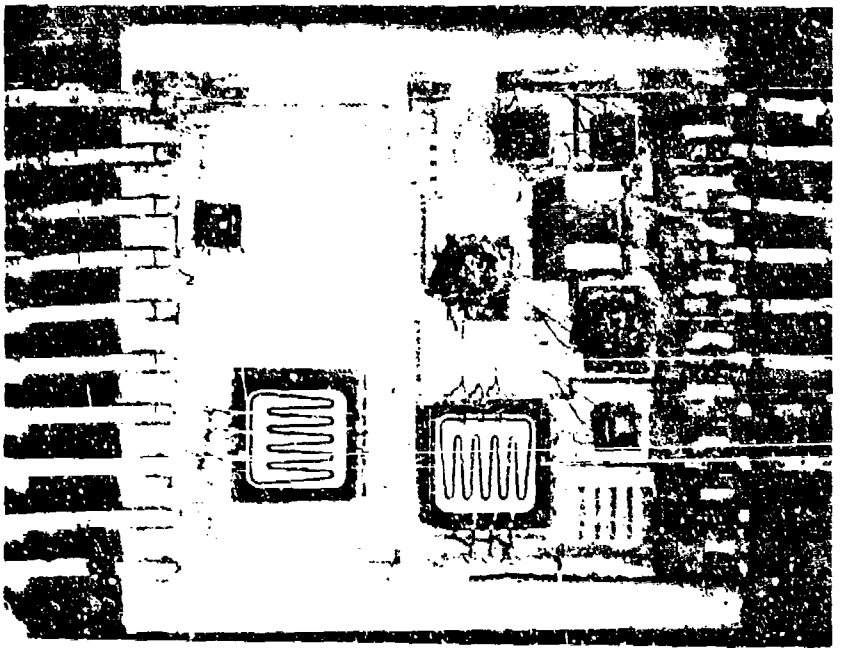


Figure 10. Random Wire Directions

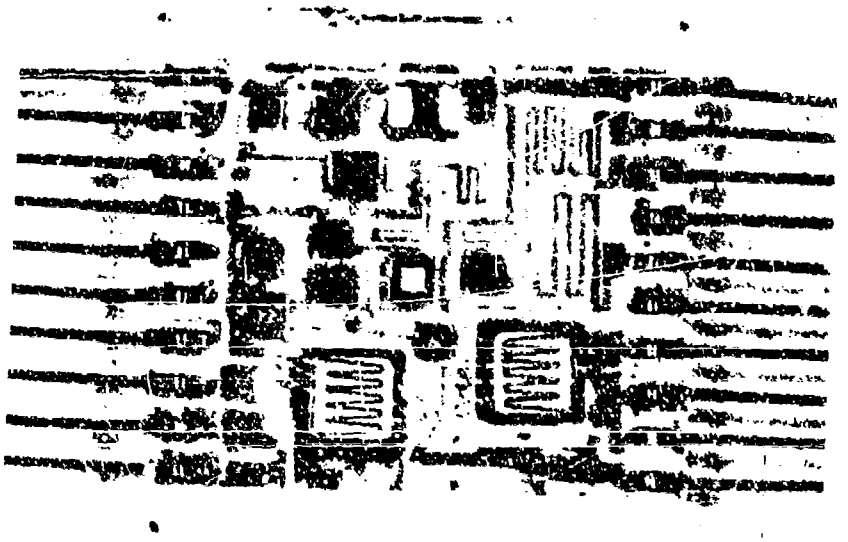


Figure 11. Controlled Wire Direction

ENGINEERING STUDY OF DEVELOPMENT OF TWO-LEVEL ANODIZED Al INTERCONNECTS FOR MSI AND LSI

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ABSTRACT

This study covers the process development for two-level anodized aluminum interconnects suitable for LSI integrated circuits, included in this study is a reliability evaluation and a comparison with conventional two-level aluminum interconnect systems.

Multilevel aluminum interconnect systems have been traditionally plagued by open metal problems, interlevel shorting problems, and interlevel contact resistance problems. These problems are all indirectly the result of conventional interconnect processing in which metal films and insulator films are deposited and then selectively removed. The development of aluminum anodization as a useful method of defining interconnect systems has opened the way for the development of a multilevel aluminum interconnect system that is free from these problems. Al anodization is a conversion process not a subtractive process in which selected areas of aluminum metal are converted to aluminum oxide insulating layers. This conversion process yields a monolithic conductor-insulator system, that is basically flat and does not suffer from the deficiencies incurred in conventional aluminum-silicon oxide multilevel interconnect systems.

The anodization process can be carried out in a series of electrolyte baths. The electrolyte used in this study consists of an oxalic acid solution in ethyl alcohol. The anodic process was carried out at room temperature with an applied dc potential of 125V. Under these conditions the rate of anodic conversion of metallic aluminum to the oxide is 4 micro inches per minute.

The anodic process sequence is outlined in Figure 1. The process sequence uses steps similar to those used in conventional multilevel interconnect systems, but the order in which the process steps are carried out is in some cases reversed. Step 1 involves the definition

of the first to second level via holes. Step 2 involves the definition of the leads, the secon' and subsequent levels of interconnects are formeo by iterations of this process. Note that the aluminum leads are imbedded in and overcoated with aluminum oxide. Also note, that the first to second level contact via holes are formed in place, not by an etching operation. The patterns are defined using conventional photolithography.

Figures 2 and 3 show areas of a two-level test pattern. Figure 2 is a test pattern in which the first level interconnect is formed by aluminum anodization. Figure 3 is the same test pattern in which the first level interconnect is formed by conventional etching techniques and the insulation layer is deposited silicon dioxide. Note in particular in the scanning electron micrographs the absence of steps at the metal crossover points on the anodized aluminum samples. Also note the interlevel contact points in the anodized aluminum test pattern shown in Figure 2 exhibits an almost planar structure both at the metal edges and at the interlevel contact points. This planarity of the anodized surface is a critical factor in eliminating the open metal problem and the interlevel shorting problem. The interlevel contact resistance problem has been significantly impacted by eliminating the etching operations normally used to open the contact window.

Preliminary data indicates an improvement in the mean time to failure for anodized aluminum leads vs. conventional aluminum leads under high current stress conditions. Other preliminary data indicates that the anodized aluminum structure offers good barrier properties to ionic contaminants that affect integrated circuits.

ACKNOWLEDGEMENT

The work described in this paper was performed under contract N00019-70-C-0487 with the monitorship of code: AIR-52022 (Mr. A. D. Cline, Mr. C. D. Caposell and Mr. A. S. Glista) of the Naval Air Systems Command.

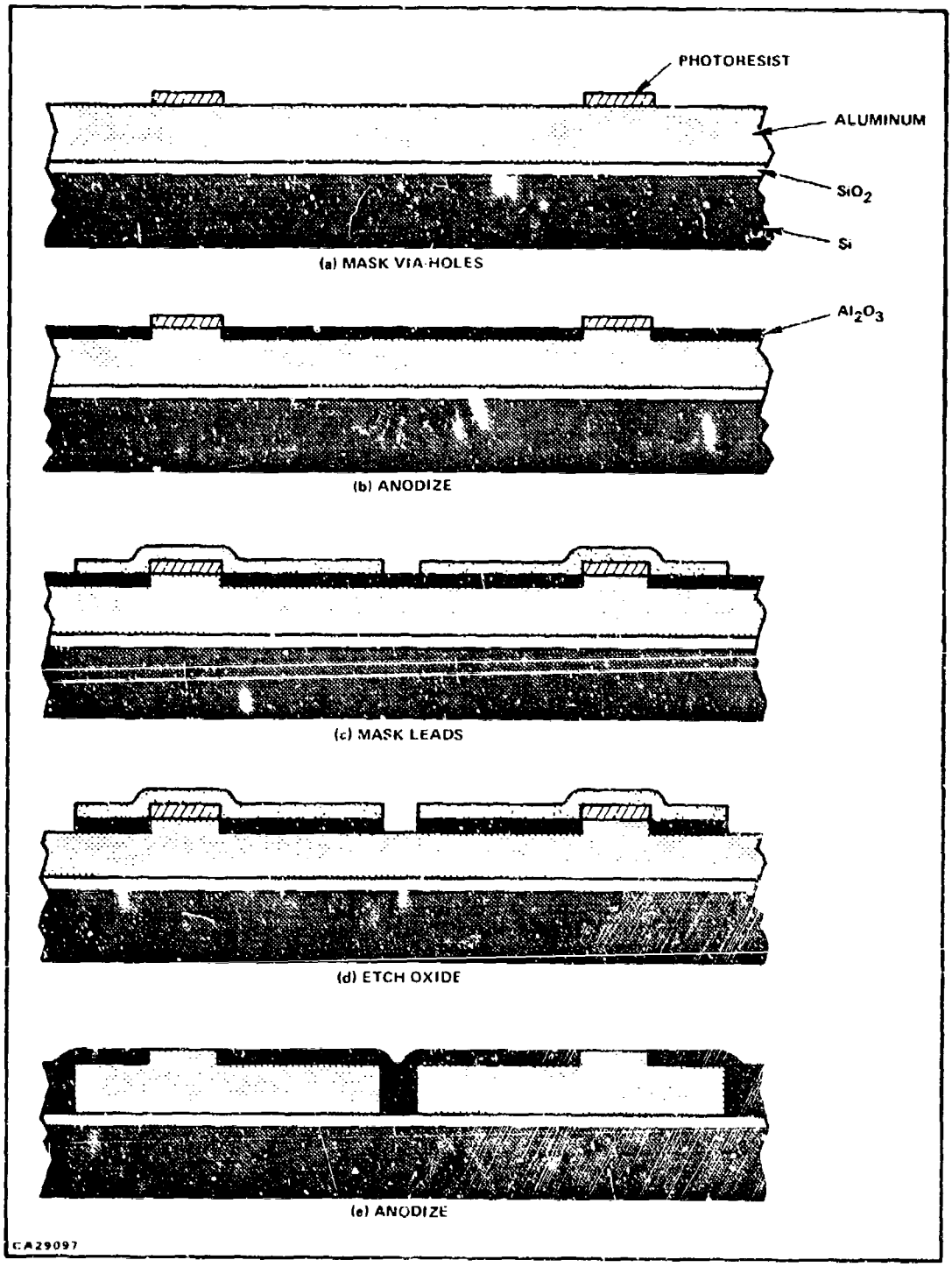

Figure 1 - Anodization Process Sequence

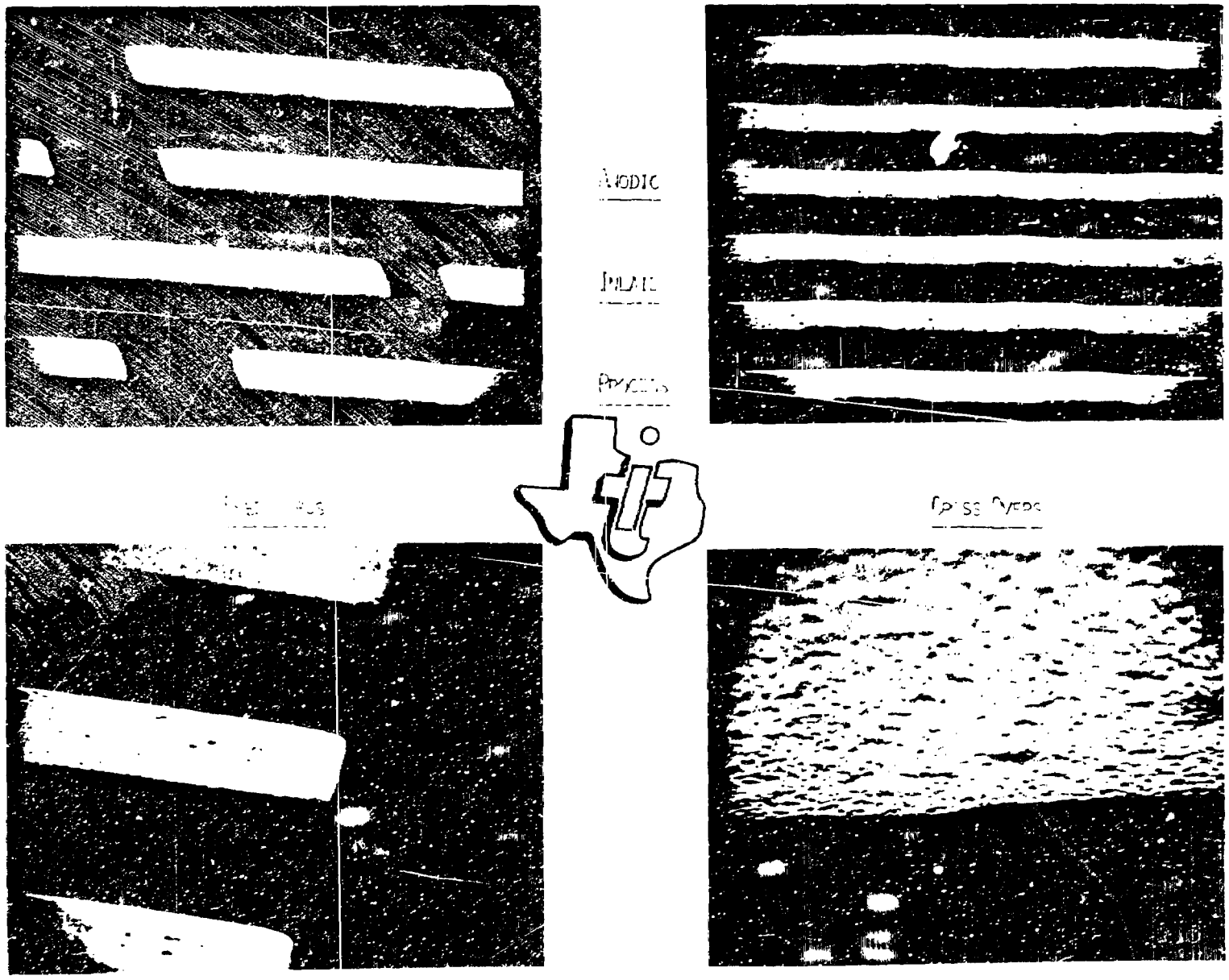

Figure 2 - Two-Level Structure-Anodic Process

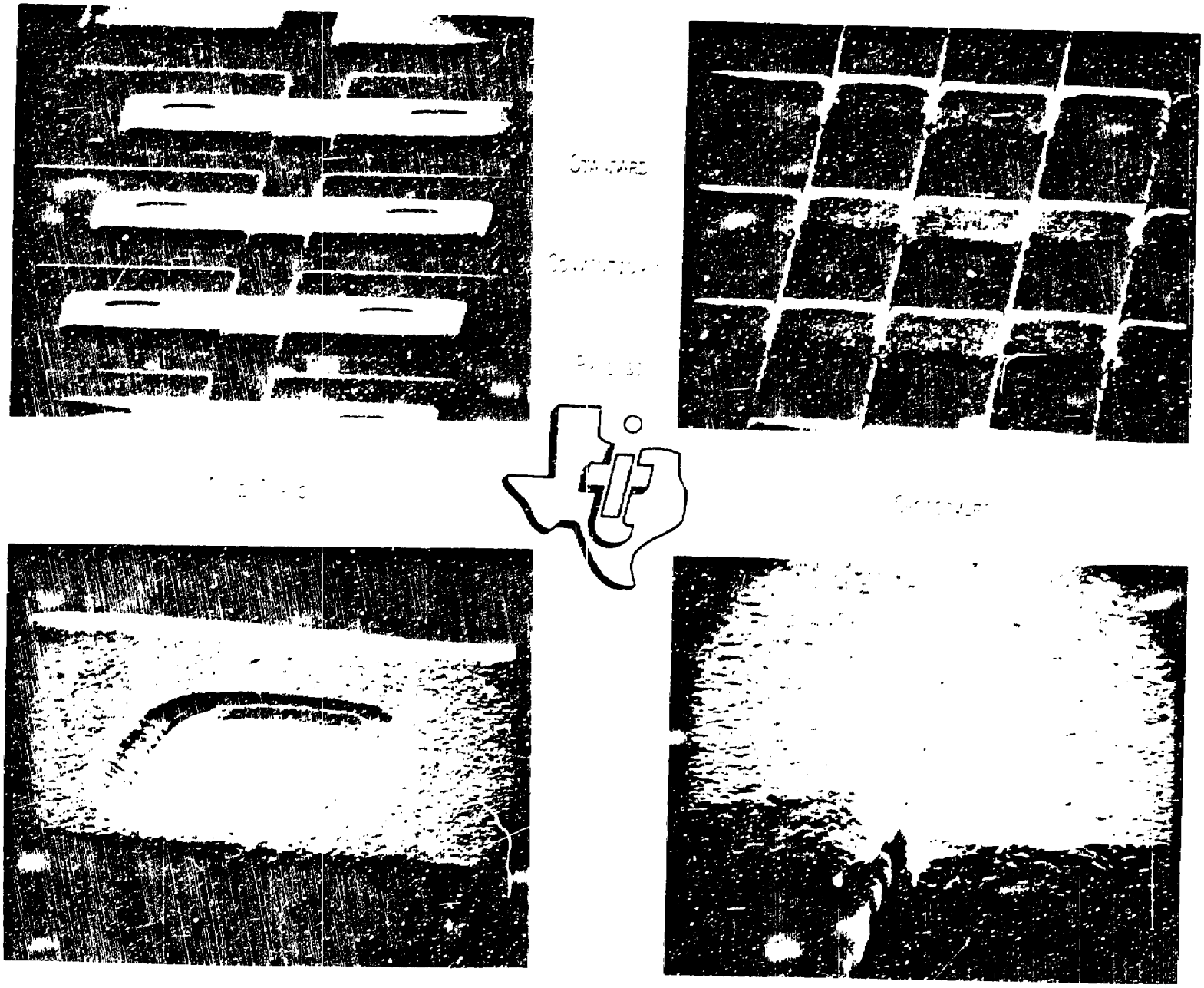

Figure 3 - Two-Level Structure-Conventional Process

TIME-SHARED CIRCUITS

William H. Licata

Naval Ordnance Laboratory

A circuit has been designed to generate the vector sum of two DC input signals using a time-shared multiplier. It has been shown that special analog modules can be used in a time-shared mode with savings in cost, size, and power consumption. Increased accuracy may also result.

INTRODUCTION

The investigation of time-sharing techniques applied to analog circuit modules was motivated from a system design standpoint. It is hoped that the development of this idea can greatly increase the flexibility of analog guidance computers and reduce total hardware cost. Although a multiplier was used in the vector summer circuit, many other analog and probably digital circuits can be used in a time-shared mode.

TIME-SHARED CIRCUIT

Analog guidance computers require many special computational circuits. One such circuit is a vector summer circuit which calculates the square root of the sum of the squares of two numbers. This function could be instrumented using three analog multipliers and two operational amplifiers. Two multipliers would be used as squaring circuits and the third would be used as a square root circuit. This circuit approach is straightforward and no design problems would be anticipated.

To perform the desired circuit function, it was decided to use only one multiplier in a time-shared mode. This means multiplexing the input signal to the multiplier and demultiplexing the multiplier output. The square root function can be accomplished using the multiplier as a squaring circuit in the feedback loop of an integrator. This means the multiplier will always be used as a squaring circuit. In other applications, it might be necessary to change the operating mode of the multiplier to perform multiplications, divisions, and obtain powers.

The main addition in circuitry to the multiplier and operational amplifiers is the timing circuits needed to sequence the multiplier through the different operations. Given some base time interval, the interval is divided into four subintervals. Each channel of the multiplier will be on during one subinterval and off for the remaining three intervals. Only three squaring operations are needed, so the fourth channel is a spare. To prevent coupling between the channels, care must be taken to ensure the timing signals do not overlap.

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To generate the four timing signals, a square wave oscillator and some digital logic is needed. The oscillator provides a base frequency and specifies the base time interval. The oscillator output drives a toggle flip-flop which acts as a frequency count down circuit. This lower frequency signal drives a second count down circuit and provides a third square wave at 1/4 the base frequency. By comparing the base frequency and subfrequencies using NOR gates, the four timing signals shown in Figure 1 are generated. The base frequency is shown as 1 kHz, and, therefore, the base time interval is 1 ms. Each channel is therefore on for 1/4 ms and off for 3/4 ms every millisecond. The schematic of the timing circuit is shown in Figure 2.

Since each channel is not on continuously, the three multiplier outputs must be stored over the 3/4 ms when the channels are off. This is accomplished using a simple hold circuit. The hold circuit consists of a capacitor connected across the input of an operation amplifier used as a follower. The amplifier is used to provide a high impedance load to the capacitor and to provide a low impedance output. The capacitor charge time should be small and the discharge time long. If the base frequency is increased the operational amplifier can be eliminated. The capacitor is then shunted by the input impedance of a summer circuit. The discharge time may be long compared to the base time interval. There are trade-offs which can be made and other problems are encountered if the base frequency is made too high.

The main circuit is shown in Figure 3 and requires a ±15V power supply. The timing circuit in Figure 2 also operates off ±15V and, therefore, contains a +5V regulator to supply the logic voltage. A modified version of the timing circuit uses COS/MOS logic which can operate off +15V. The power consumption of the COS/MOS logic is also much less than the transistor logic. The multiplexing is accomplished using FET's as analog switches. To pass ±10V signals, the gate voltage of the FET's must switch between ±15V. The logic voltage is too small to drive the FET's directly and, therefore, operational amplifiers must be added to the timing circuit to boost the logic voltage. In a practical circuit the operational amplifiers would be replaced by a simple transistor or FET amplifier. In practice, one timing circuit may drive many time-shared circuits. This is why the total circuit is divided into two parts.

Table 1 shows some typical test data. When both inputs are zero a fairly large bias is present. This is to be expected since the square root of a small number is larger than the number itself. With a bias of .01V, a .1V offset can be anticipated at the output. The accuracy of the data is better than anticipated. One possible reason for this is that the same multiplier is used to calculate the square and square root. The effect of inaccuracies is opposite when taking squares and square roots. There may be some cancellation of errors.

One possible way to improve circuit accuracy is to use the spare channel to cancel the multiplier offset. The input to the spare channel is grounded and the output is stored. This output voltage will be the multiplier offset. It can be subtracted from the other three

outputs. Doing this continuously, the circuit tracks variations in the multiplier offset. At present, this is not done. Other errors predominate and the effect of the multiplier offset is masked out by these other errors.

At the moment, the primary problem area in improving the circuit performance is cross coupling between the channels. The multiplier used has a 100 kHz bandwidth, but the sampled output signal is distorted slightly. The output of the multiplier is a staircase type of function. The corners of the output function are rounded off due to high frequency attenuation, but of more importance is the phase shift introduced. The output of the multiplier is shifted slightly in phase from the input. This means the output is slightly out of phase with the timing signals causing cross coupling between the channels. To overcome this, the timing signals to the FET's at the multiplier output should be shifted an equal amount in phase. This means adding a low pass filter which matches the frequency characteristics of the multiplier. Besides cross coupling of the channels no other real problems were encountered. Variations in base frequency are not important. An unsymetric square wave signal out of the oscillator causes short periods of time when no channel is on. This causes ±15V spikes in and out of the multiplier. Adding a capacitor across the input of the amplifier driving the multiplier eliminates this problem.

In conclusion, it is felt that it has been demonstrated that special analog modules can be used in a time-shared mode. The breadboard unit described in this paper is shown in Figure 3. A small reduction in cost of about $20 was realized. Larger reductions in costs appear when many time-shared circuits appear in a system. The cost of the timing circuit is distributed over many circuits. A size reduction is achieved due to the large size of the multiplier in comparison to the digital logic and operational amplifiers. Also a small savings in current drain was realized. Although the study of time-sharing analog modules was motivated from a systems standpoint, it does appear to hold out some promise for improved circuit accuracy and much more flexibility in designing complex computational modules.

Table 1

ACCURACY DATA

X Volts	Y Volts	$(X^2 + Y^2)^{1/2}$ Volts	True Value Volts
0	0	.01	0
0	1	.99	1.
0	2	1.99	2.
0	3	2.99	3.
0	-1	.98	1.
0	-2	1.99	2.
0	-3	3.00	3.
1.	1.	1.41	1.41
2.	2.	2.83	2.83
3.	3.	4.24	4.24
4.	4.	5.64	5.66
5.	5.	7.05	7.07

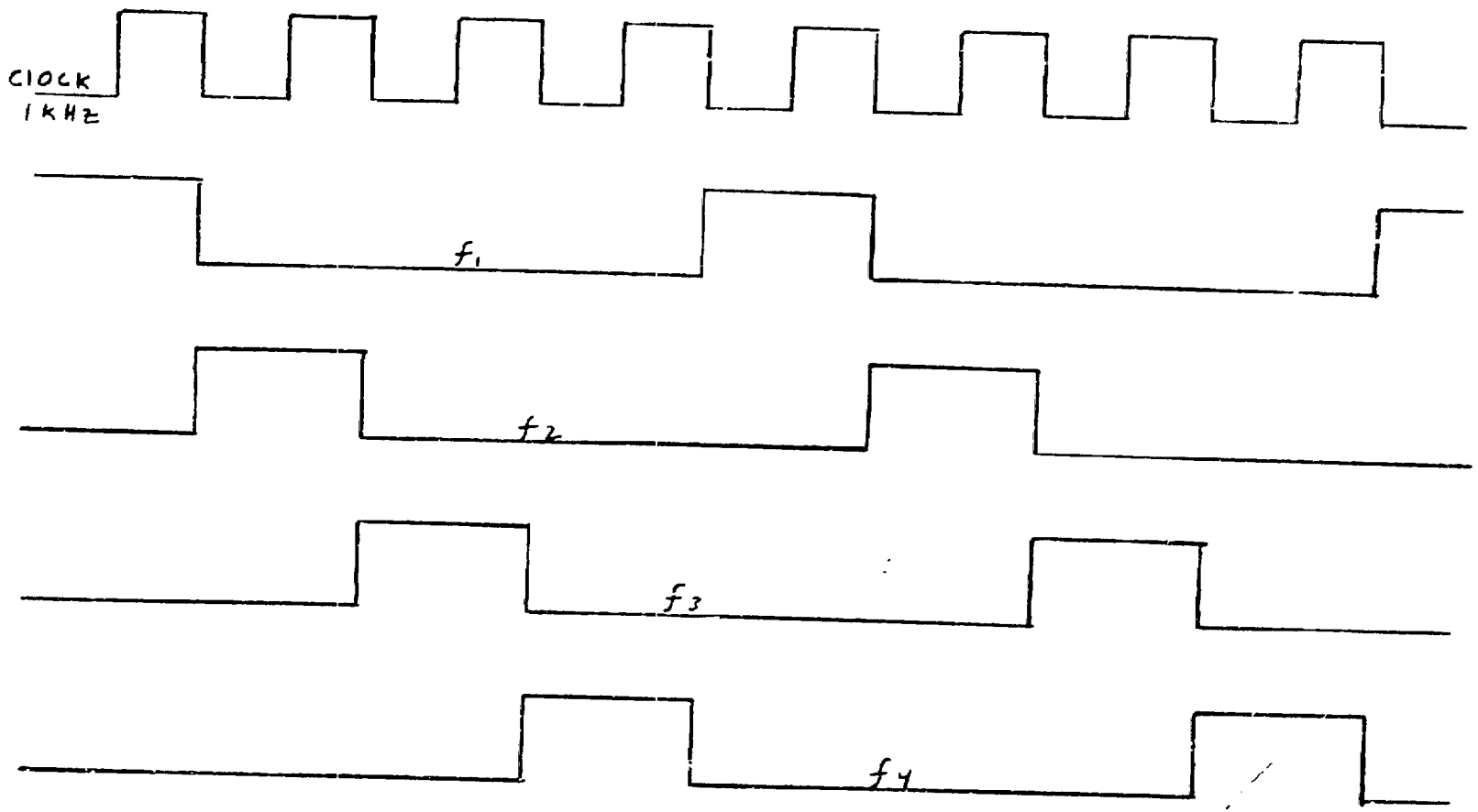

Figure 1 Timing Signals

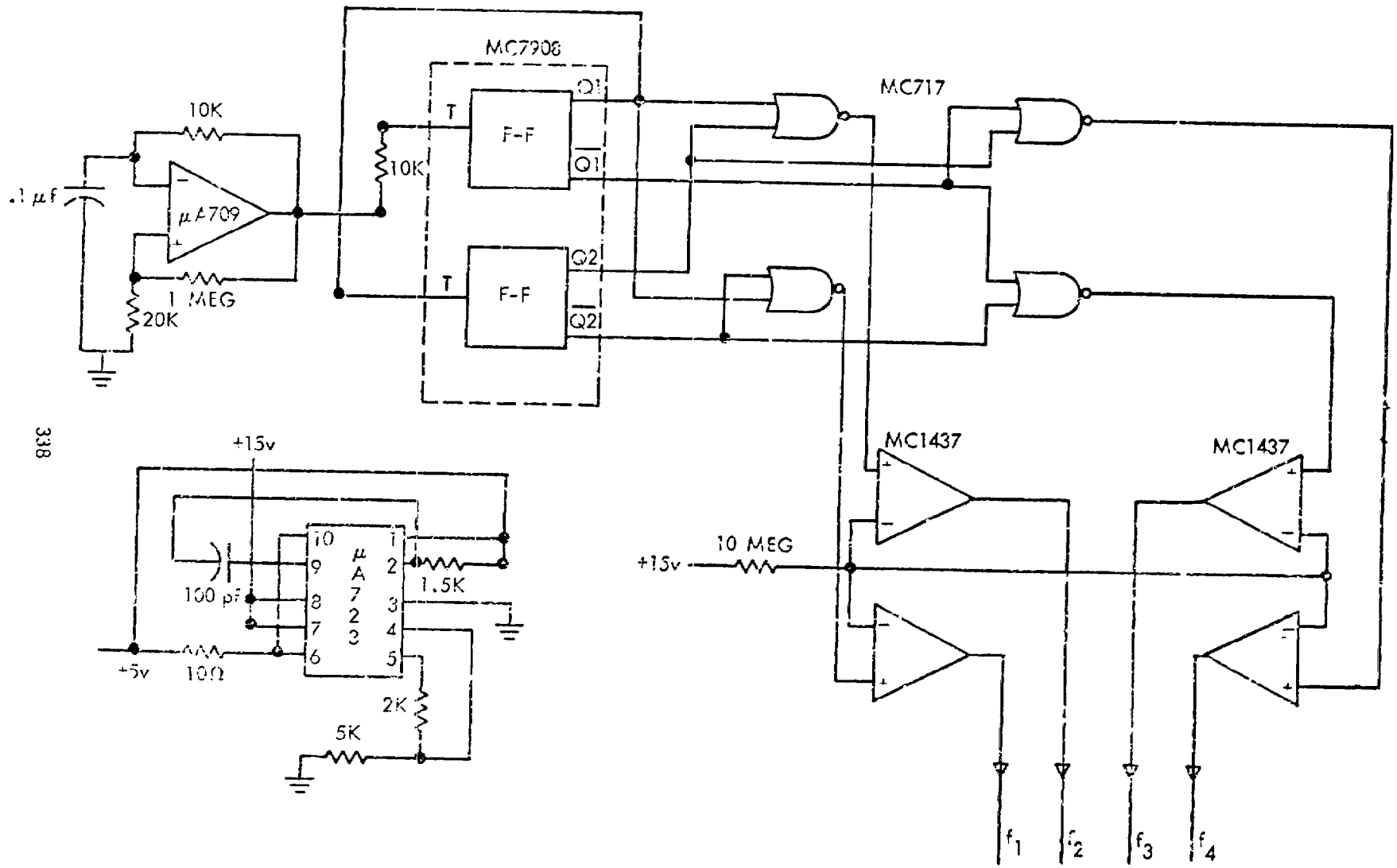

Figure 2 Timing Circuit

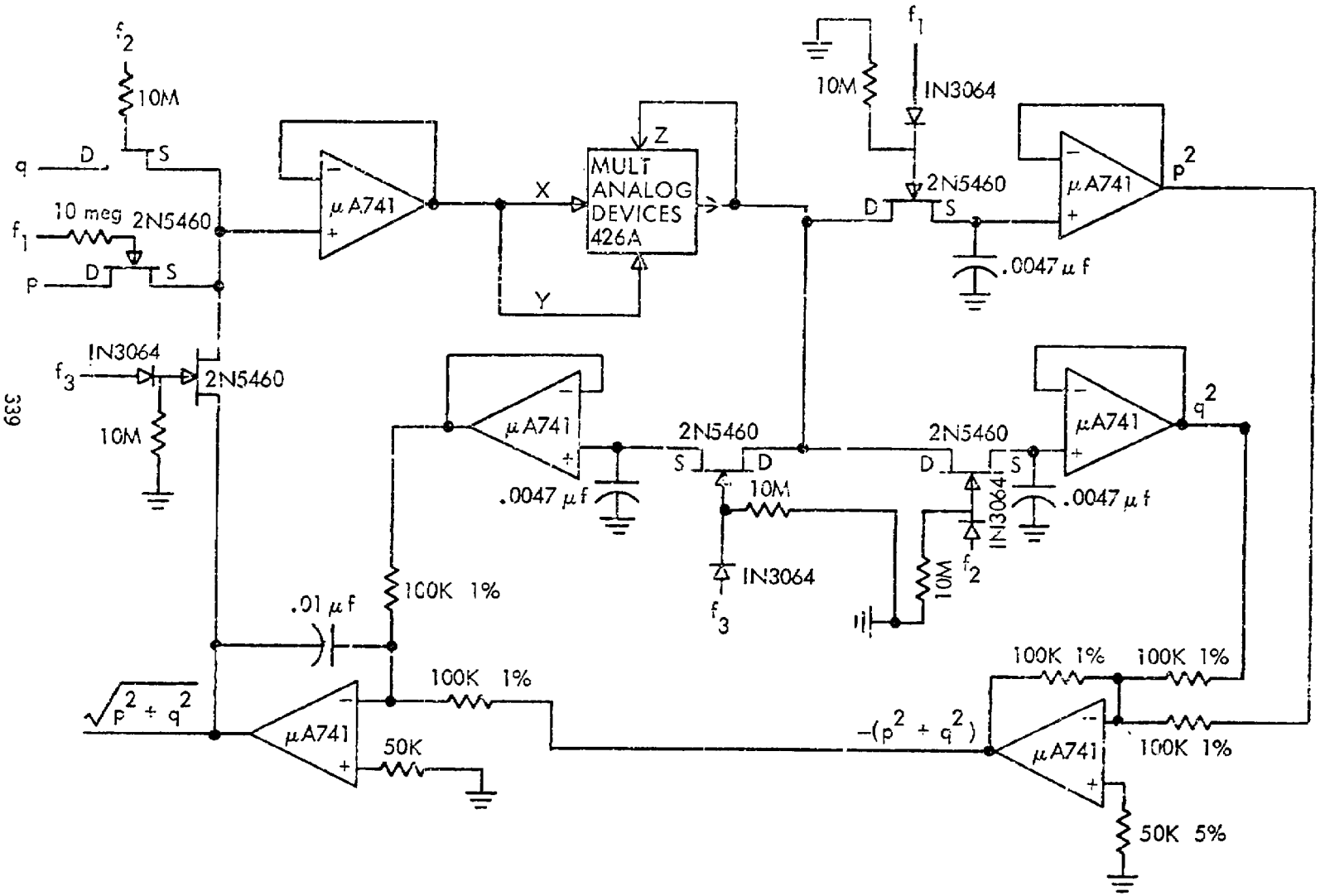

Figure 3 Vector Summer Circuit

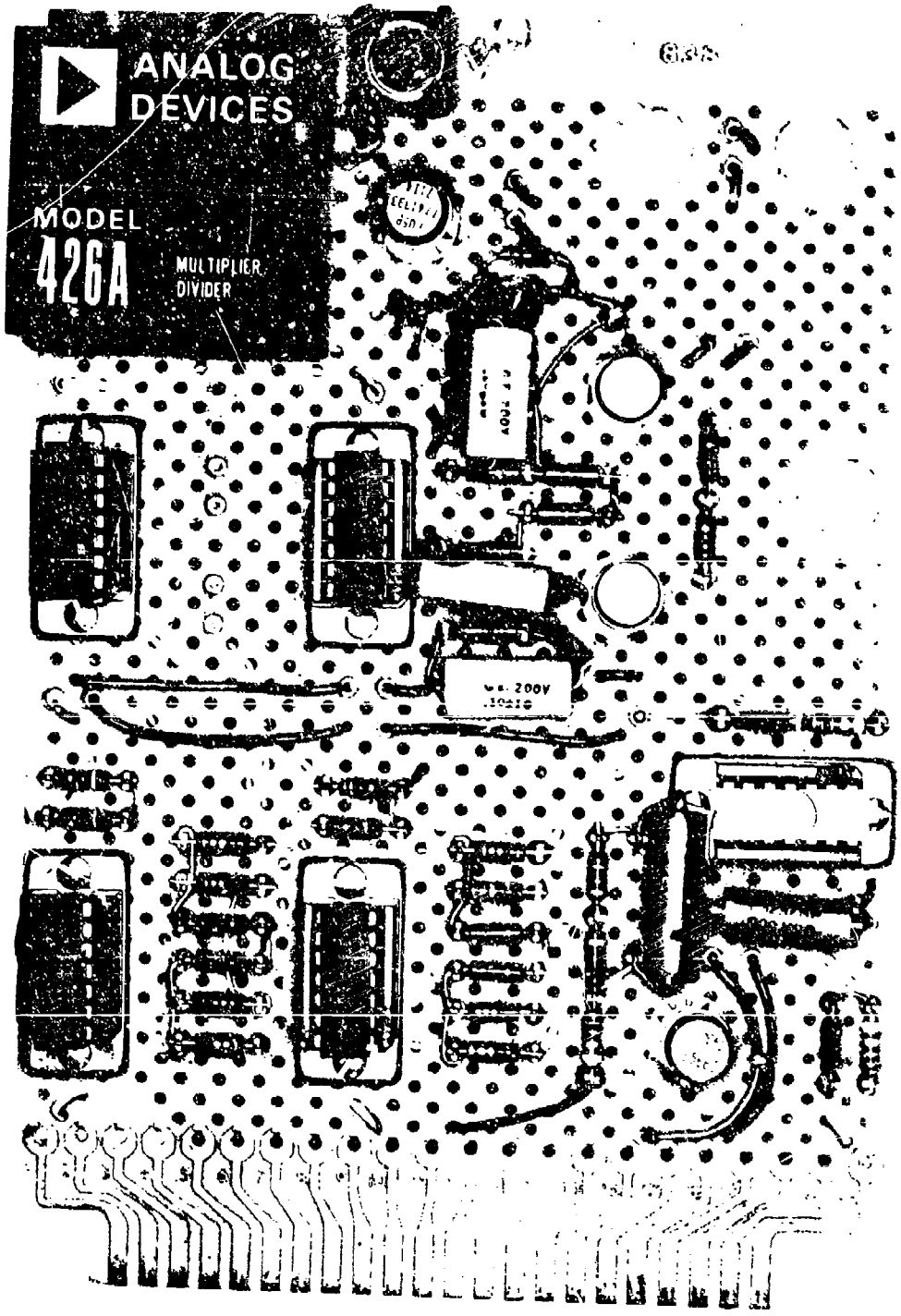

Figure 4 Breadboard Circuit

DEVICE IMPLICATIONS OF ION IMPLANTATION DAMAGE IN SILICON

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Abstract - Thermal stimulated current and diode recovery measurements are presented for ion implanted silicon. The results are used to evaluate device possibilities such as bipolar transistors and hyper-abrupt diodes where control of implantation damage is critical.

Ion implantation offers a doping method that promises to extend the current state of the art of both discrete devices and integrated circuits. The advantages of the precise control attainable over the total dopant dose introduced together with the extreme uniformity in both depth of penetration as well as laterally over an entire wafer surface are immediately apparent. The greatest concern over the applicability of the process centers on the radiation damage that is introduced and how well it can be annealed.

In some applications such as with the self aligned gate of MOS transistors, the implanted region does not form the active part of the device and any residual damage after annealing should not affect the device too adversely. This is not so, however, once the implanted layer becomes the critical part of a device such as with the base of a bipolar transistor or is incorporated to give a p-n junction hyper-abrupt properties. It is well known, for example, that deep levels such as the gold centers affect the capacitance of p-n structures.[1] Consequently, implanted layers have been examined for deep defect levels and the minority carrier lifetimes have been monitored as a function of annealing temperature.

For both the defect level and lifetime determinations, phosphorus diffused junctions are used that are then implanted at sufficiently high energies for the ions to penetrate to the region immediately beyond the junction. In this respect the structures resemble actual devices where the implanted layer corresponds to the bipolar base region or to the region that gives the junction its hyper-abrupt properties.

As it is the damage rather than the doping that is under examination, non-dopant ions have been used. At the high energies of ~ 1 MeV that are used, the initial energy loss of the ions will be electronic in

nature and only towards the end of their paths after being considerably slowed down do nuclear collisions and hence lattice damage become appreciable. In this manner, most of the damage will be confined to the region immediately below the junction and which is the region probed by the measurement techniques used.

It should also be noted that even though the energies used here are appreciably greater than those normally used for device work, the degree of damage obtained will not be considerably higher. As the implant energy is increased, the fraction of the total energy dissipated in damaging nuclear collisions progressively decreases. Thus, on increasing the implantation energy of carbon ions from 300 KeV to 1 MeV, the energy dissipated in nuclear collisions only increases from 41 to 54 KeV.[2]

Thermal stimulated currents (T.S.C.) have been used for the defect investigation.[3] The implanted sample is cooled to 78°K and light applied to fill the various defects with carriers. These carriers are released on heating the sample (usually at a uniform rate of ~ 1°C sec^{-1}) and give rise to current (T.S.C.) peaks that are superimposed on the diode leakage current. The charge released, and hence the size of the peak, is a measure of defect concentration while the temperature at which a TSC peak occurs is related to the depth of the defect level within the bandgap. It will be seen that several defects with overlapping peaks will be observable and on annealing small variations in the TSC peak temperature occur. This variation, which should not arise if the defect energy remains constant, is attributed to the influence of other partially overlapping peaks and whose rate of growth or annealing differ.

Figure 1 shows the TSC's obtained from sulfur damaged diodes. They were recorded prior to and after annealing to the temperatures indicated in the figure. Being of nearly similar mass to phosphorus, the sulfur damage should be indicative of phosphorus damage and the dose required for hyper-abrupt applications will be close to the 1.5×10^{14} ions cm^{-2} used here. The TSC peaks shown represent levels ranging from .25 eV to .38 eV deep. The large current seen at the higher temperatures is the rise in the dark current of the diode as it is heated towards room temperature.

Other implanted ions give rise to similar levels. The most notable difference has been seen with the lighter carbon and oxygen ions.[4] Then, an additional level grows in at ~ .4 eV while the intermediate peak obtained ~ 140°K does not show the appreciable growth that is seen here for sulfur.

From the device viewpoint, what is important is whether these defects can be annealed out. As can be seen, annealing up to ~ 250°C serves to form additional rather than anneal out the initial concentration. They are still present to greater than the pre-anneal concentrations at 400°C (not shown) but are largely annealed by 510°C. Non-electrical measurements such as Rutherford backscattering indicate that low dose damage anneals between 200 and 400°C[2] while the present result clearly indicates that device quality layers are not obtained unless annealed to at least 500°C.

For the carrier lifetime, the reverse recovery pulsed technique is used. Usually, the lifetime can be considered as being fairly uniform over the low doped side of a diode. Obviously, this is not so here and most of the effect of the ion damage will be confined to a micron or so wide layer immediately below the junction. Even within this region the lifetime can be expected to be non-uniform and exhibit some form of Gaussian distribution. Despite these difficulties, the indicated lifetime from the measurement will accurately pinpoint the annealing required to restore the lifetime to its pre-irradiated value.

Annealing of the minority carrier lifetime is shown in Fig. 2. The example given is for carbon (similar mass to boron) and implanted to a dose that approaches that required for a bipolar base. As can be seen, the lifetime recovers to values greater than 1 μs and matches that in similar but unirradiated diodes by 600-650°C. Thus, the damage does not inhibit the lifetime from recovering to values that are adequate for base transportation.

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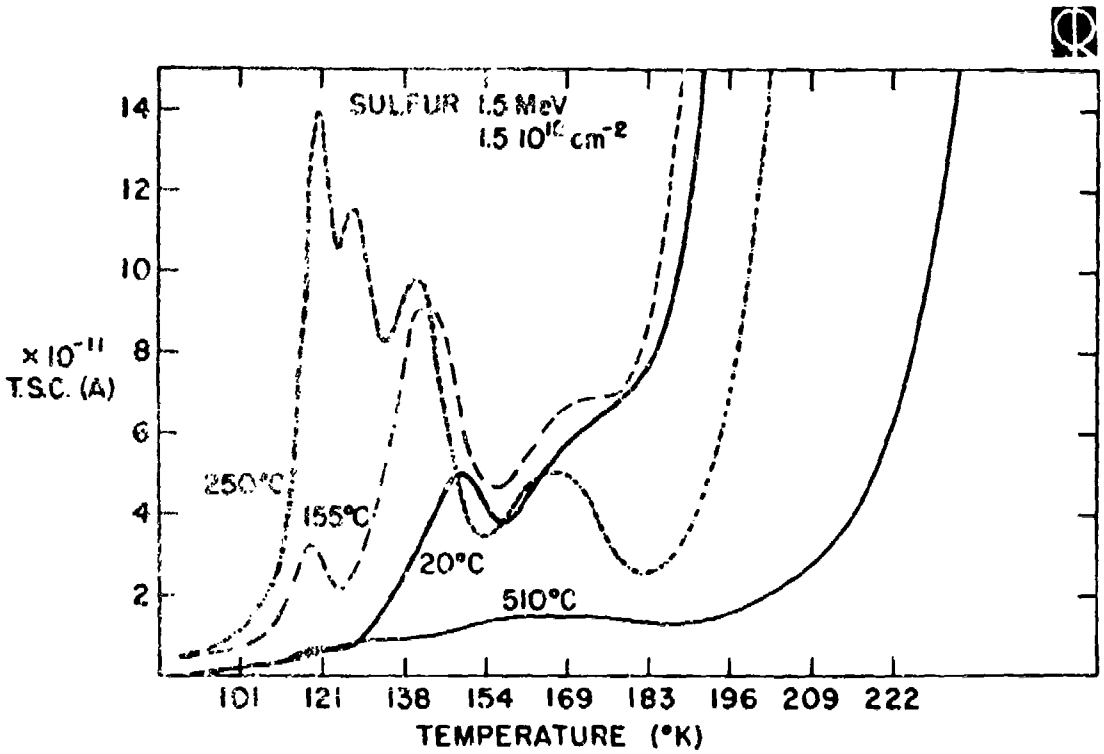
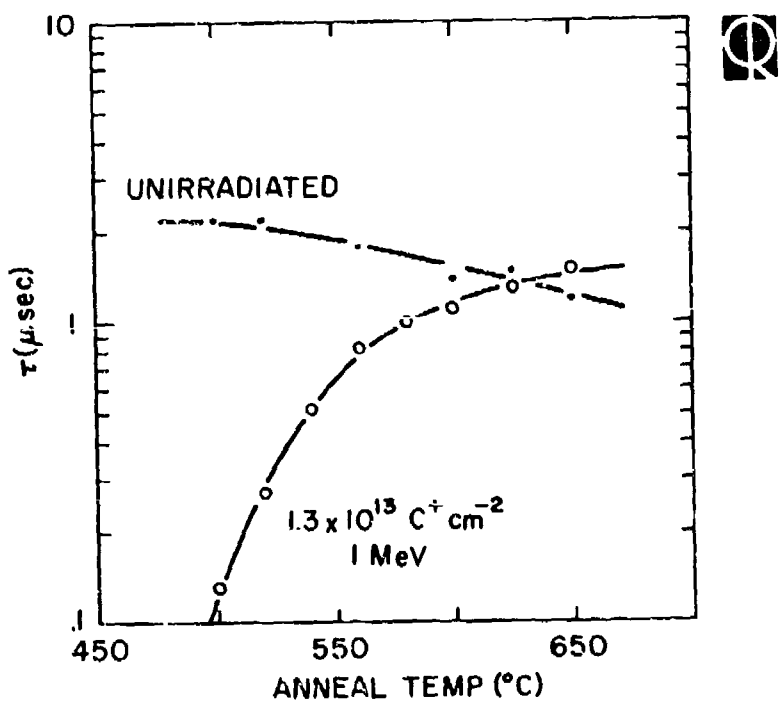

SULFUR 1.5 MeV
1.5 10^12 cm^-2
14
12
10
8
6
4
2
x 10^-11
T.S.C. (A)
250°C
155°C
20°C
510°C
101
121
138
154
169
183
196
209
222
TEMPERATURE (°K)


10
1
.1
τ(μ sec)
UNIRRADIATED
1.3 x 10^13 C+ cm^-2
1 MeV
450
550
650
ANNEAL TEMP (°C)

A VARACTOR-TUNED RF AMPLIFIER INTEGRATED CIRCUIT FABRICATED USING ION-IMPLANTED DEVICES

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ABSTRACT

Ion implantation has been used in the fabrication of components for a varactor tuned RF amplifier integrated circuit having a gain of over 20 dB and tunable from 50 to 76 MHz. The amplifier was designed to establish production capability for this type of circuit, and consists of varactor, resistor and dual-gate MOSFET devices on a 48 by 60 mil chip.

An RF amplifier integrated circuit has been designed for a production engineering measure in progress, the objective of which is establishment of production capability for ion implanted circuits. The amplifier circuit consists of a dual-gate MOSFET transistor, a voltage variable tuning capacitor (varactor) and resistors. The circuit schematic is shown in Fig. 1.

The circuit was designed to be suitable for the front-end of a receiver for the 50-76 MHz band. The input circuit is electrically tuned by the varactor. The dual-gate MOSFET provides power gain and the resistors are for biasing the MOSFET and the varactor.

The incorporation of a high quality varactor on the same chip as the MOSFET and resistors makes this circuit unique. The specific requirements for the varactor in the IC were

$$Q > 70 \text{ at } -2.5 \text{ volts, } 50 \text{ MHz,}$$

$$C_R = \frac{C(2 \text{ volts})}{C(12 \text{ volts})} \simeq 3.5 - 4.0.$$

$$I_{rev} = \lesssim 100 \text{ nA at } -12 \text{ volts, } 25°C.$$

Ion implant doping was used in fabricating the varactor, which made possible a hyper-abrupt junction and a high Q device.

Ion implantation was also used to fabricate all the resistors. This made possible small, high value resistors, which were desirable to minimize loading of the input tuned circuit. The use of ion implant for MOSFET threshold voltage adjustment was also investigated as part of this work. Both enhancement and depletion type MOSFET's were studied in the RF amplifier IC.

A picture of the IC chip, which measures 48 x 60 mils, is shown in Fig. 2.

The IC was made with an n^+ substrate on which a 4 μM thick, 4 Ω-cm n-type epitaxial layer was grown. The varactor was fabricated as a p^+-n hyper-abrupt junction diode. Ion implanted phosphorus was used as a low concentration pre-deposit to dope the n-epitaxial varactor region. The phosphorus was then driven in so as to provide a concentration gradient, with the donor concentration varying from about 10^{17} cm^{-3} at the surface to 10^{15} cm^{-3} at a depth of 2 μM. The p^+-region was formed by ion implanting a high dose of boron ions, followed by a high temperature anneal step. The resulting p^+-n junction was located approximately 0.4 μM from the silicon surface. Varactor series resistance was kept small through the use of the low resistivity n^+-substrate material.

A capacitance-voltage curve for the varactor diode in the IC is shown in Fig. 3. For these devices, the capacitance

ratio $C_R \simeq 3.5$.

A dual-gate MOSFET transistor is an ideal device for an RF amplifier, because of its high gain, low noise and small cross modulation. The MOSFET chosen for this circuit was a p-channel diffused device having a channel width-to-length ratio $\simeq 500$. A fairly conventional aluminum gate, SiO_2 dielectric structure was used. The transconductance for these devices was about 7000 μmhos.

Threshold voltage adjustment through the use of ion implant channel doping [1] was used to evaluate the merits of lower gate 1 and 2 bias voltages. A p-channel device having a threshold voltage $V_T \simeq 3.5$ V required $V_{G2S} = -10$ V and $V_{G1S} \simeq -7$ V in order to bias it in a high transconductance region. If the threshold voltage were lowered to about $V_T \simeq 1.5$ V (by ion implant, for example), the bias voltages were $V_{G2S} \simeq -7$ V, $V_{G1S} \simeq -4$ V. Depletion-mode devices were also made by channel doping with a low dose of boron ions. MOSFET's were made which operated in a high transconductance region with $V_{G2S} = -4$ V, $V_{G1S} = 0$ V.

The admittance "y" parameters were measured for discrete p-channel dual-gate MOSFET's as fabricated on the IC. From this, the maximum available gain MAG was calculated and found to be about 33 dB at 50 MHz and 27 dB at 76 MHz.

Resistors in the IC were p-type, boron ion implanted. A sheet resistivity of 2.5 kΩ per square was chosen for the resistors, based on considerations of TCR, junction capacitance and junction breakdown voltage.

The RF amplifier IC's were packaged in 12 lead TO-5 type cases and their performance was evaluated. A single 12-volt supply was used for biasing and input circuit tuning. The measured power gain was greater than 20 dB at 76 MHz, for an input power of -40 dBm. The total power dissipation of the IC chip was less than 200 mW. The measured noise figure at 70 MHz was approximately 3 dB at a gain of 20 dB.

References

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Acknowledgement

This work was sponsored by the U. S. Army Electronics Command, Philadelphia, Pa., under Contract No. DAAB05-71-C-2877.

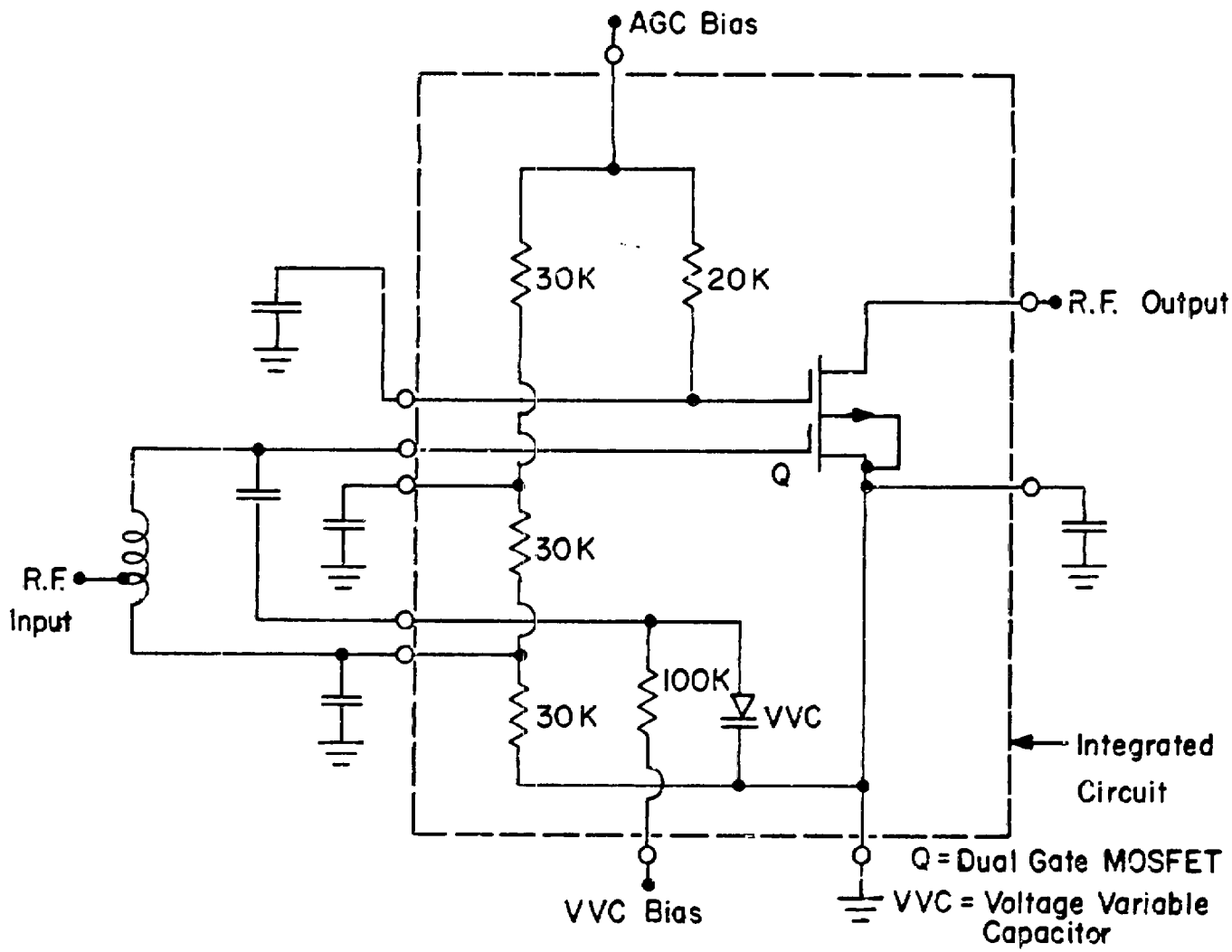

Figure 1. Varactor-Tuned RF Amplifier Integrated Circuit.

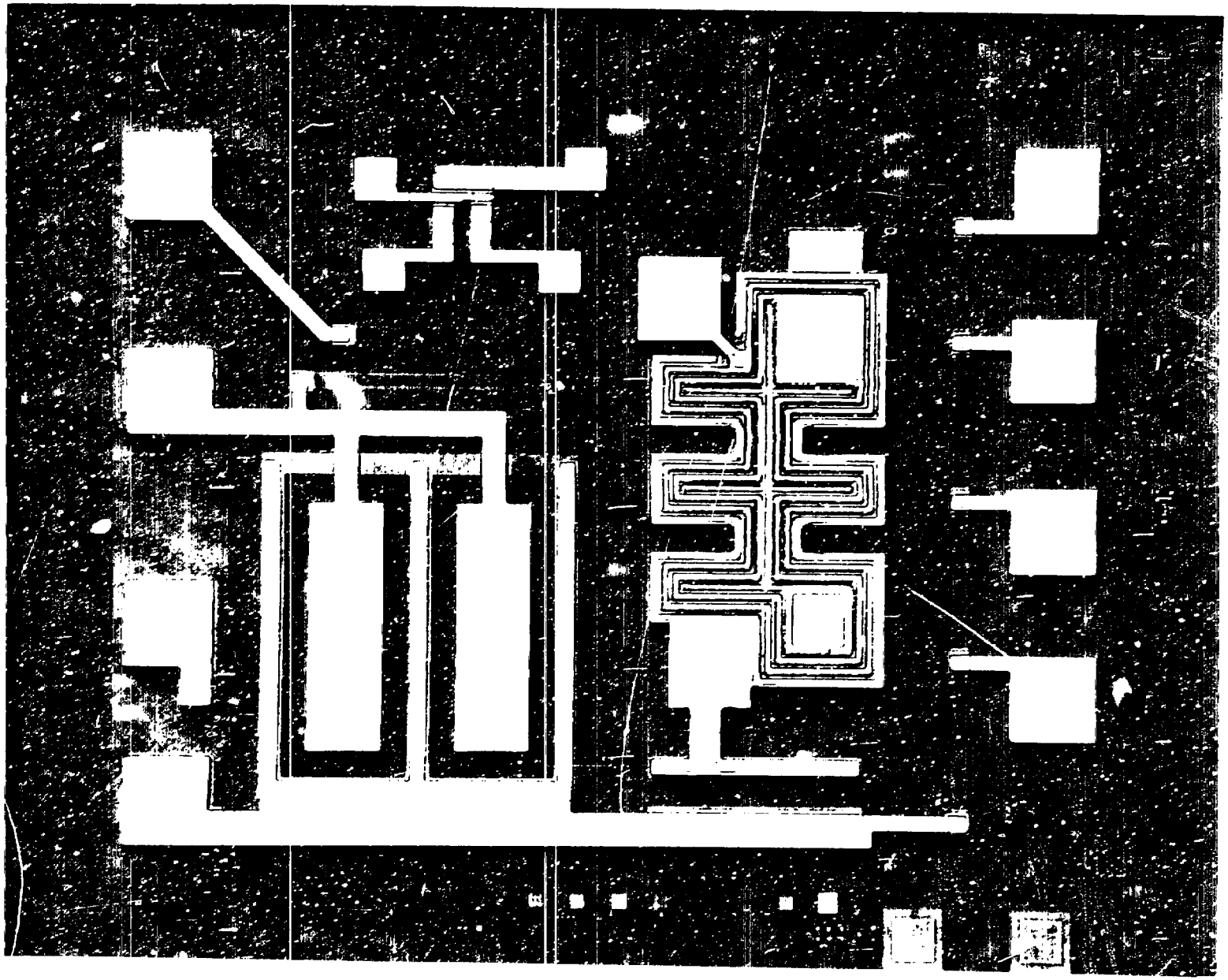

Figure 2. Hanson et al., LPF Amplifier I.C. Chip

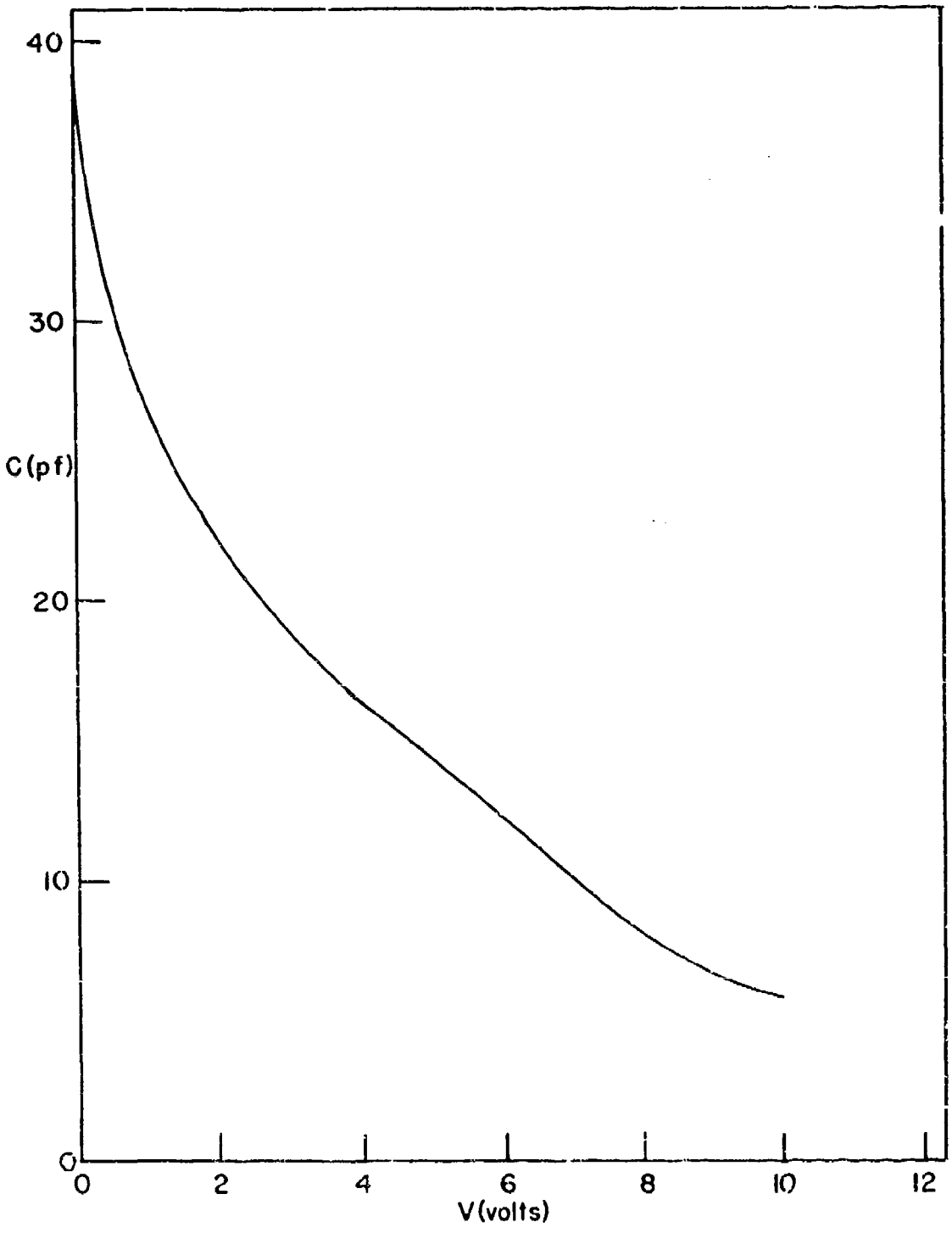

Figure 3. Varactor Capacitor-Voltage Characteristic.

COS/MOS FUZE TIMER COMBINES SCR AND ANALOG VOLTAGE DETECTOR ON SINGLE IC*

by

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ABSTRACT

An integrated circuit for the XM56 mine system combines complementary MOS and bipolar technology to provide analog and digital timing functions with a monolithic SCR output device.

SYSTEM REQUIREMENTS

The system requirements for the XM56 electronics are:

a) Interface with and detect time delays generated by two E-cell timing devices. One delay shall provide circuit arming and charging of a firing capacitor. The other E-cell delay shall provide for self-destruct at the mission completed time.

b) Discriminate over-run time duration and provide output upon over-run or 17 T_1, whichever is less, for over-run greater than T_1. A secondary input (anti-disturbance) providing a 17 T_1 time delay until detonation, regardless of duration, shall also be provided.

c) Include output capability of 5000 ERGS for T20E1 detonator from 120 microfarad capacitor at 5 volts.

* This work was supported by the Department of the Army, Picatinny Arsenal

d) Include low-supply voltage detector for self-destruct if battery voltage is less than 5.6 volts after arming.

e) Operate from 6.75-volt 5-milliampere-hr. battery for mission duration.

ANALOG DETECTOR CIRCUITS

E-cells, electrochemical devices used for timing applications, provide a changing electrical characteristic after prescribed charge transfer occurs. These devices consist of a cathode and an anode immersed in an electrolytic solution. During plating, the device has a low impedance and a voltage drop of 30 millivolts. After plating has ceased, the device impedance increases and 800 millivolts is the typical device voltage.

E-cell voltage changes are difficult to detect usin MOS transistors because the final voltage is less than the typical MOS threshold voltage. The circuit described below utilizes the substrate effect in a unique push-pull arrangement to detect the E-cell voltage change and translate this change into levels compatible with the MOS circuitry.

The E-cell detector in Fig. 1(a) operates in the following manner: Device N_1 is connected in a bias circuit with an external diode. The gate voltage of device N_2 is:

$$Vg_2 = V_D + V_N\ th + Ks\ (V_D - V_E) \qquad (1)$$

where Ks is the substrate effect constant in volts per volt of source reverse bias.

The source voltage of N_2 is the E-cell voltage (V_E), which is initially 0 volts. The threshold voltage of device N_2 may be described as follows:

$$V_{N_2}\ TH = V_N\ TH + K_S\ (V_E) \qquad (2)$$

N_2 will turn off when $V_{gs_2} \leq V_{N_2}\ TH$

$$V_{gs_2} = V_D + V_{N\ TH} + K_S\ (V_D - V_E) - V_E \qquad (3)$$
$$\leq V_{N\ TH} + K_S\ (V_E)$$

The effects of the actual threshold voltage cancel and switching occurs when:

$$V_E = \frac{(1 + K_S)}{(1 + 2K_S)} V_D \qquad (4)$$

For K_S = 1 volt/volt, switching will occur for an E-cell voltage equal to 2/3 the external bias (V_D). For a 0.5 volt diode, V_E = 0.33 volts, and thus the circuit will detect as the E-cell voltage makes the transition from 0 volts to 0.8 volts. Switching is very rapid due to the push-pull action of transferring substrate effect between devices.

The low-supply voltage detector in Fig. 1(b) utilizes the same basic concept. V_E, (V_{DD}-V_Z) in this case, is chosen such that device N_2 is off, and hence, for a given V_Z, the supply voltage at detection equals V_Z + V_E. The integrated circuit has a zener diode fabricated on-chip and an external limiting resistor to provide control of the sampling current. Present COS/MOS processing does not allow fabrication of forward biased diodes for the bias circuit without parasitic transistor action, hence an external diode is required.

Each integrated circuit contains two E-cell detectors and one low-voltage detector.

TIMING LOGIC

Fig. 2 illustrates the logic functions of the integrated circuit used for discrimination of input duration and control of delayed firing. A COS/MOS RC oscillator provides an accurate time base (T_1). A logic 1 at the over-ride input will start the oscillator. FF_1 divides by two and is the clock for a divide-by-8 counter and T_1 discriminator (FF_2). Output "Y" from the counter will cause detonation at $17T_1$ while FF_2 records T_1 and will cause detonation if the over-ride signal is removed after T_1. The anti-disturbance input utilizes the same countdown path so that the over-ride time delay dominates. Transistor count is greater than 150 devices.

OUTPUT

The output section of the integrated circuit, Fig. 3, consists of an SCR device, fabricated by means of the standard COS/MOS diffusion profiles, and control circuitry.

The signal from the arming E-cell detector controls device P_1, and allows charging of the firing capacitor after the arming delay. As the firing capacitor voltage reaches the threshold voltage of N_1, device N_2 is paralleled with the 20-kilohm shunting resistor, providing a

low-impedance shunt, while the capacitor voltage is applied to the SCR anode.

Firing signals from the timing logic, LVD, and end of mission E-cell detector are OR'ed for turn-on.

The SCR is a composite lateral-vertical-bipolar transistor with a PMOS transistor shunting the p-n-p emitter-collector. Turn-on is predominantly by means of MOS transistor P_2.

Typical ON resistance is two ohms.

Breakdown voltage is greater than 15 volts.

PERFORMANCE

Packaged in a 16-lead DIC, the circuit requires external timing resistors, timing and firing capacitors, LVD sampling resistor, and bias diode.

Current drain for the analog functions is less than 80 microamperes. The quiescent current drain of the COS/MOS logic is less than 10 microamperes. Peak firing current from a 120 microfarad capacitor at 5 volts into a 3-ohm load is one ampere.

Fig. 4 illustrates the distribution of low-supply voltage detection for 588 units.

Circuits have been delivered in quantity in both commercial and high-reliability grades. The engineering design test results for the system electronics are summarized below.

ENGINEERING DESIGN TEST RESULTS

Introduction

The XM56 Aircraft Mine Dispensing Subsystem is an aerially delivered scatterable mine system dispensing anti-tank, anti-vehicle mines. The XM56 electronic module, including battery, connectors, printed circuit board, external components, and integrated circuit, was tested with the following results:

Test Procedure

Aircraft Vibration - MIL-STD-810B
Transportation Vibration - MIL-STD-331
Temperature Conditioning - +125°F to -25°F
Rough Handling - MIL-STD-331
Jolt and Jumble - MIL-STD-331

Results

After being subjected to the above environmental tests, the items were electrically armed and allowed to time-out for self-destruct. The results of these tests were:

Arming - 96.3%
Self-Destruct - 98.9%

Mines were also ejected from a helicopter and subjected to anti-tank, anti-vehicle over-runs and anti-disturbance functioning with the following results:

	(Reliability (Point Estimate)
Anti-vehicle	*20-88.8%
Anti-tank	98.6%
Anti-disturbance	93.0%

*Dependent upon speed of vehicle

Failures in the above categories were determined to be caused by faulty components, such as switches and connectors, and to poor solder joints on printed circuit boards.

The electronic circuit has an over-all reliability of 98.6 percent (point estimate). There were no failures directly attributed to the integrated circuit.

CONCLUSIONS

The developmental work under this contract has demonstrated the feasibility of integrating low-power complementary MOS logic circuitry with SCR output capability. The ability to perform both analog and digital functions on a single integrated circuit makes COS/MOS the ideal choice for low-power, battery-operated, portable systems.

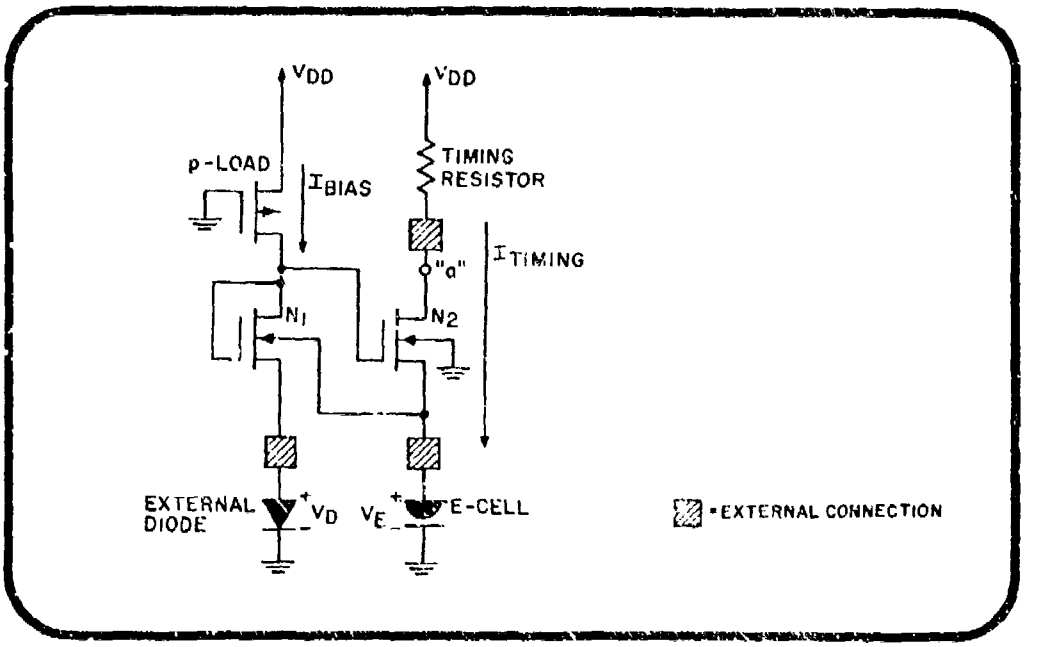

Fig. 1(a) - E-Cell Detector.

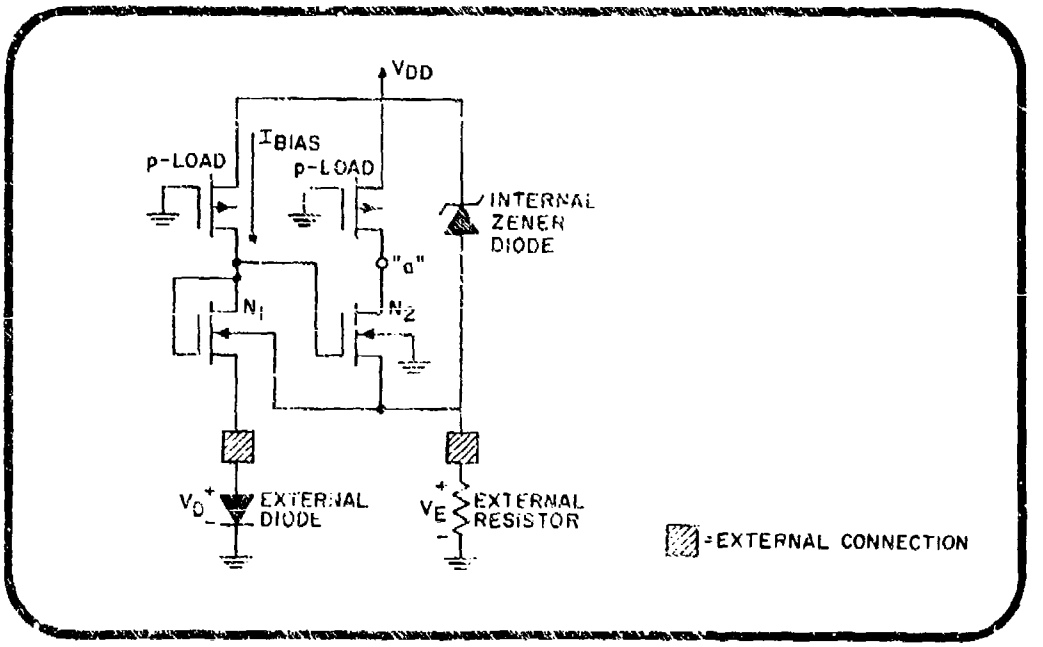

Fig. 1(b) - Low-Voltage Detector.

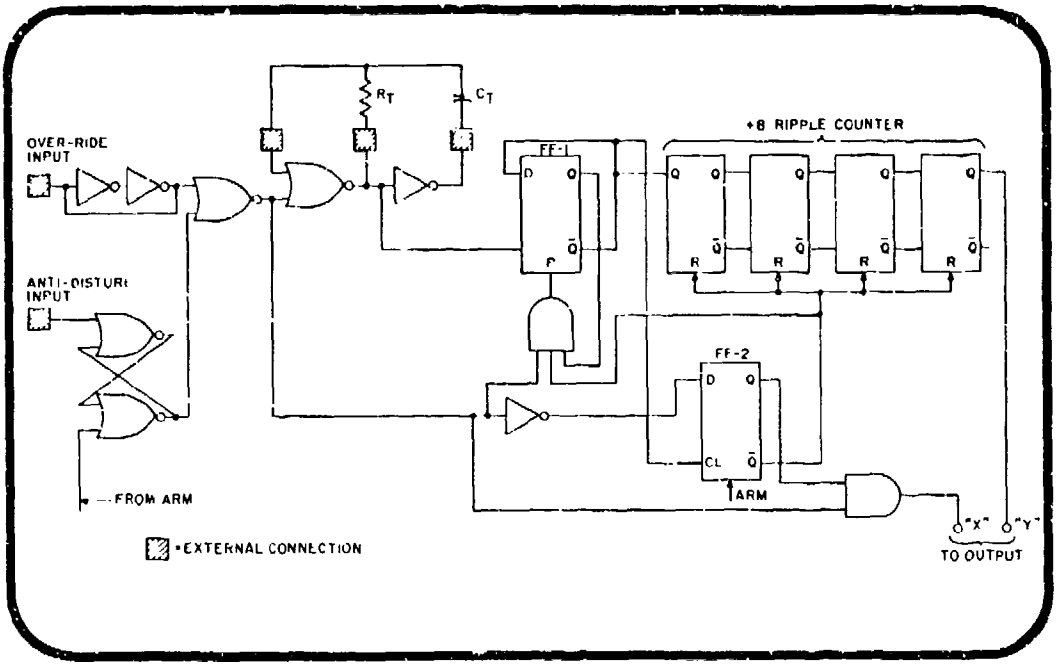

Fig. 2 - Timing Logic

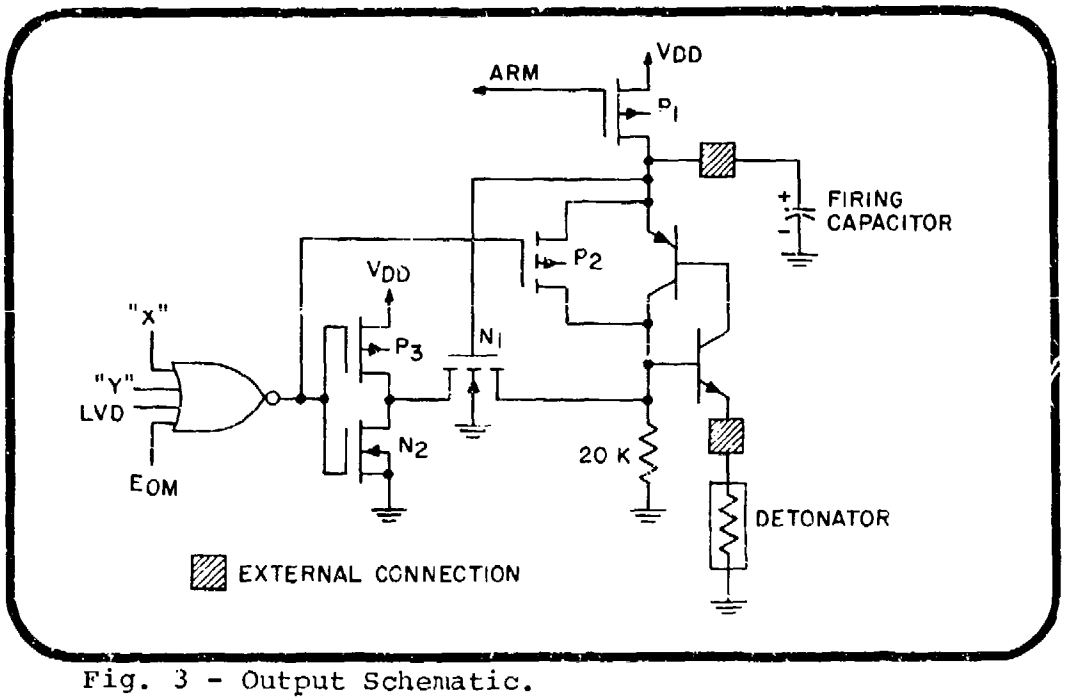

Fig. 3 - Output Schematic.

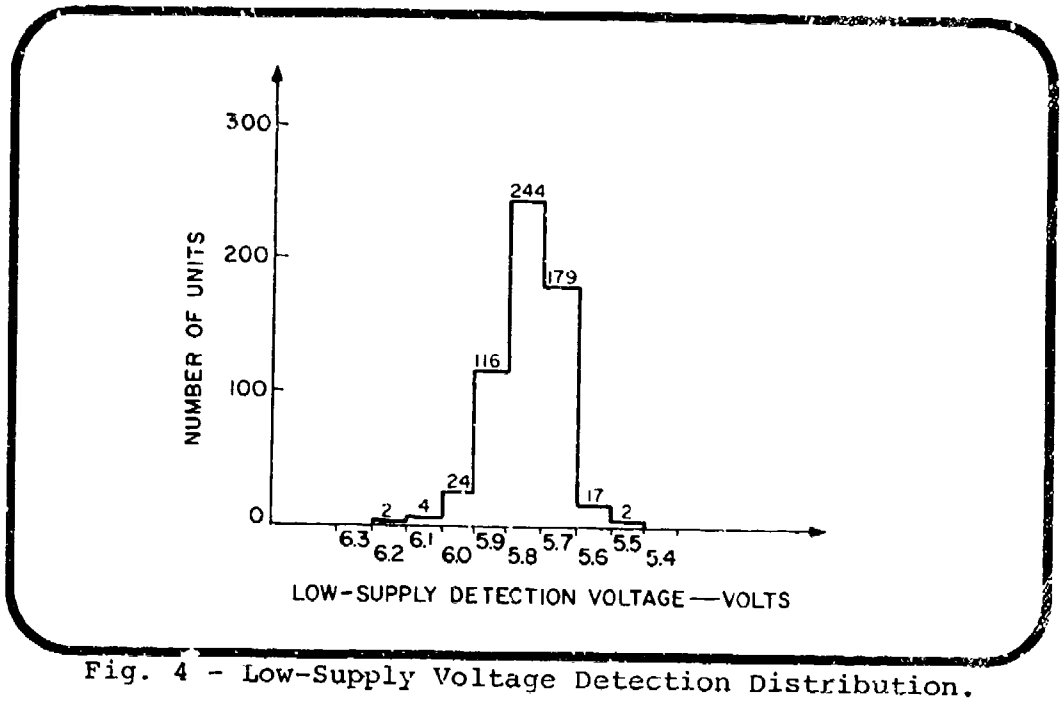

Fig. 4 - Low-Supply Voltage Detection Distribution.

A COMPUTER-AIDED METHOD FOR THE DESIGN OF A WIDE CLASS OF MICROWAVE COUPLERS AND FILTERS

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ABSTRACT

A numerical method, suitable for use in the computer-aided design of a wide class of microwave filters and couplers, is presented. The convergence characteristics of the method are illustrated. The performance characteristics of two directional couplers, designed and fabricated based upon results generated by the method, are shown. One coupler employs a configuration of microstrip over a slotted ground plane. The other coupler employs a "reduced" ground plane, with oversized microstrip lines.

INTRODUCTION

This paper describes and demonstrates the usage of a computer-aided method for designing microwave filters and couplers employing uniform, coupled sections of a wide class of transmission lines. Included in this class are microstrip, slot line, sandwich slot-line, and coplanar waveguide. Previously, efforts to incorporate the latter three transmission media in couplers and filters have been substantially empirical [1], [2], [3].

FORMULATION

The coupled transmission line structures treated in this work are characterized by the admittances and phase velocities of the even and odd modes of propagation. In terms of these quantities it has been shown how to design microwave directional couplers and filters [4].

The method developed in this work for computing these admittances and phase velocities is described as follows. Consider a specified configuration of dielectric loaded, coupled transmission lines in terms of which it is desired to design a directional coupler or filter. Now consider a second structure,

obtained from the first by fictitiously removing the dielectric regions, but retaining the same conductor geometry as in the original structure. This second structure will heretofore be referred to as the empty structure. For both the original and the empty structures quasi-TEM propagation models are invoked for both the even and odd modes of propagation. By virtue of these models, for each structure the even and odd mode transmission line capacitances to ground are computed in terms of scalar potential functions. Finally, the necessary admittances and phase velocities of the original structure are computed in terms of these capacitances.

The computational scheme is now described in somewhat greater detail for an arbitrary configuration of dielectric loaded coupled transmission lines. The cross section of this configuration is illustrated in Figure 1(a). The cross section of the corresponding empty configuration is shown in Figure 1(b). The application of quasi-TEM models to the even and odd modes of both configurations allows for mode excitations to be defined in terms of voltages. Hence,

$$\left.\begin{aligned} V_1 = V_2 &= 1 \\ V_3 &= 0 \end{aligned}\right\} \quad \text{even mode excitation} \tag{1}$$

and

$$\left.\begin{aligned} V_1 = -V_2 &= 1 \\ V_3 &= 0 \end{aligned}\right\} \quad \text{odd mode excitation} \tag{2}$$

Here, V_1, V_2, and V_3 are the voltages shown in Figures 1(a) and 1(b).

The computation of the even and odd mode transmission line capacitances, for a designated line in each of the two configurations, is accomplished as follows. The voltage excitation schemes from (1) and (2) are impressed on each configuration yielding four different distributions of scalar potential. The potential at any point P, in each of these four distributions, is of the form

$$\phi(P) = \int \sigma(\ell) \ln \frac{k}{R} \, d\ell \tag{3}$$

Here, σ is some equivalent source distribution which, for a structure of conductors and dielectrics, is the sum of free and bound charges. This source distribution lies along the boundaries of conductors and dielectrics. R is the distance between an equivalent source point, at path location ℓ, and the point P. k is a constant defined, due to numerical considerations, as

$$k > R_{max} \tag{4}$$

where R_{max} is the maximum value possible for R when P is constrained to lie at source points. The equivalent source distribution, corresponding to each of the four potential distributions and its corresponding excitation, is discretized and ultimately computed by a moment solution. The moment solution chosen here embodies a pulse function expansion of each source distribution and point matching of the boundary conditions. The capacitances to ground for the even and odd modes of the original and empty configurations are ultimately determined from their corresponding equivalent source distribution by strategically applying Gauss's Law at the conductor boundaries shown in Figures 1(a) and 1(b).

It is now shown how these two sets of even and odd mode capacitances, comprising the four cases previously mentioned, are used to compute the even and odd mode admittances and phase velocities for a configuration like the one shown in Figure 1(a). Let the even and odd mode capacitances to ground for one of the transmission lines in Figure 1(a) be represented by C_e and C_o, respectively. Similarly, for the corresponding transmission line in Figure 1(b), let the even and odd mode capacitances be represented by $C_{e,e}$ and $C_{e,o}$ respectively. Define the even and odd mode transmission line admittances for the configuration in Figure 1(a) according to the expression

$$Y_i = v_i C_i \tag{5}$$

Here, "i" can be either "e", for the even mode, or "o", for the odd mode. The phase velocities v_e and v_o can be expressed as shown in (6).

$$v_i = \frac{1}{\sqrt{L_i C_i}} \tag{6}$$

where the subscript "i" is defined as it was for (5). The transmission line inductance, L_i, introduced in (6) is defined implicitly by the expression for the phase velocity in the empty structure in Figure 1(b). Thus,

$$c = \frac{1}{\sqrt{L_i C_{e,i}}} \tag{7}$$

in (7), c is the velocity of light in free space. Finally, the admittances and phase velocities for the designated transmission line of the configuration in Figure 1(a) can be expressed succinctly as

$$Y_i = c\sqrt{C_i C_{e,i}} \tag{8}$$

and

$$v_i = c\sqrt{\frac{C_{e,i}}{C_i}} \tag{9}$$

It is the quantities Y_i and v_i which are pertinent to coupler and filter design.

The method described here has been programmed in Fortran IV for use on the CDC 3800 digital computer at the Naval Research Laboratory Computation Center. The matrix calculation portion of the program is a modification of a routine due to Pontoppidan [5].

The convergence of the method is illustrated in Figures 2 and 3. These figures show the variation in computed line impedance and phase velocity as the number of equivalent charge functions is varied on the strip and ground plane of a nominally 50 ohm microstrip line. Values due to Bryant and Weiss [6] are shown for reference. Convergence here produced agreement to within 3 percent compared to the reference values.

EXAMPLES

a. Microstrip-slotted ground plane configuration

A directional coupler was designed using computer results generated by the method described in the previous section. The coupler was fabricated on a 2"x1"x0.025" portion of alumina substrate using thin film techniques. The circuits on each side of the substrate are shown in Figures 4(a) and 4(b). The configuration used here is a variation of that used by Garcia [3] in a wideband, quadrature, 3 dB coupler developed empirically. The performance of the coupler developed in this work is illustrated in Figures 5(a), 5(b), and 5(c). The designed-for midband value is 5.4 dB, while the measured value is 5.3 dB. The coupling is 6.0 $\pm$ 0.7 dB over a 60 percent bandwidth about the midband frequency. Over more than an octave band, the return loss is 19.5 dB or better and the directivity is better than 14 dB. It is to be noted that this device is the result of a single design attempt using the computer results.

b. Reduced ground plane microstrip configuration

A second directional coupler, designed using the method presented here, was fabricated on a 2"x1"x0.025" portion of alumina substrate. The double-sided circuit employed is shown in Figures 6(a) and 6(b). Due to the non-optimal transition from narrow to wide microstrip, shown in Figure 6(a), the return loss of this coupler was originally 16 dB or better over the range from 2 to 4 GHz. The return loss characteristic was improved to that shown in Figure 7(b) by a simple tuning technique. The

performance of the coupler developed here is shown in Figures 7(a), 7(b), and 7(c). The designed-for and measure value of midband coupling is 6.8 dB. The coupling is 7.2 $\pm$ 0.4 dB over a 56 percent bandwidth about 3.125 GHz. Over the octave band shown in Figure 7, the return loss is 23 dB or better and the directivity is 13 dB or better.

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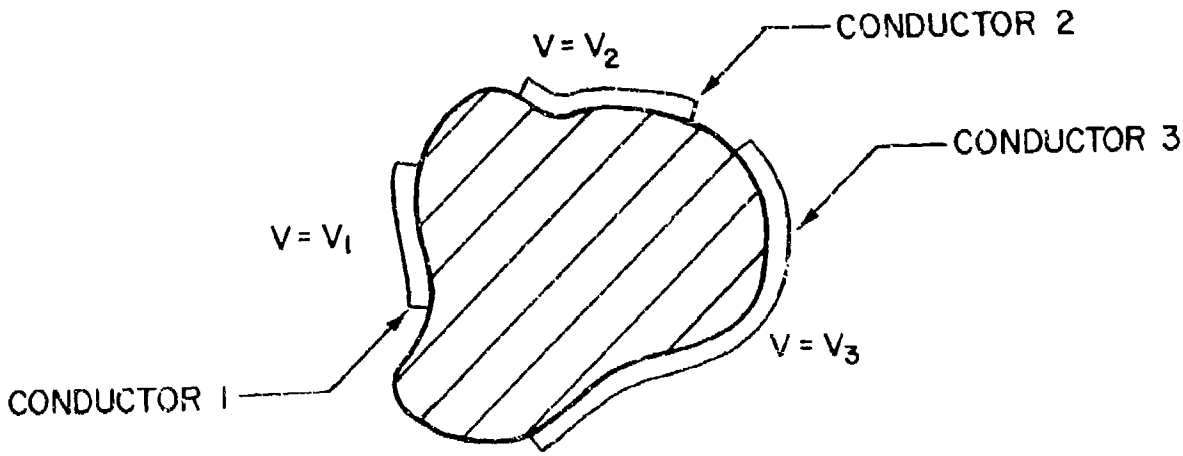
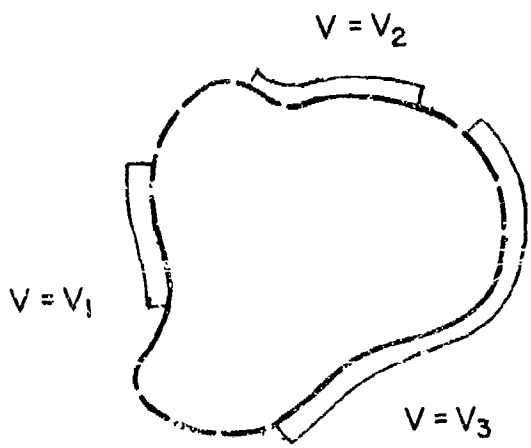


(a)



(b)

Figure 1 Cross Sections of Arbitrary Configurations of Coupled Transmission Lines (a) Dielectric Loaded (b) Empty.

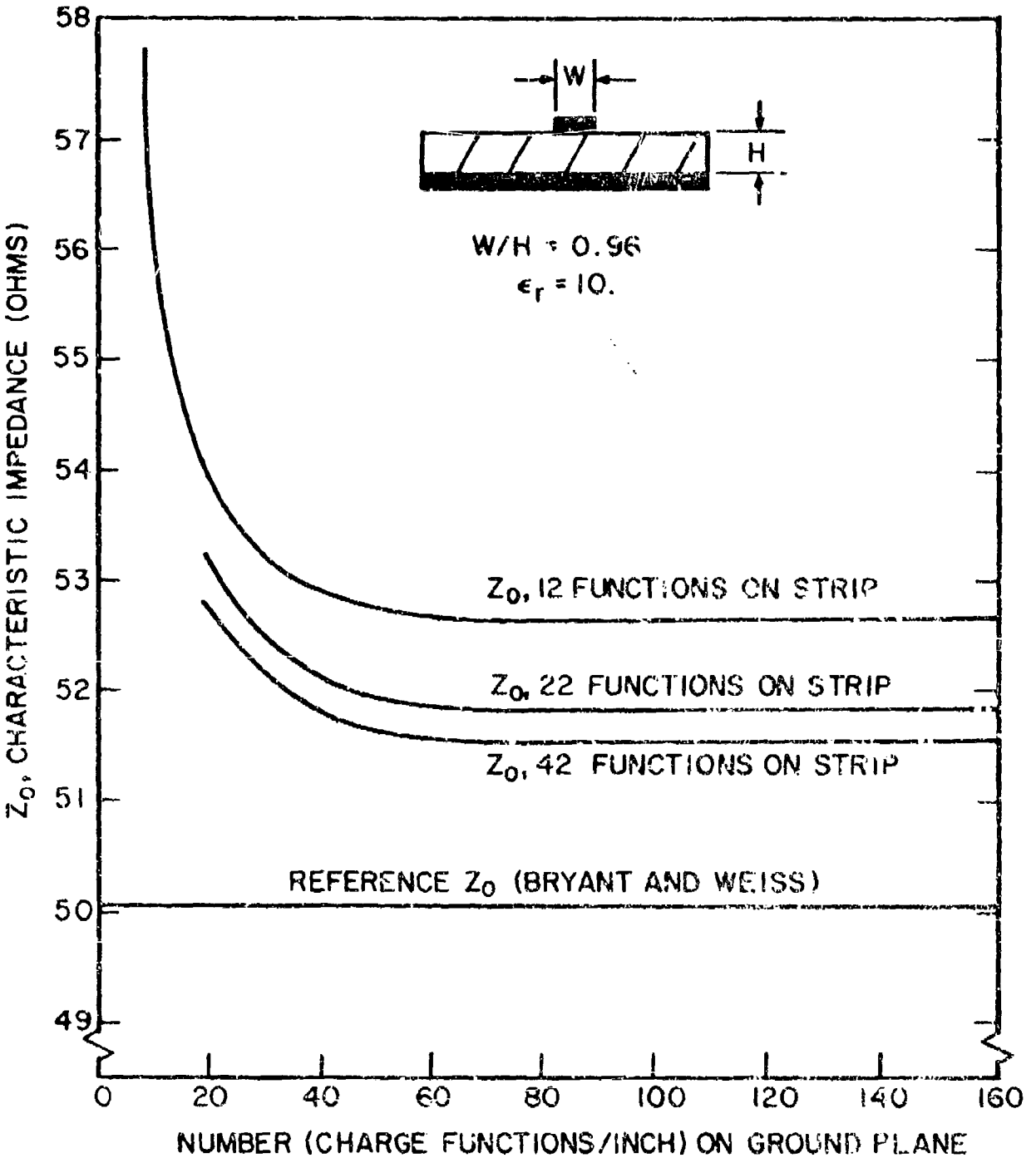


Figure 2 Convergence of Impedance for Microstrip Line.

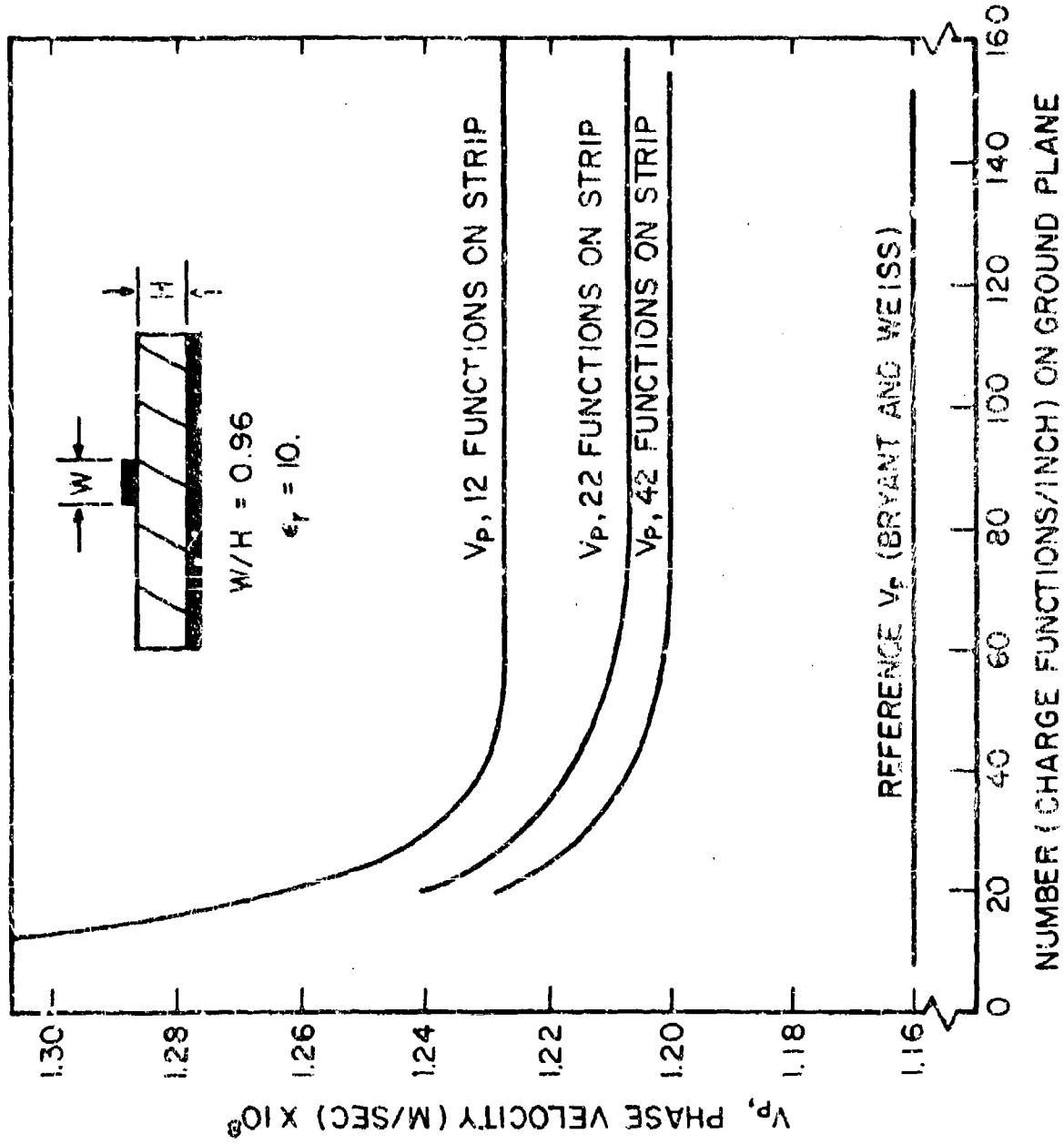
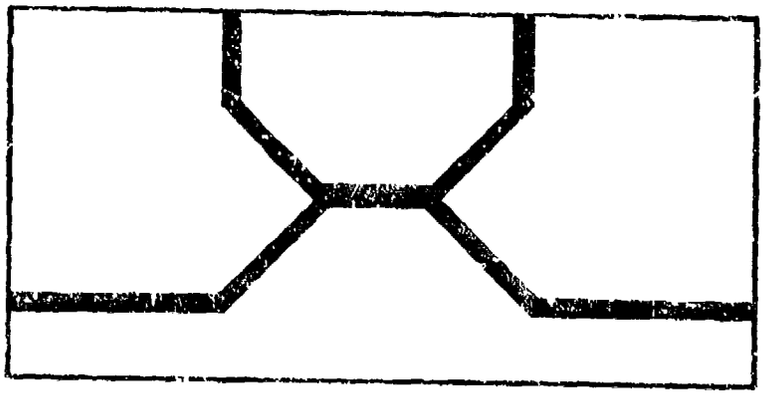
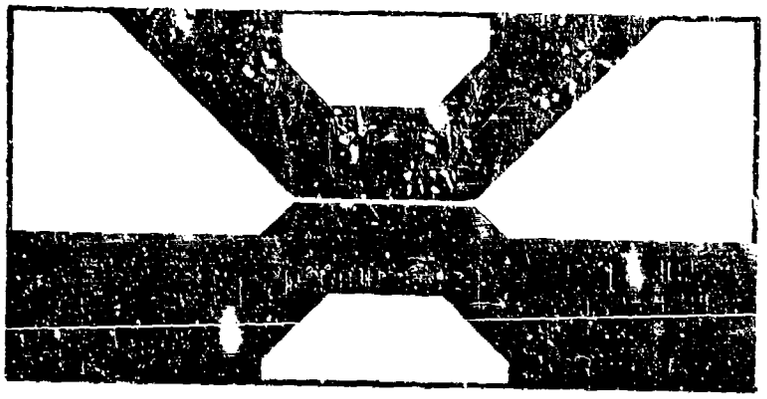


Figure 3 Convergence of Phase Velocity for Microstrip Line.



A



B

Figure 4 Microstrip Slotted-Ground Plane Coupler.

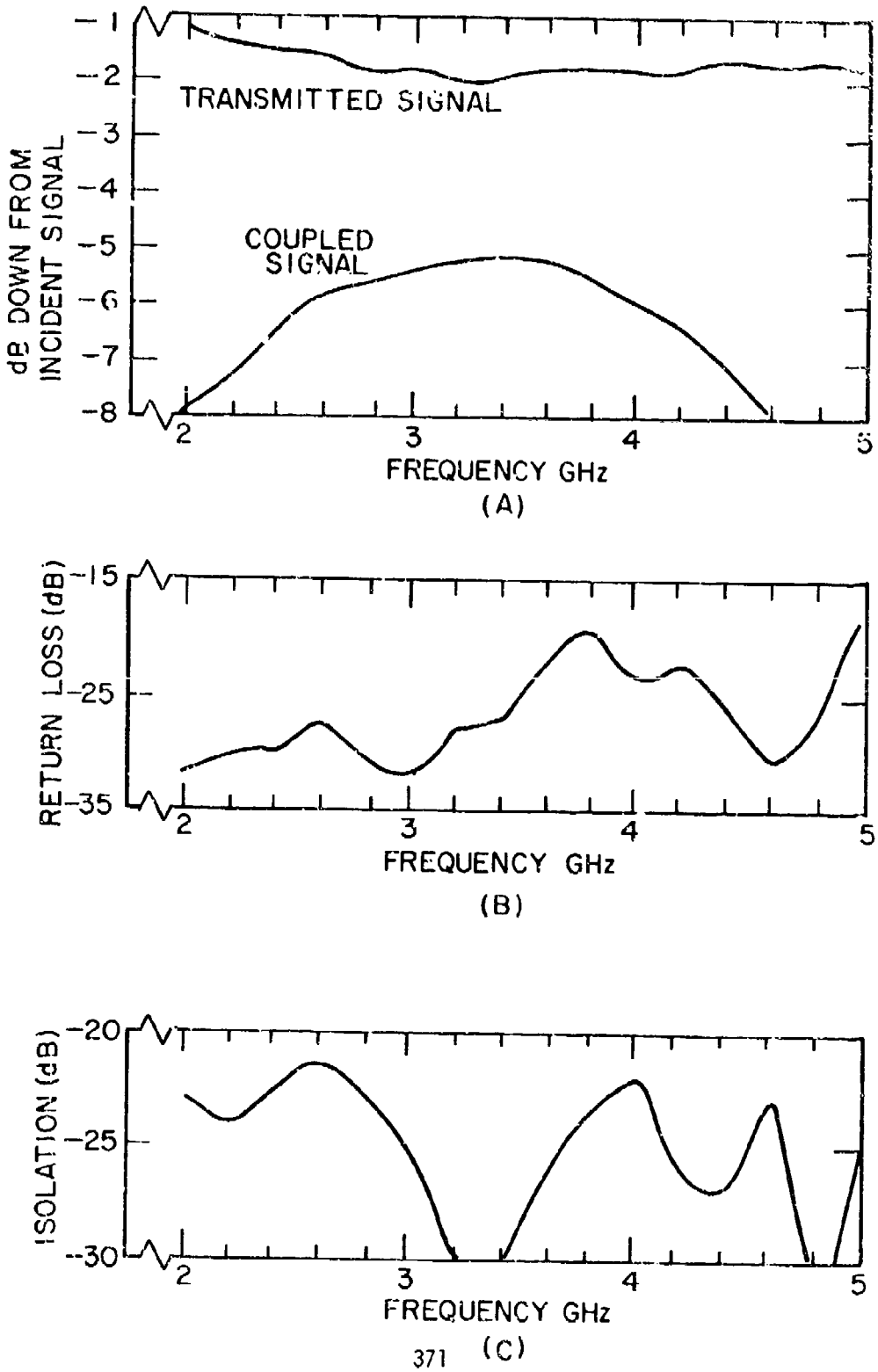
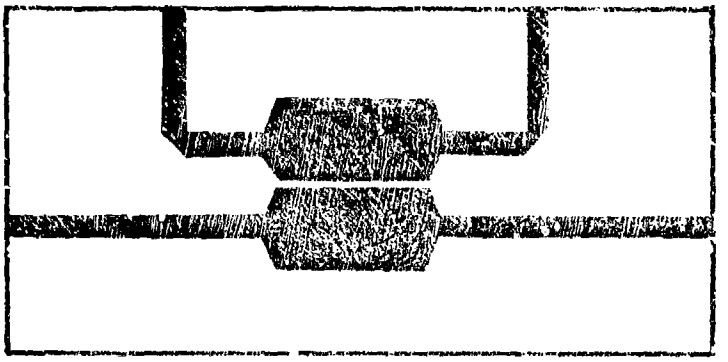
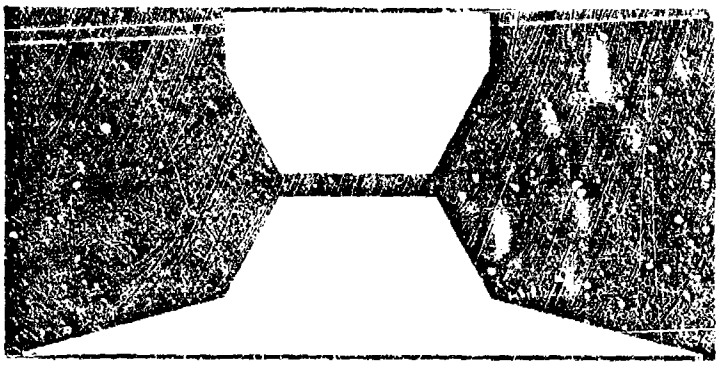


Figure 5 Performance of Microstrip Slotted-Ground Plane Coupler.



A



B

Figure 6 Circuit for Reduced Ground Plane Microstrip Coupler.

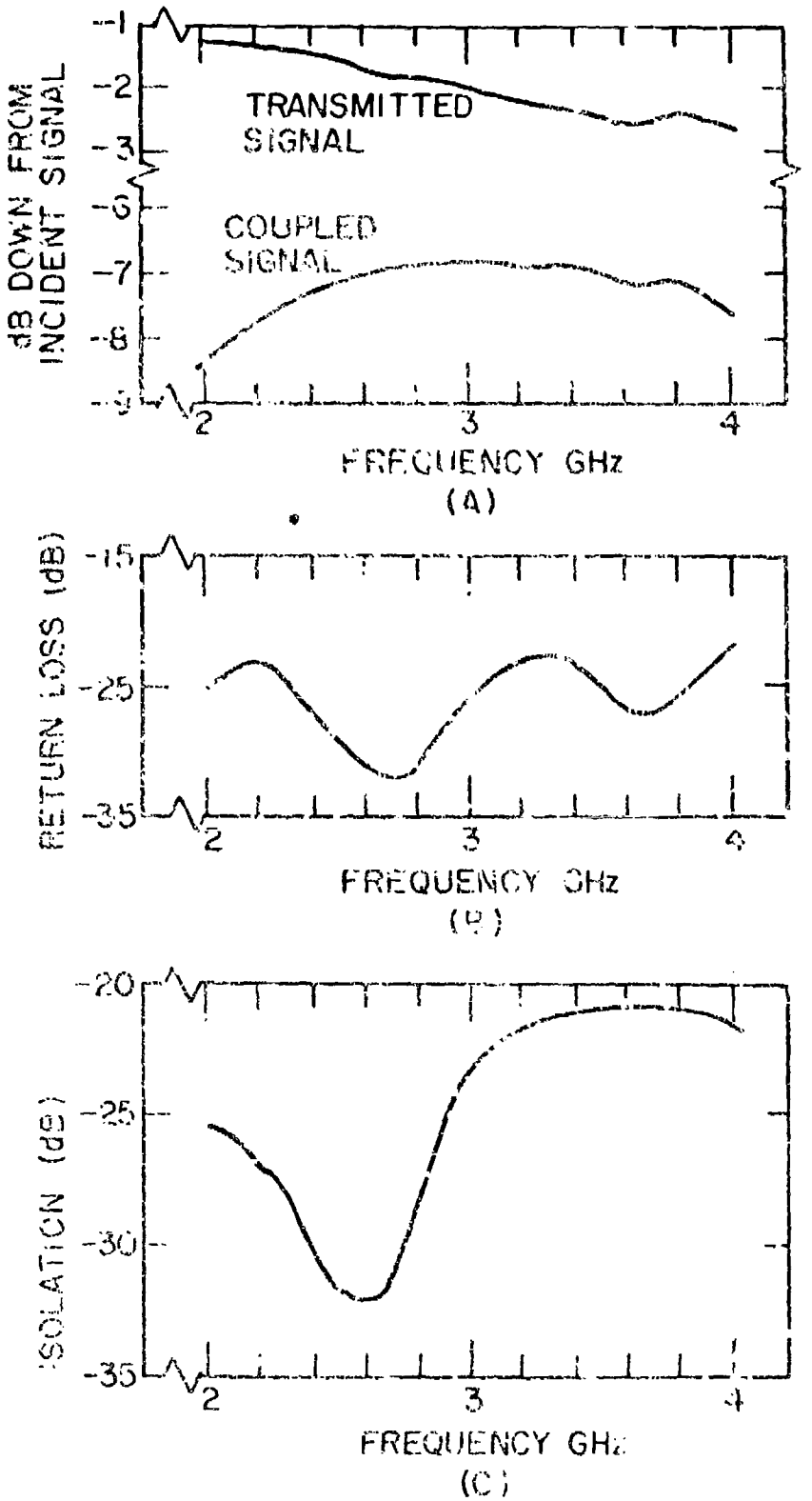


Figure 7 Performance of Reduced Ground Plane Microstrip Coupler.

MICROWAVE INTEGRATED FILTERS

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ABSTRACT

Passive high Q filter elements capable of satisfactory performance in the Microwave Integrated Circuit area are restricted to dielectric and YIG resonators. However, temperature enevironment may limit their usefulness unless certain techniques are utilized in the design and fabrication of these I.C. filter elements.

INTRODUCTION

Physical dimensions of microwave filters have been significantly reduced by the use of integrated microcircuits. However, reducing the cavity size to an extent comparable with other miniaturized elements usually results in a drastic reduction in Q. In contrast to waveguide components for which Q's range between 5,000 and 15,000, microstrip transmission circuit resonator Q's range between 100 to 300. There are, nevertheless, significant I.C. applications for which Q's comparable to waveguide values are required, i.e. require high Q passive filters. High Q's are necessitated when bandwidths of 0.1% or less are desired.

Passive high Q filter types useful for integrated microwave circuits are limited to the following:

1. Dielectric
2. YIG (Yttrium-Iron-Garnet)

However, temperature environment can restrict their usefulness unless these filters are designed by specific guidelines.

DIELECTRIC RESONATORS

Low loss, high dielectric constant objects will resonate in a microstrip configuration for sizes more than an order of magnitude smaller than the waveguide cavity equivalents. The dielectric resonator is the electromagnetic dual (E & H fields are interchanged) of the metal wall cavity. Microwave energy will be confined to a region in and near the resonator provided the dielectric constant is sufficiently high. The disk geometry has been found most suitable for integrated circuit devices. With proper choice of length to diameter ratio, a disk insures a large frequency separation between the fundamental resonance mode, $TE_{01}\delta$ and the next higher order mode. Radiation losses are suppressed for sufficiently high dielectric constant material ($\epsilon_r \geq 80$). High unloaded Q ($Q_u = 1/\tan\delta$) will be obtained at microwave frequencies, if the dielectric constant is large ($\epsilon_r \geq 80$). Unloaded Q's, Q_u, of 3,000 to 10,000 are available from such single crystal materials as rutile, TiO_2 ($\tan\delta \leq 0.0001$). A microstrip S-Band double pole filter configuration is shown in Figure 1. All coupling from line to disk and disk to disk is magnetic or dipole type. The butterworth filter has a frequency response at 2.3GHz as shown in Figure 2; an insertion loss of 2.4db and a 3db bandwidth of 4.6MHz. The temperature sensitivity by the following equation:

$$\frac{\Delta f}{fo} = \pm \frac{1}{2} \frac{\Delta \epsilon_r}{\epsilon_r} \qquad (1)$$

where $\epsilon_r = \epsilon_r$ (T)

At S-Band frequency, rutile has a TCK (temp. coefficient of permittivity) of -1000 PPM/°C over 50 to 100°C, which can be translated into a 50MHz change in center frequency. This temperature sensitivity has limited, to some degree, the usefulness of I.C. dielectric filters.

However, advances in obtaining a temperature stable materials are being made. Usually materials with high ϵ_r also have negative TCK such as rutile; nevertheless, materials with fairly high permittivities with positive TCK do e.g. $Bi_4 Ti_3 O_{12}$ and Ca Ti Si O_5. Mixing of materials (one with high positive and the other high negative TCK) in the proper volume fraction will result in a temperature stable (low TCK) material. Usually the ϵ_r is reduced below a value which is useful for microwave filter applications. The most promising material (from the standpoint of obtaining a low loss, high dielectric constant, temperature stable microwave dielectric) investigated to date is $Bi_2O_3TiO_2CaOZrO_2$. The characteristics of this material as well as others investigated at Westinghouse will be discussed.

YIG FILTERS

YIG resonators make use of bulk gyromagnetic materials and are typically formed into spheres which are 20 to 50 mils in diameter. For numerous integrated circuit applications, permanent magnet (rather than electromagnetic) bias would be used except for its extreme frequency sensitivity over a given ambient temperature range (typically 1 to 2MHz frequency drift per 1° C change in temperature at C-band frequencies).

This paper describes an integrated circuit, C-band double-pole YIG filter[1] with a permanent magnet biasing source. This filter has been temperature stabilized by a simple yet effective method which simultaneously compensates the permanent magnet and YIG resonator. This planar filter shown in Figure 3, consists of two shielded microstrip transmission lines separated by a metal wall. The RF transmission lines are deposited on an alumina substrate with the YIG spheres and the positioning rods imbedded in the upper dielectric medium. At resonance, energy is coupled from the input line to the first YIG. The first YIG, then radiates a circularly polarized field which propagates thru the metal iris and couples the energy to the output line. The purpose of the coupling slot is to prevent direct coupling from the input to output line.

A method has been developed for temperature stabilizing the resonant frequency of the YIG filter which eliminates the need for temperature compensating shunts on the permanent magnets and high precision X-ray orientation of the YIG sphere. Instead of eliminating these two effects, this technique uses the temperature sensitive anisotropy of the YIG to cancel the corresponding change in the biasing field. No pre-orientation of the YIG along a preferred crystalline axis is required. The YIG sphere is merely rotated to a position such that

$$\frac{\Delta H_o}{\Delta T} + F(\theta)\frac{\Delta H_a}{\Delta T} = 0 \qquad (2)$$

where

$F(\theta)H_a$ = effective internal anisotropy field (oe)
H_o = external magnetic biasing field (oe)
H_a = temperature dependent anisotropy field (oe)

Once this is accomplished, the center frequency of the filter is stabilized to $\pm$ 1MHz over the temperature internal of + 20° C to 70° C, as shown in Figure 4. This represents a reduction in the drift by a factor or 50. Interpole tracking of the two resonators was better than $\pm$ 1MHz over the 100° C temperature interval.

CONCLUSION

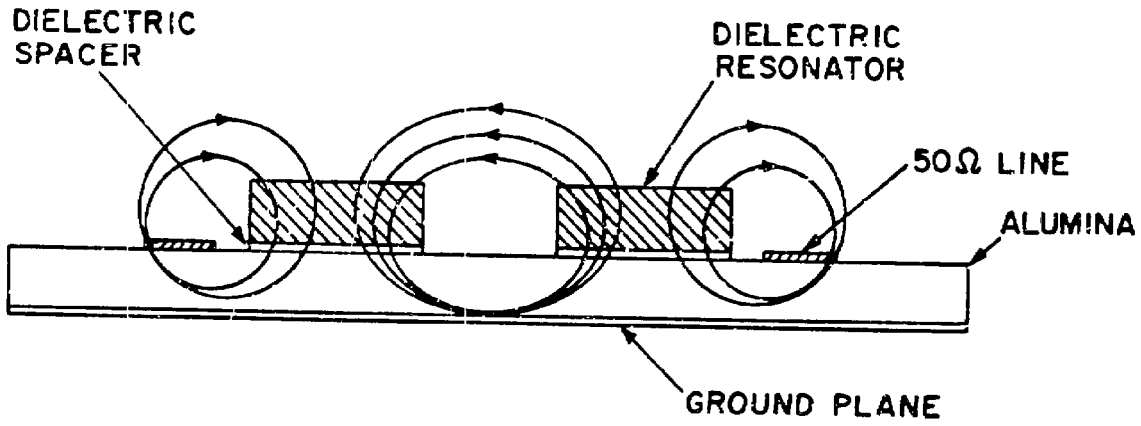
I.C. Dielectric and YIG filters demonstrate characteristics which make them valuable for Microwave Integrated Circuit design.

REFERENCE

1. J. M. Schellenberg and R. R. Jones, "YIG To YIG Coupling Cuts Temperature Drift", Microwaves, June, 1972.

Figure 1

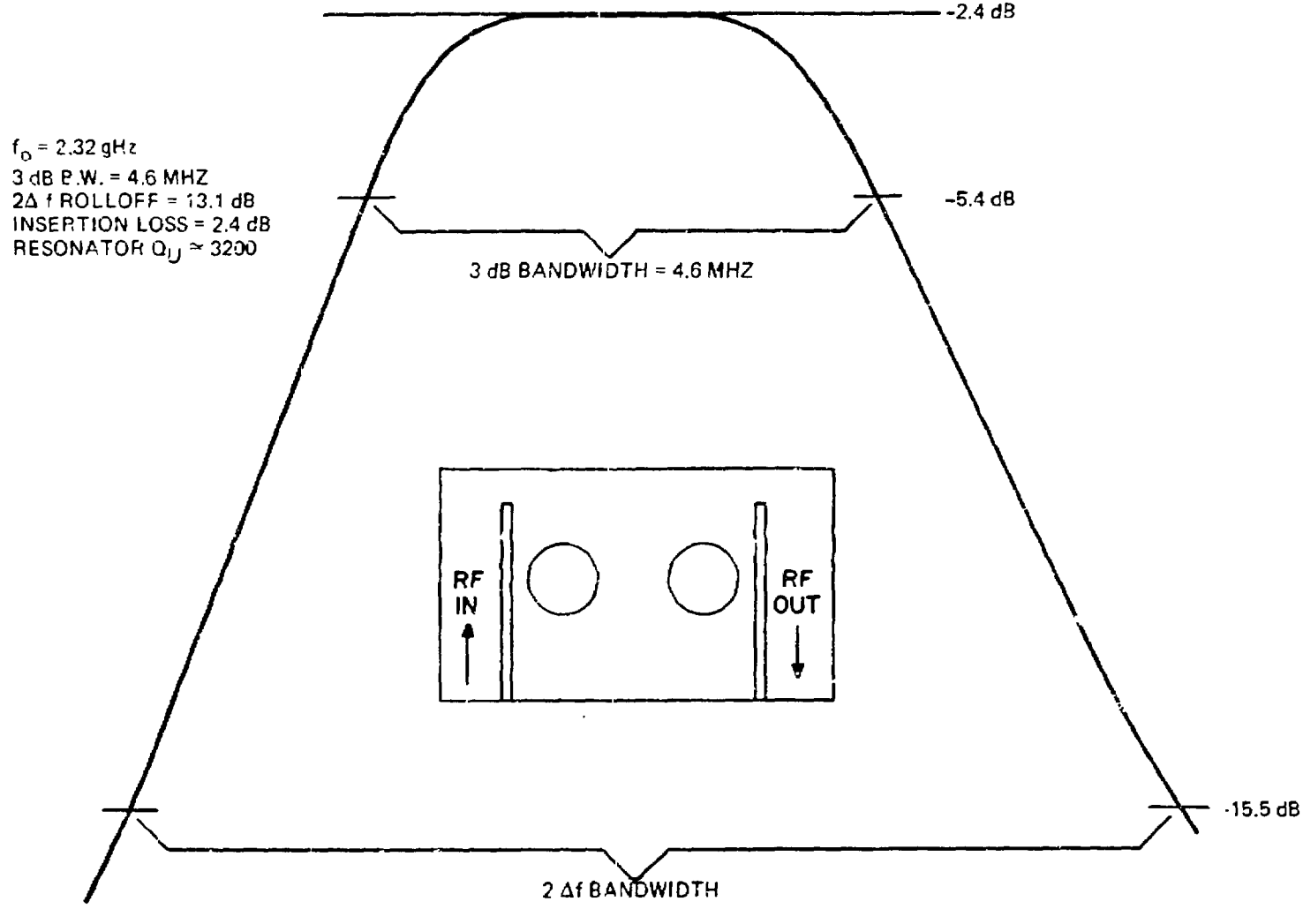
FIELD OF DIELECTRIC DISKS IN MICROSTRIP GEOMETRY



$$k \propto \frac{D^4 L \epsilon_r}{\lambda_0^2} \frac{H_2}{M_1}$$

Figure 2

PASSBAND RESPONSE OF TWO-POLE MICROSTRIP DIELECTRIC FILTER



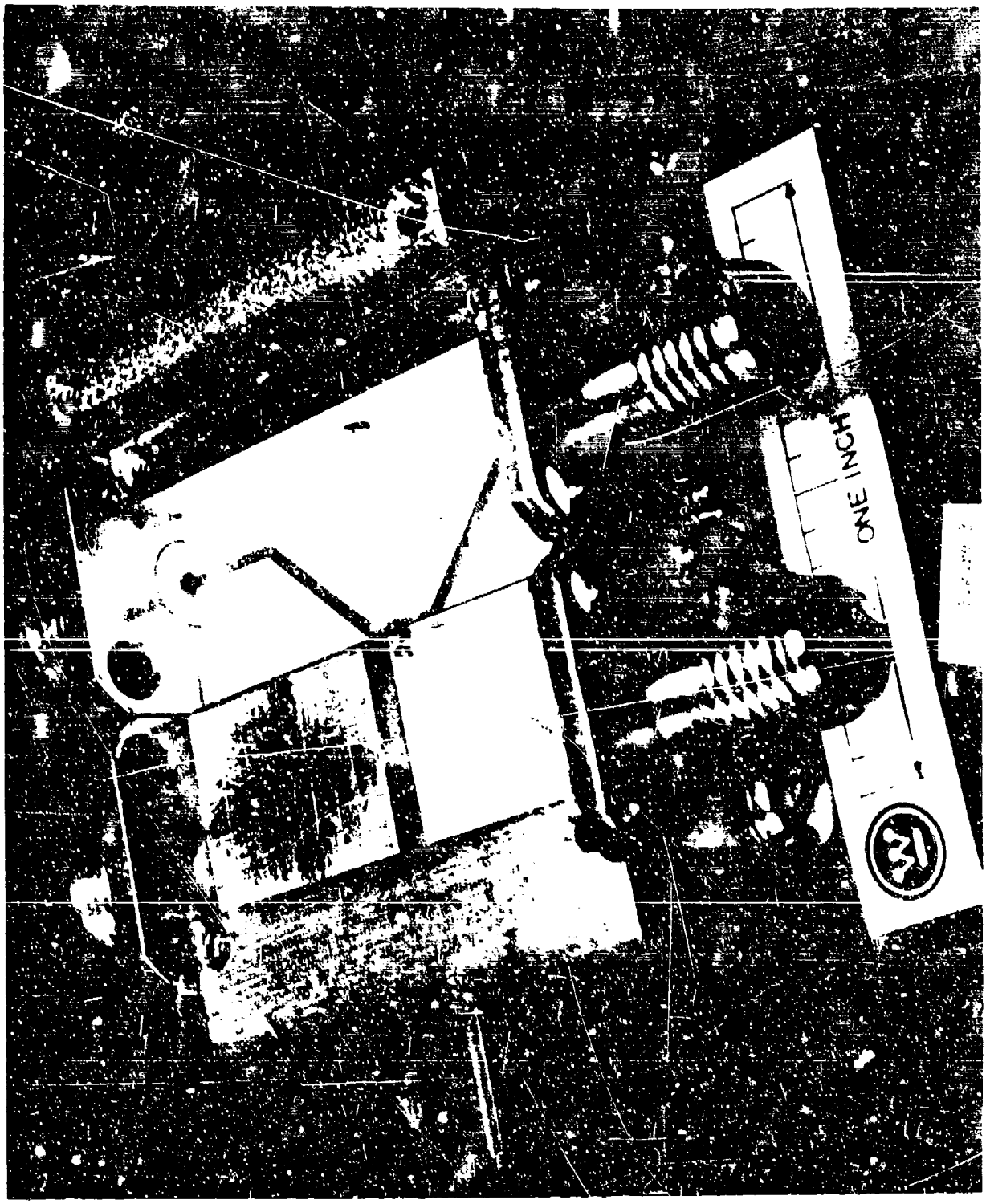
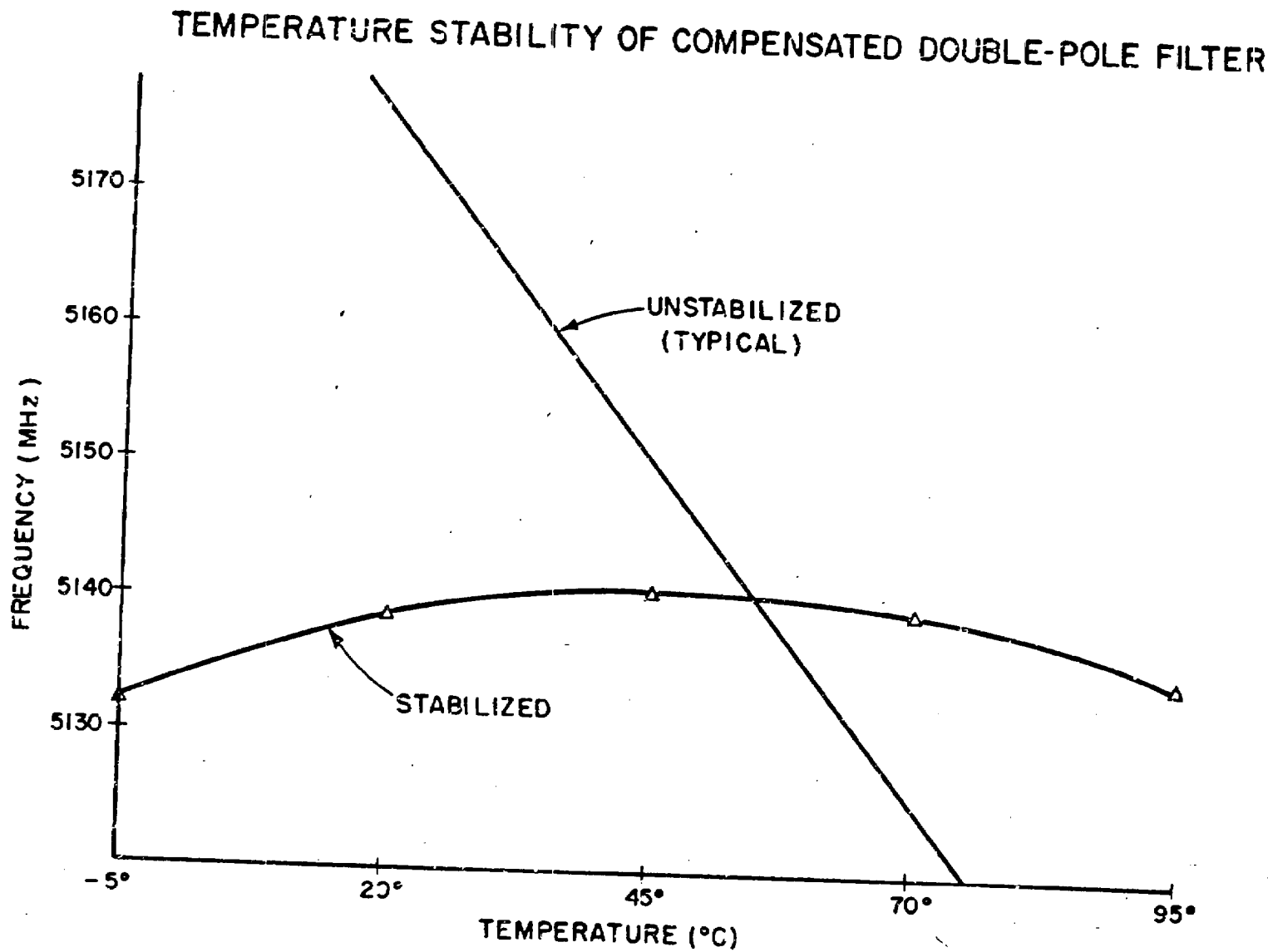

ONE INCH

Figure 4


TEMPERATURE STABILITY OF COMPENSATED DOUBLE-POLE FILTER
FREQUENCY (MHz)
5170
5160
5150
5140
5130
UNSTABILIZED
(TYPICAL)
STABILIZED
-5°
20°
45°
70°
95°
TEMPERATURE (°C)

QUASI-LUMPED MICROSTRIP DIRECTIONAL COUPLERS

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ABSTRACT

Theoretical and experimental results are presented on quasi-lumped directional couplers in microstrip, employing interdigitated capacitors as the coupling elements. The principal advantage of the technique is that tight coupling can be produced, in small size, with straightforward, single-step, photolithographic processing.

INTRODUCTION

The lumped interdigitated capacitor on microstrip has been discussed by Alley [1], and a quasi-lumped directional coupler has been described briefly by Peppiatt, Hall, and McDaniel [2]. Combining and extending these two ideas has produced a useful microstrip component.

TWO-CAPACITOR COUPLER

An example of the experimental microstrip coupler developed in this work, shown in the Figure 1 drawing, consists of transmission lines on a dielectric substrate above a ground plane. Interdigitated capacitors are shown as coupling elements, separating the main transmission lines far enough that there is no significant direct coupling between them.

Figure 2 shows the electrical equivalent circuit of the microstrip configuration. The Even and Odd Mode analysis technique, summarized in [3], is a convenient method for the solution of the performance of circuits of this type. To review briefly, the ABCD matrix relates circuit input quantities to output quantities according to

$$\begin{bmatrix} E_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} E_2 \\ I_2 \end{bmatrix} \quad . \tag{1}$$

The ABCD matrices of the even mode circuit and the odd mode circuit, shown in Figure 3, are determined independently. Even and odd mode transmission and reflection coefficients are then determined and used to calculate the emerging voltage vectors (b_1 through b_4) at the terminals of the four port network. The even and odd mode ABCD matrices are the following:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} \cos\theta & jZ_o \sin\theta \\ jY_o \sin\theta & \cos\theta \end{bmatrix} \tag{2}$$

and

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_o = \begin{bmatrix} \cos\theta - 2\omega C Z_o \sin\theta & jZ_o \sin\theta \\ j(4\omega\cos\theta + Y_o \sin\theta - 4\omega^2 C^2 Z_o \sin\theta) & \cos\theta - 2\omega C Z_o \sin\theta \end{bmatrix} , \tag{3}$$

where ω is radian frequency and the other terms are as defined in Figure 3. For the coupler shown, the condition for infinite isolation ($b_2 = 0$) and perfect match ($b_1 = 0$), occurring simultaneously, is that

$$\tan\theta_o = \frac{1}{\omega_o C Z_o} \quad , \tag{4}$$

where ω_o is the radian frequency of infinite isolation and θ_o is the electrical length of the interconnecting transmission lines at that frequency. When this value of θ_o is inserted into the equation for the voltage emerging at Port 3, the value of voltage coupling at ω_o is determined to be

$$b_3 = \cos\theta_o \quad . \tag{5}$$

Using the circuit values obtained from the desired coupling value at ω_o, the complete performance versus frequency may be determined directly from the general equations given in Figure 3.

Figure 4 gives the computed response of a directional coupler of this type, whose values are selected for 3 db coupling at 1250 MHz design center ($C = 2.54$ pf and $\theta_o = 45$ degrees). Useful bandwidth is about 10%, length is only one-eighth wavelength, and width is that required to assure negligible direct main line coupling. In general, capacitance values are small - a few picofarads at 1 GHz - with required values decreasing as frequency increases and as coupling loosens, making the capacitors realizable using interdigitated capacitor techniques on microstrip.

The photograph in Figure 5 shows two quasi-lumped microstrip couplers on .025 inch thick alumina substrate. Data from the upper unit, a 6 db coupler at 1450 MHz, is given in Figure 6. The capacitors have 22 fingers, .060 inch long, with .0035 inch wide lines and .0014 inch spaces. Data for the lower unit is given in Figure 7. The capacitors have seven fingers, .230 inch long, with .0022 inch wide lines and .0014 inch spaces. This measured data has been compared with computed response curves in each case, in order to establish whether the coupler bandwidth may be significantly affected by the capacitor form factor (length to width ratio). The computations assumed frequency independent capacitors, while the actual capacitors used show some frequency dependence, which is related to form factor. However, bandwidth deviation from computed values was negligible for both capacitor types. Therefore, it was concluded that increasing the number of coupling elements should be investigated as a means to achieve wider bandwidth.

THREE-CAPACITOR COUPLER

The analysis for a three capacitor coupler was carried out using the procedure described earlier. Figure 8 shows the equivalent circuit of the device analyzed. The simplifications used were that the two end capacitors are equal and the four interconnecting lines are of equal length. The equations for the even and odd mode ABCD matrices are the following:

<u>Odd</u>

$$A = \left[(4\omega^2 C_1 C_2 Z_o^2 - 1)\tan^2\theta - (4\omega C_1 Z_o + 2\omega C_2 Z_o)\tan\theta + 1\right]\cos^2\theta$$

$$B = j\left[(-2\omega C_2 Z_o^2)\tan^2\theta + (2Z_o)\tan\theta\right]\cos^2\theta \qquad (6)$$

$$C = j\left[(8\omega^3 C_1^2 C_2 Z_o^2 - 4\omega C_1)\tan^2\theta + (2Y_o - 8\omega^2 C_1^2 Z_o - 8\omega^2 C_1 C_2 Z_o)\tan\theta + (4\omega C_1 + 2\omega C_2)\right]\cos^2\theta$$

$$D = A$$

Even

$$A = \cos 2\theta$$

$$B = jZ_o \sin 2\theta$$

$$C = jY_o \sin 2\theta \qquad (7)$$

$$D = A$$

Solving again for the condition of infinite isolation and unity VSWR, which occur simultaneously, provides the following:

$$\tan\theta = \frac{2\omega C_1 Z_o (C_1 + C_2) \pm \sqrt{4\omega^2 C_1^4 Z_o^2 + 4C_1^2 - C_2^2}}{4\omega^2 C_1^2 C_2 Z_o^2 + C_2 - 2C_1} \qquad (8)$$

Two poles of isolation are apparent - one for the positive sign before the radical and one for the negative sign. The two poles may be simultaneously located at the coupler design center frequency by requiring that the term under the radical be zero. The resultant condition is that

$$C_2 = 2C_1 \sqrt{\omega^2 C_1^2 Z_o^2 + 1} \qquad (9)$$

For perspective, Figure 9 gives a plot of a specific case in which f_o is 1250 MHz and Z_o is 50 ohms. Coupling values from approximately 40 db to 0.5 db are shown, with C_1 values from about .02 pf to 2 pf. The line length required is also plotted and C_2 is assumed to be the value given by equation (9). The 50 ohm, 3 db coupler case, with both isolation poles located at 1250 MHz, requires C_1 = 1.1 pf, C_2 = 2.4 pf, and θ = 56.7 degrees. The computed response is plotted in Figure 10, where it is compared with the computed performance of the two capacitor coupler.

Other cases may be of interest in which the simultaneous location of the two poles of isolation at f_o is not the primary design criterion. A zero db coupler may be produced, for example, with parameters which are equivalent to a tandem connection of two-capacitor 3 db couplers, having a single pole of isolation at f_o. A 3 db, three-capacitor coupler with all capacitors equal may also be produced. Although it has only a single pole of isolation at f_o, its bandwidth is slightly greater than the two-capacitor version. All of the couplers described have 90 degree phase difference at f_o between the direct and coupled output ports.

SUMMARY

An analysis technique for multi-capacitor directional couplers has been presented which may be extended to any number of coupling elements. A technique of fabrication on microstrip using interdigitated coupling capacitors has been demonstrated, with measured results in agreement with computed performance. In many relatively narrow band applications, the use of this coupler design can eleminate the cross-over complication and/or the larger size of other types of microstrip couplers.

ACKNOWLEDGMENT

The author wishes to thank Mr. C. Banks for his support in the generation of the information for and the testing of the experimental circuits and for his assistance in the graphical presentation.

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[3] R. Levy, in "Advances in Microwaves, 1966," (Leo Young, ed.), Vol. 1, page 125FF, Academic Press, New York and London, 1966.

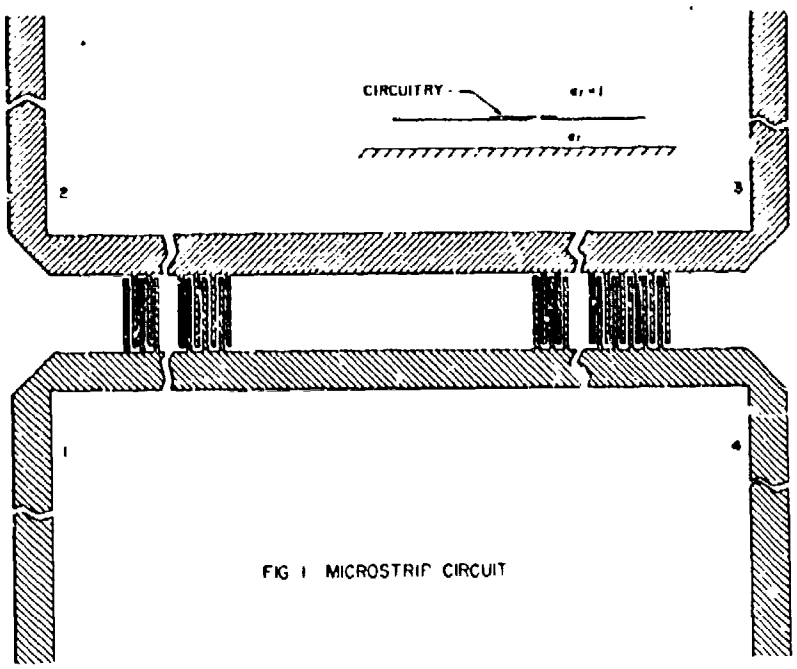

FIG 1 MICROSTRIP CIRCUIT

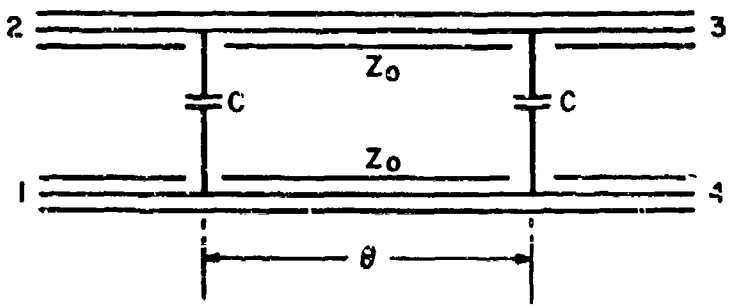

FIG. 2 ELECTRICAL CIRCUIT

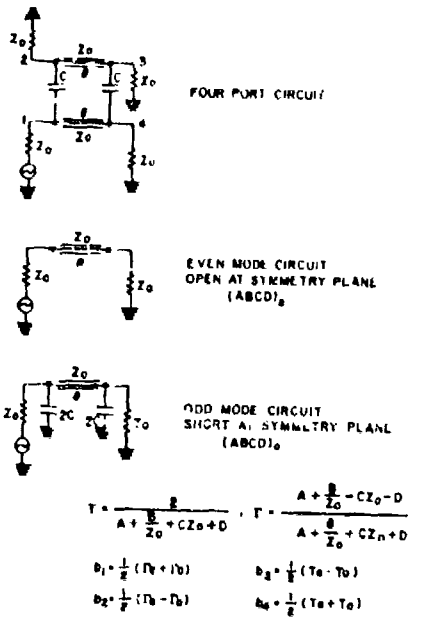

FIG 3 ANALYSIS CIRCUITS

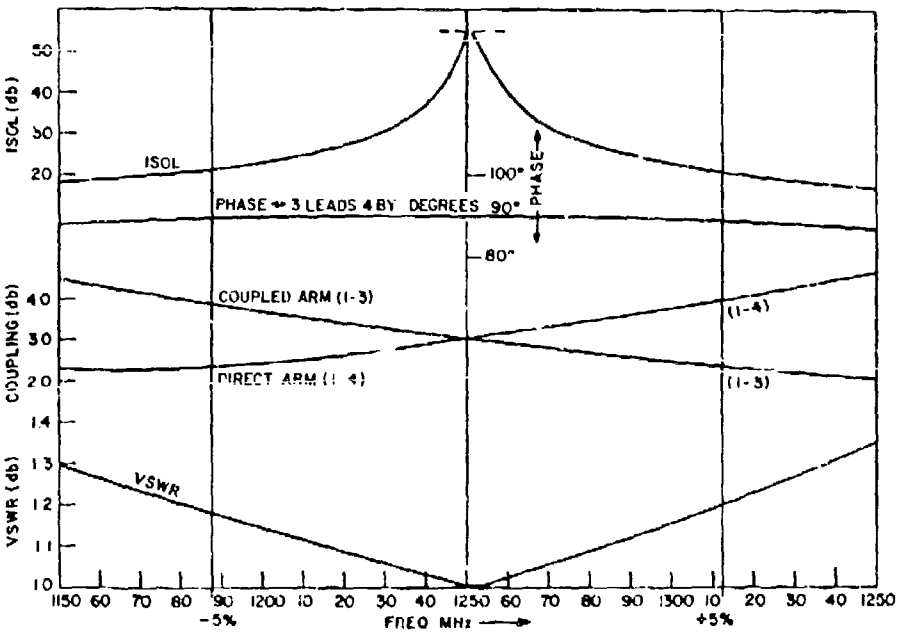

FIG 4 COMPUTED PERFORMANCE

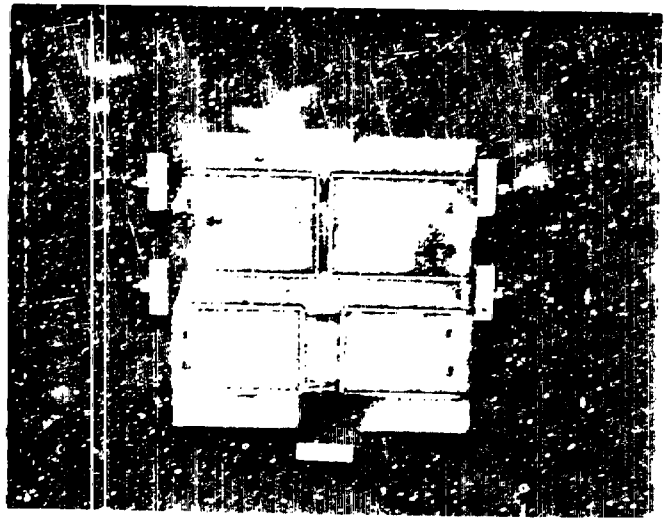

FIG. 5 QUASI-LUMPED COUPLERS

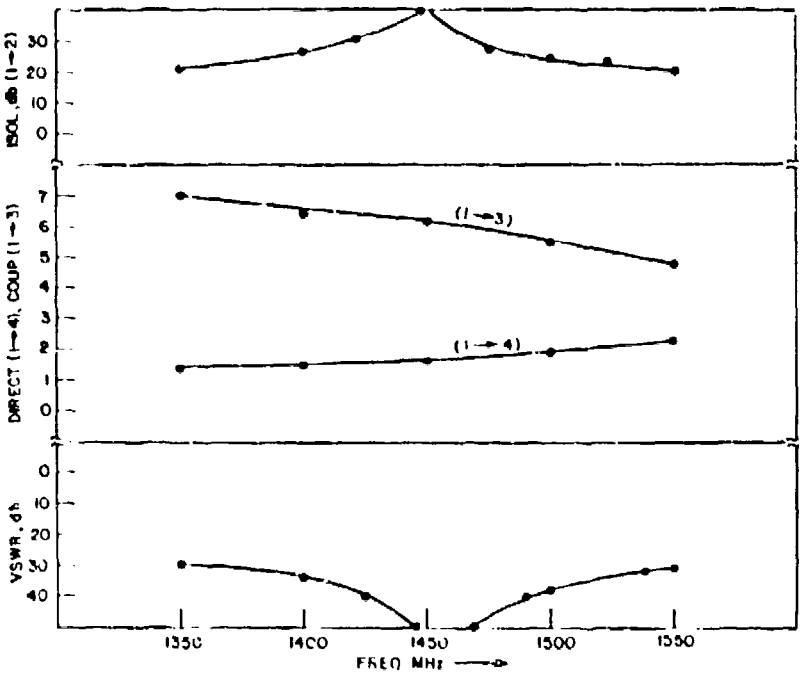

FIG 6 6db COUPLER DATA

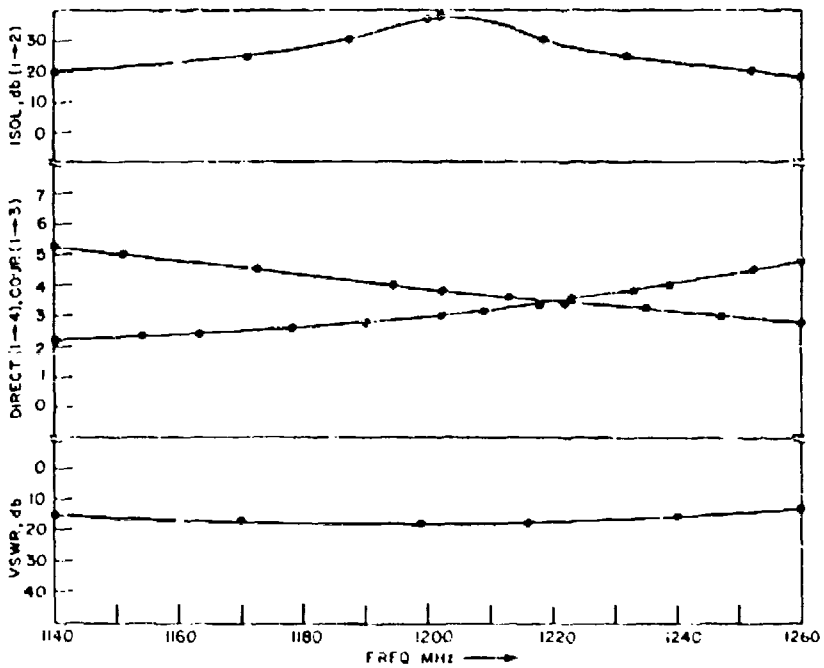

FIG 7 3.8db COUPLER DATA

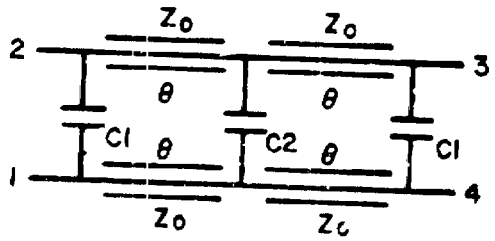

FIG. 8 THREE CAPACITOR COUPLER

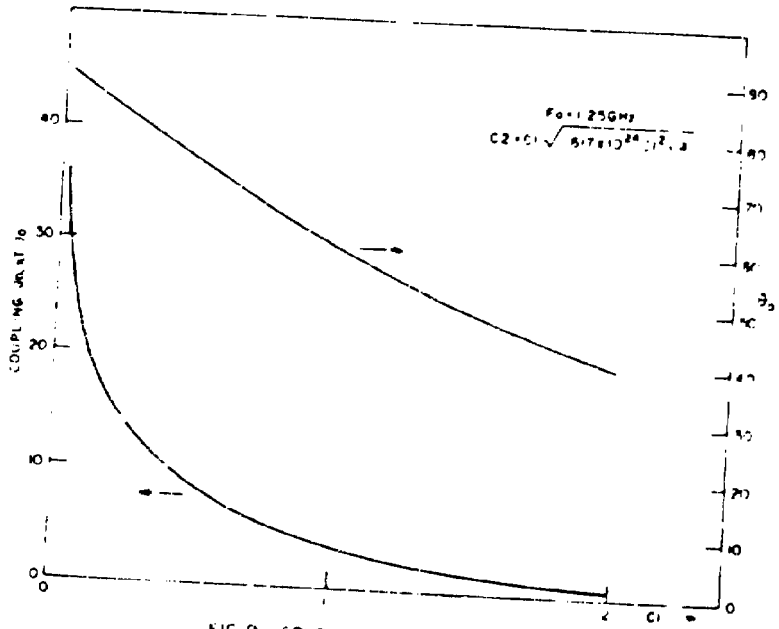

FIG 9 COUPLING WID LINE LENGTH VS C1

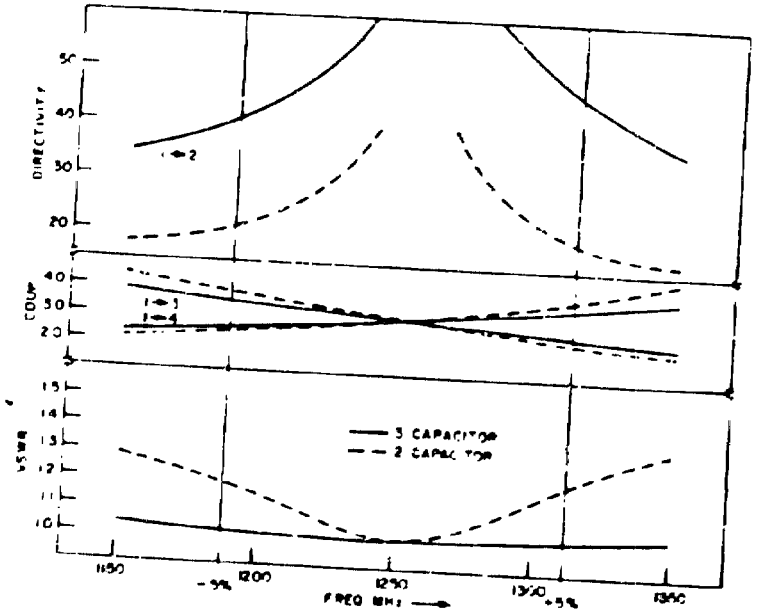

FIG 10 COMPUTED PERFORMANCE

VARIABLE DISPERSION MEANDER-LINE

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ABSTRACT

An S-Band variable dispersion meander line circuit has been developed. The amount of phase dispersion can be continuously varied while maintaining an excellent impedance match over a bandwidth well in excess of an octave. This device has been used to suppress second harmonic power generated in amplifier chains.

INTRODUCTION

This paper describes a variable phase dispersion device for use in suppressing second harmonic power generated in power amplifier chains. Due to its variable dispersion characteristic, this device also has possible application as a variable phase equalizer or as a variable time delay device.

The approach for second harmonic cancellation is illustrated in Figure 1. With the variable phase dispersion device (called "harmonic phase adjuster"), the phase relationship between the first and second harmonics can be controlled. When the phase is adjusted properly, the second harmonic power generated in the output amplifier will be cancelled by the injected second harmonic signal. While, in general, it is necessary to control the amplitude as well as the phase of the injected harmonic to achieve complete cancellation, a reduction of more than 10 dB in the second harmonic content of an output amplifier has been demonstrated by adjusting only the phase of the injected harmonic.

VARIABLE DISPERSION MEANDER-LINE

The meander line circuit considered here is a planar circuit generated by winding the center conductor of a stripline transmission line in a zig-zag pattern. The characteristics of this circuit have been analyzed by several authors.[1-3] Due to its planar nature and simplicity, the meander-line circuit is well suited for variable dispersion applications. Figure 2 illustrates the phase characteristics of the meander-line. As s/D is

decreased from one to zero, the phase characteristics vary from non-dispersive to resonant. Figure 3 shows the configuration developed for varying s/D and hence the dispersion. The structure is composed of two substrates with a meander-line pattern etched on each substrate. The etched patterns are mirror images of each other such that when the substrates are placed together, the patterns exactly match. If the top substrate is moved off center, the spacing between adjacent strips "s" is reduced resulting in tighter coupling and more dispersion. In addition to providing a simple means of varying the dispersion, an important characteristic of this circuit is that the characteristic impedance is a slowly varying function of s/D.

Cromack[1] has shown that the characteristic impedance of the meander-line circuit can be expressed as

$$Z_o(\phi) = \sqrt{Z(\phi)\, Z(\phi + \pi)} \qquad (1)$$

Where $Z(\phi)$ is defined as the characteristic impedance of any tape conductor in a tape array propagating a TEM traveling wave with a phase change of ϕ per tape. $Z(\phi)$ can be expressed in terms of the physical parameters of the meander-line circuit.[1] Consider the case of $\phi = n\, 2\, \pi$, where $n = 0, 1, 2 \ldots$ Then $Z(\phi)$ and $Z(\phi + \pi)$ become the so called even and odd mode impedances respectively and can be expressed in terms of Cohn's[4] fringing capacitances for zero thickness strips. As s/D is reduced $Z(\phi)$ increases and $Z(\phi + \pi)$ decreases while, the product, which determines the characteristic impedance remains approximately constant. This is strictly true only if W is held constant. However, with the configuration shown in Figure 3, the variation in the characteristic impedance can be minimized if the circuit is designed such that $W >> s$. The above argument is also true for an arbitrary value of ϕ.

Figure 4 illustrates Z_o as a function of s/D with D constant rather than W as required by the geometry of Figure 3. The analysis is exact for the idealized model which assumes lossless conductors of zero thickness and corners of zero electrical length. In order to minimize the variation of Z_o, s/D should be less than 0.1.

For a given maximum impedance mismatch, Figure 4 determines the range over which s/D can be varied. The amount of dispersion corresponding to this s/D range can be determined from Cromack's dispersion equation for the meander-line circuit which is:

$$\tan^2 \frac{\theta}{2} = \tan^2 \frac{\phi}{2} \quad \frac{Z(\phi)}{Z(\phi + \pi)} \qquad (2)$$

where $\phi = \beta_o D$

$\theta = ka$

and β_o is the propagation constant of the fundamental space harmonic traveling in the z-direction. k is the propagation constant for the TEM

wave traveling in the x-direction and is given by:

$$k = \frac{\omega}{c} \sqrt{\epsilon_r}$$

and "a" is the length of the coupled section. Therefore, ϕ represents the phase shift per tape and θ represents the electrical length in radians of the coupled section. Note that θ is directly proportional to frequency while ϕ is not.

When employing the meander-line as a harmonic phase adjuster, the quantity of interest is the phase difference introduced between the first and second harmonics. The phase difference $\Delta \phi$, as defined in Figure 1 can be expressed as:

$$\Delta \phi = \delta(2\theta_1) - 2\delta(\theta_1)$$

where $\delta(\theta_1)$ is the phase deviation from linearity at the first harmonic frequency. It can be shown that $\Delta \phi$ is a maximum for θ_1 (the fundamental frequency variable) equal to 60°. $\Delta \phi$ is ploted as a function of s/D in Figure 5 with 2A/D as a parameter and $\theta_1 = 60°$. This figure translates the permissible s/D variation from Figure 4 to $\Delta \phi$ variation.

EXPERIMENTAL RESULTS

A variable dispersion meander-line circuit has been constructed and tested as a harmonic phase adjuster. The design parameters were:

(1) $\Delta \phi$ to be variable over a 180° range from an arbitrary minimum value
(2) $\Delta \phi$ variation over a given frequency range to be a minimum
(3) maximum VSWR = 1.5:1

Condition (3) determines the range over which s/D can be varied. Consider the idealized case of a uniform transmission line of characteristic impedance Z_o terminated in a 50 Ω load and driven by a 50 Ω source. The worst case mismatch occurs when the transmission line is an odd multiple of $\lambda/4$ in length and the magnitude of the VSWR at that frequency is

$$VSWR = \left(\frac{Z_o}{50}\right)^2 \text{ or } \left(\frac{50}{Z_o}\right)^2$$

depending upon whether Z_o is greater or less than 50 Ω. On the basis of this idealized model, the characteristic impedance of the meander-line must be maintained within the range 40.8 Ω to 61.3 Ω in order to satisfy condition (3). Figure 4 translates this impedance variation into permissible s/D variation and Figure 5 relates s/D to $\Delta \phi$. The phase difference $\Delta \phi$ plotted in Figure 5 as a function of s/D is the phase difference per section or per tape. For an n section meander-line circuit, the total $\Delta \phi$ is n $\Delta \phi$. Therefore, knowing the range of s/D and hence $\Delta \phi$ per section, the number of sections n can be determined as required by condition (1).

Figure 6 illustrates the measured values of the phase difference $\Delta \phi$ as a function of the normalized fundamental frequency variable θ_1. The three curves plotted in Figure 6 were obtained with the unit in three different settings. The bottom curve was obtained with the device in the minimum phase difference position, i.e., the top substrate positioned such that the two meander patterns match resulting in minimum dispersion. The theoretical curve for this setting is also shown in the Figure. The experimental $\Delta \phi$ curves do not reach a maximum value at exactly $\theta_1 = 60^\circ$ as theory predicts, but the maximum point shifts toward 60° as s/D is decreased. This effect can be attributed to the finite length of the meander-line corners. The corners capacitively load the coupled section of the meander-line increasing its effective electrical length. By reducing the spacing s, the effective length of the corners is also reduced. This in turn results in less capacitive loading, thereby approximating the zero length corners of the theoretical model.

The insertion loss was less than 1 dB over the frequency range $\theta = 50^\circ$ to 125° (1.5 octaves) for all $\Delta \phi$ settings within the 180 degree interval and the VSWR was less than 1.6:1 over the same interval.

In summary, a variable dispersion meander-line circuit has been developed with the capacity to continuously vary $\Delta \phi$ by more than 180°, while maintaining an impedance match. The theoretical model has been shown to give excellent agreement with the experimental results.

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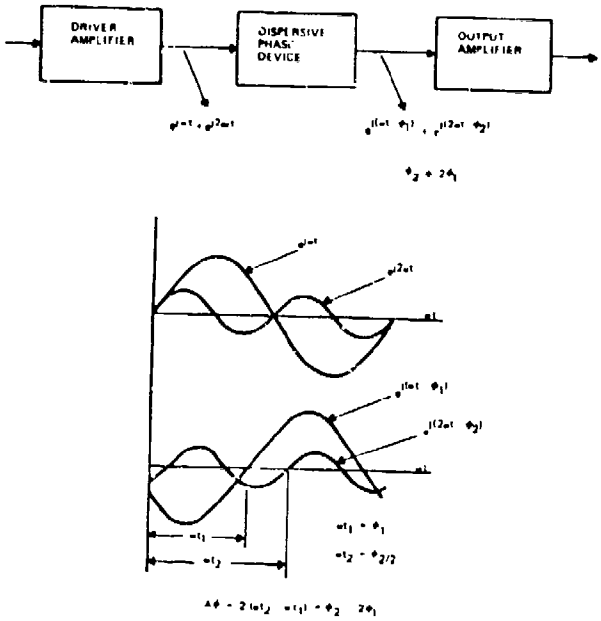

Figure 1: The Dispersive Device Changes the Phase Relationship between the First and Second Harmonics.

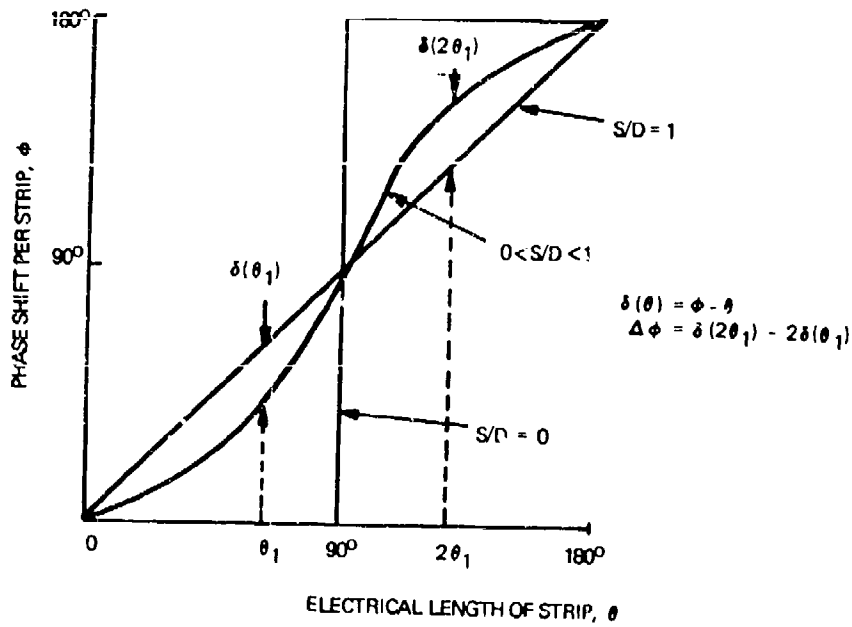

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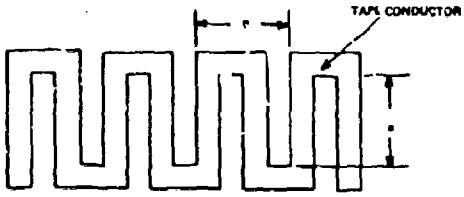
Figure 2: Phase Characteristics of the Meander-Line.



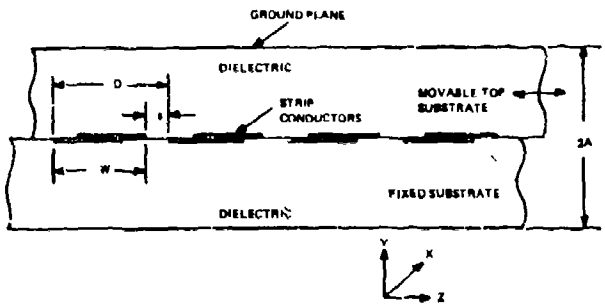


Figure 3: Geometry of Variable Dispersion Meander-Line

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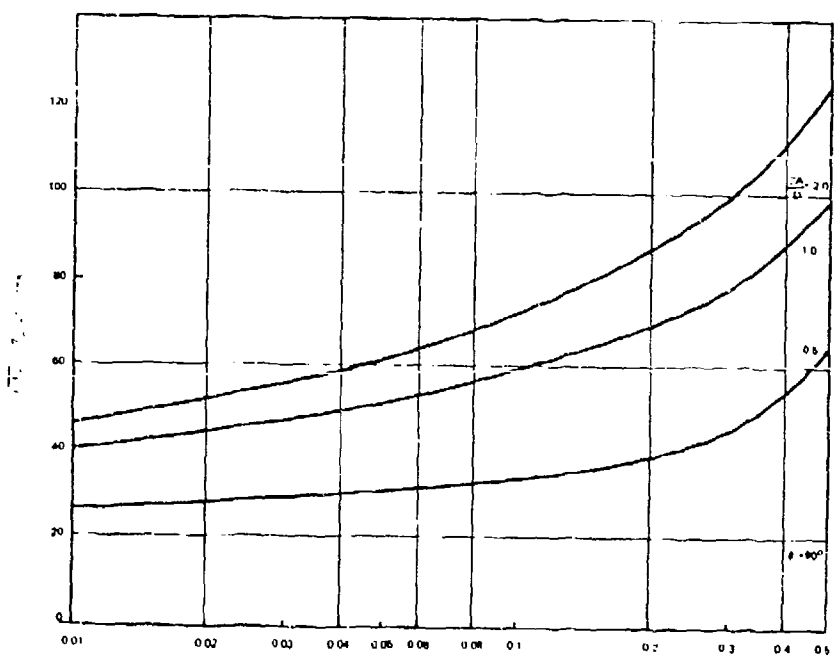
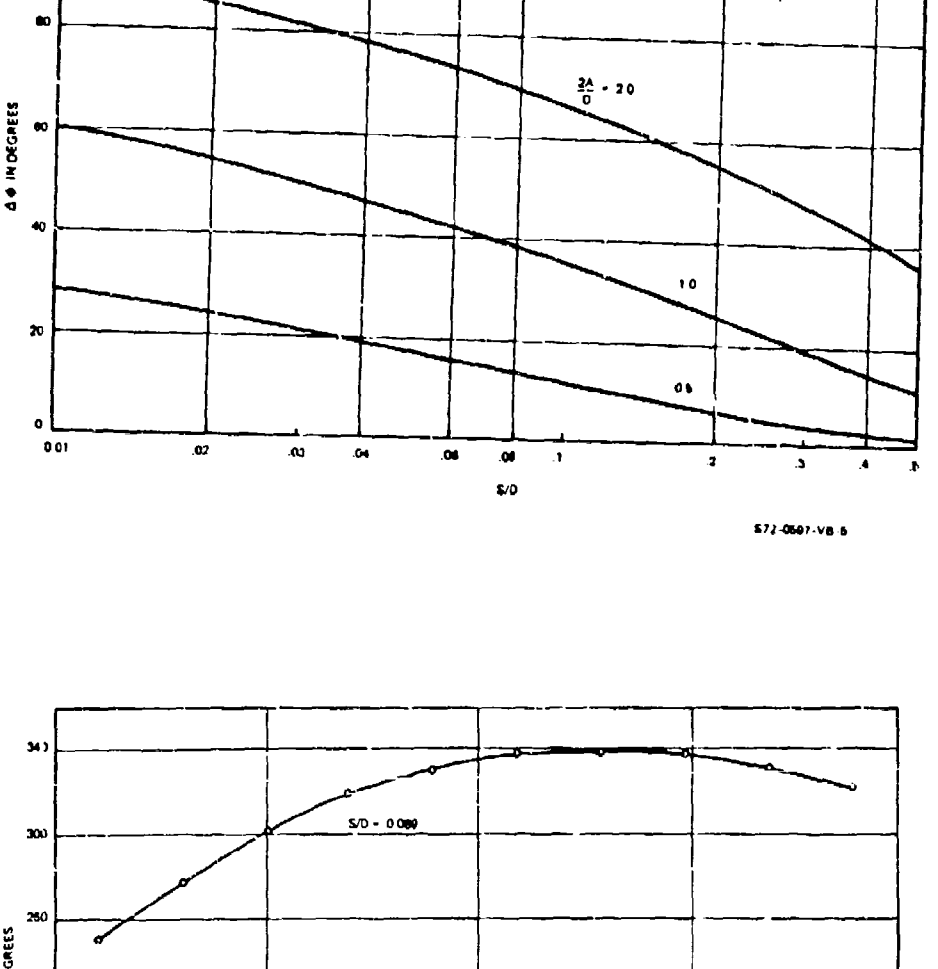


Figure 4: The characteristic impedance as a function of s/D.

572 0687 VB 4

Figure 1 The Phase Differences Δ φ Versus s/D



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LOW-POWER CMOS MASS MEMORY

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Abstract

A mass memory of 10^7 bits can be built that is random access, low power, 1.2 microsecond read or write, low size and weight and that would be suitable for airborne radar data memories and for the replacement of space tape recorders. The technology selected in 1970 for the mass memory was complementary metal oxide silicon (CMOS) because of its availability and low power dissipation. Other technologies evaluated were P channel MOS, N channel MOS, and bipolar, but each was found to dissipate considerably more power. Metal nitride oxide silicon (MNOS), change coupled devices (CCD) and orthoferrites (magnetic bubbles) were considered very promising, but they are in the development stage and unavailable in quantity.

A design of a 3.6 million-bit CMOS random access memory was performed under contract with the Naval Air Development Center (NADC)[1]. The design was proven by building of small portion of the memory [2, 3, 4] 192 words by 32 bits, using bare chip packaging techniques and ceramic substrates. The packaging and substrates incorporate the design approach for the 3.6 million-bit CMOS random access memory. The 192-word by 32-bit CMOS memory was delivered to NADC in June of 1971, and it has been operating satisfactorily since that time.

The 192-word by 32-bit CMOS memory was constructed with the two substrate packages shown in figures 1 and 2. Each package contains 192 words by 16 bits, which includes the necessary address decode and data buffers for the formation of larger memories by wiring several packages together.

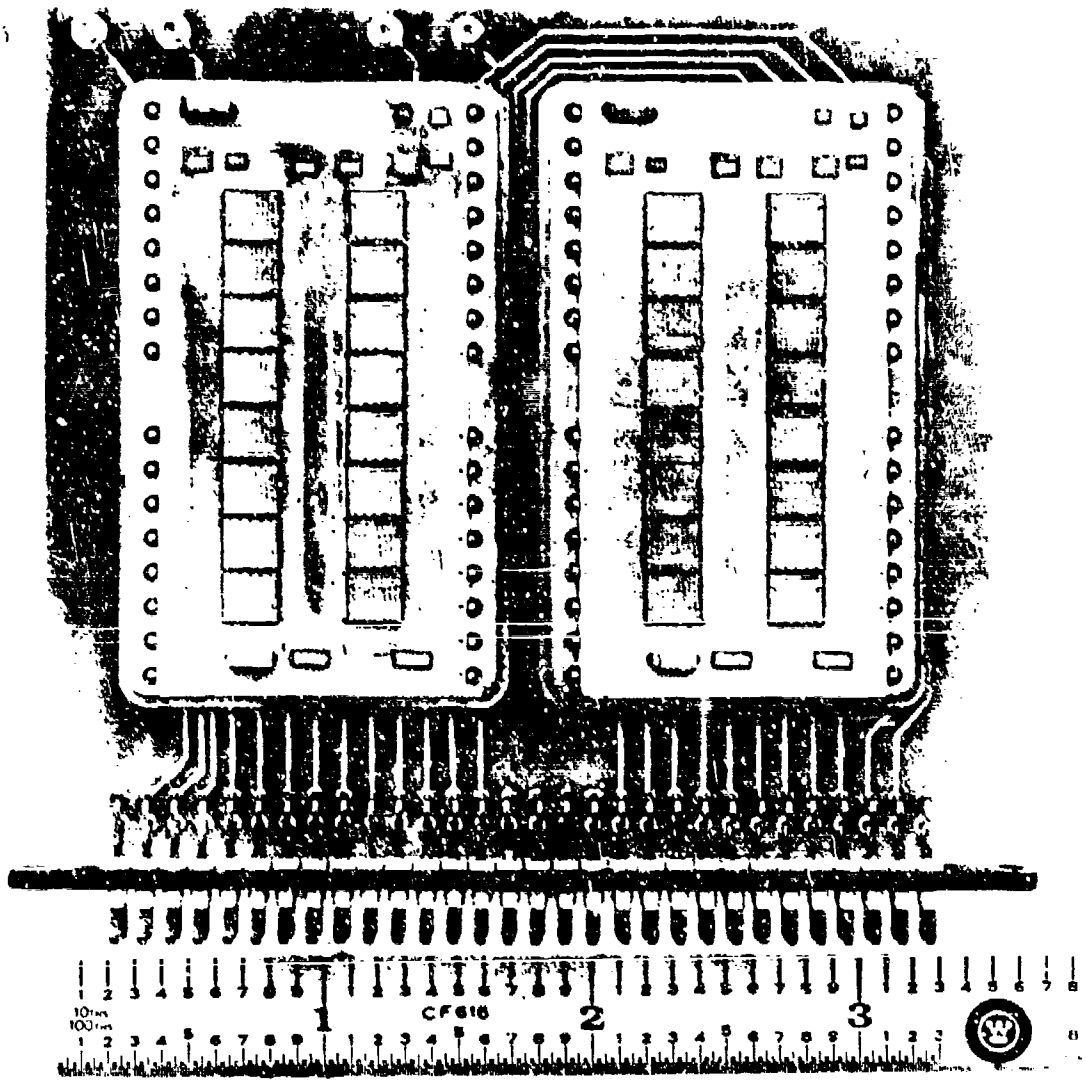

Figure 1. 192-Word by 32-Bit CMOS Memory

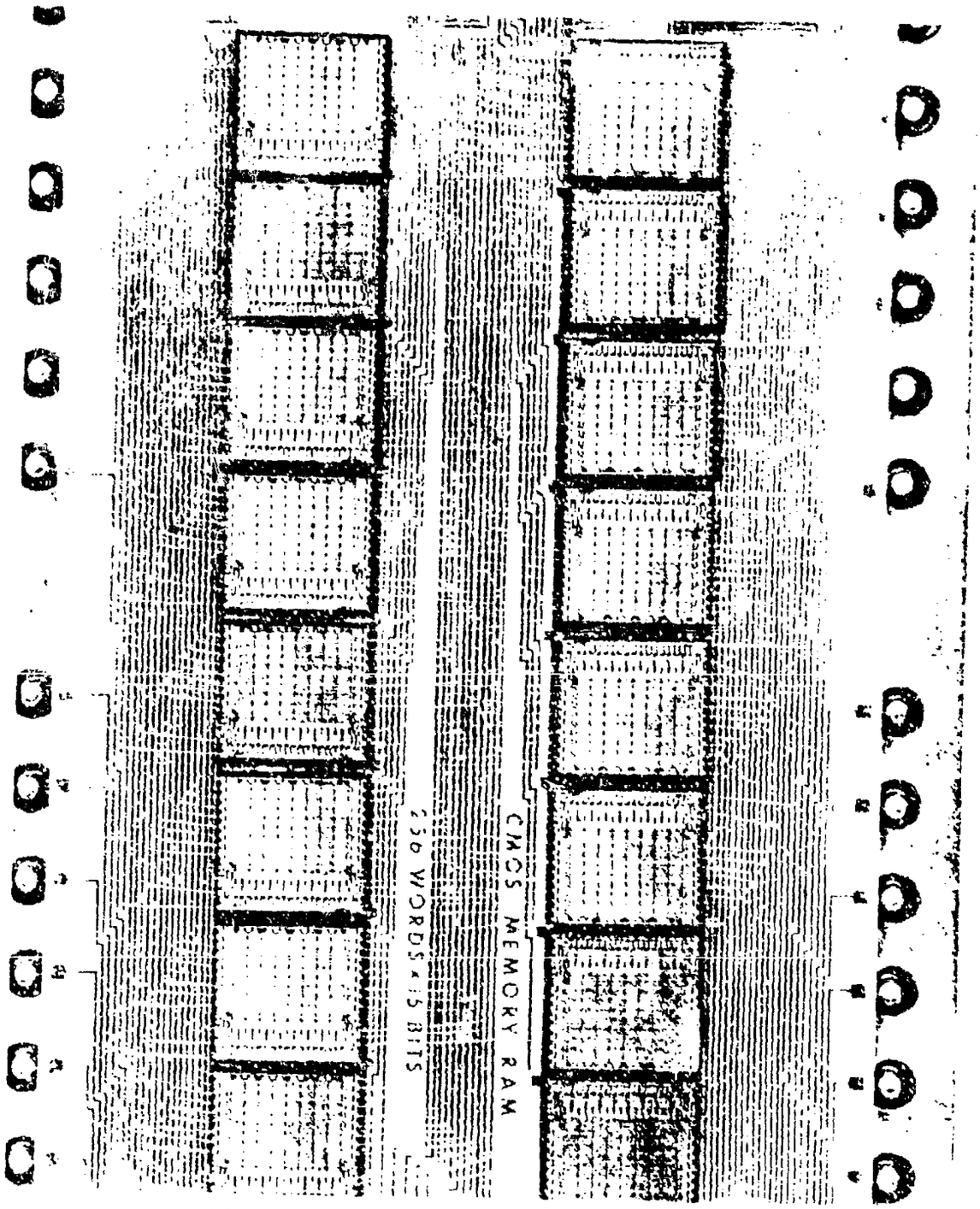

Figure 2. Westinghouse CMOS Memory Chips

Logic Design

The 192-word by 32-bit CMOS memory has 8 address lines (A1 through A8), 1 read/write line (W), 1 memory strobe line (S), 2 power lines (B+, gnd), and 32 data lines (D1 through D32) - a total of 44 interface lines. A logic 1 is at B+ voltage (12.5 V) and a logic 0 is at ground (0 V).

When the memory strobe line is a logic 1, a CMOS memory chip on each substrate will be selected by address lines A5, A6, A7, and A8. The bidirectional CMOS buffer chips (Z21 and Z22) will bring the data from the interface data lines (D1 through D32) to the memory chip for the write operation or will bring the data from the memory chip to the interface data lines for the read operation, depending on the logic level of the read/write line (W). Each CMOS memory chip has 16 words by 16 bits. Twelve chips on each substrate are bussed together, except for chip select signal, to form 192 words by 16 bits as shown in figure 3. Each bit of the 16 bits of data has a bidirectional CMOS buffer driver circuit from either chip Z21 or Z22 to buffer the data between the memory chip and interface data lines to ensure sufficient capacitance drive for speed. Address lines A1, A2, A3, and A4 are bussed to all chips on a substrate after passing through a buffer gate and address one of the 16 words on the chip.

Electrical Design

The electrical design uses all CMOS logic gates. All interfaces between CMOS chips are at CMOS logic levels 0 V or 12.5 V. Westinghouse fabricated the 16-word by 16-bit memory chips and the bidirectional CMOS buffer chips. These circuits were augmented by off-the-shelf one of eight CMOS decode chips (SCL 5206) from Solid State Scientific, hex invertor CMOS gate chips (CD4009) and four 2 input NAND CMOS gate chips (CD4011) from RCA.

The substrate package used to hold the CMOS chips has 32 pins and is 1-3/8 by 2-1/4 inches supplied by Tek Form. The ceramic substrate is 1.05 by 2.00 by 0.030 inches. The substrate is metallized by vapor deposition and plating. The interconnections are made on one side of the substrate with 0.004-inch lines and 0.005-inch spacings. Connections from the chips to the substrate are made by ultrasonically bonding 0.0008-inch gold wires. If two-layer metallization is used on the substrate, all bonding pads would be located close to the chips for easier bonding and shorter gold wires. Each substrate package is filled with dry nitrogen and hermetically sealed.

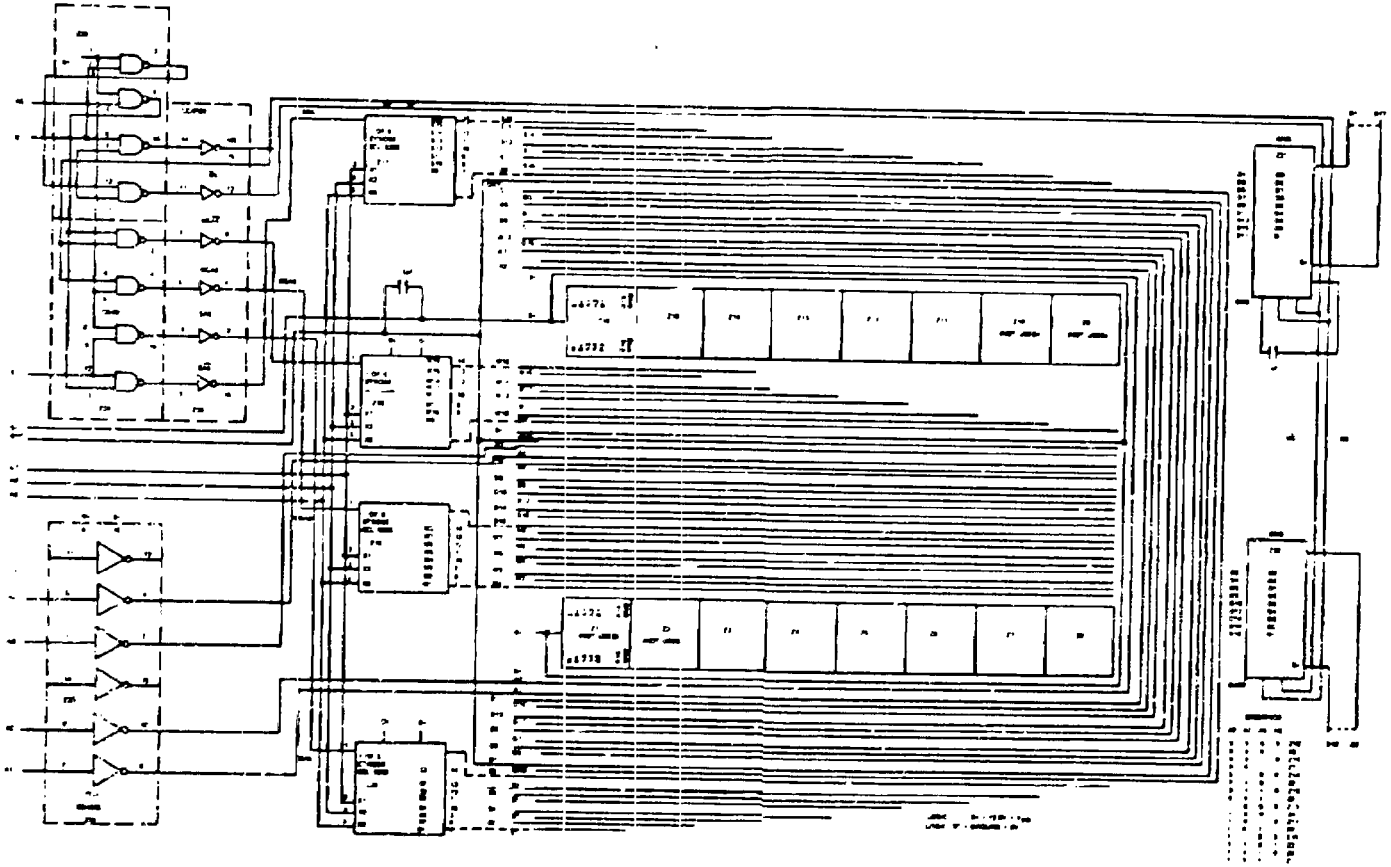

Figure 3. 192-Word by 16-Bit CMOS Memory Logic

Design of a 3.6-Million Bit Random Access CMOS Signal Processor Memory

A 3.6-million bit CMOS memory that will be random access, low power, 1.2-microsecond read or write can be fabricated using the same memory substrate packages delivered on this contract as shown in figure 1. The 3.6-million bit CMOS memory may be organized 204,800 words by 18 bits or 4,096 words by 900 bits. In addition, the memory may be configured into other memory organizations by changing the back panel interconnection wiring.

CMOS Memory Substrate Package (256 words by 18 bits)

If full use is made of the memory substrate package, as described in the previous paragraph, by using 16 memory chips and using 18 bits on the memory chip, then the memory substrate package would be 256 words by 18 bits.

CMOS Memory Section (4,096 Words by 18 Bits)

Sixteen CMOS memory substrate packages, each containing 256 words by 18 bits, may be wire bussed together as shown in figure 4 to form a 4,096-word by 18-bit memory section.

An additional 17th decode and buffer substrate package will be provided to buffer the data through a bidirectional buffer, to buffer the address lines (A1 through A8) and read/write line (W) and to decode package select address lines (A9 through A12) for package select P1 through P16. A memory section select (MSS) control line would be incorporated within the decode and buffer substrate package so that decode and buffering would not take place unless the memory section select (MSS) is a logic one.

Two 4,096-word by 18-bit memory sections may be placed on a printed circuit board 9.75 by 12.75 inches as shown in figure 5.

CMOS Memory Module (32,768 Words by 18 Bits)

Eight 4,096-word by 18-bit memory sections may be wire bussed together as shown in figure 6 to form a 32,768-word by 18-bit (589,824 bits) memory module. The memory section select decode signal will determine which memory section of the eight is addressed. An additional decode and buffer substrate package will be provided to buffer the data through a bidirectional buffer, to buffer address lines

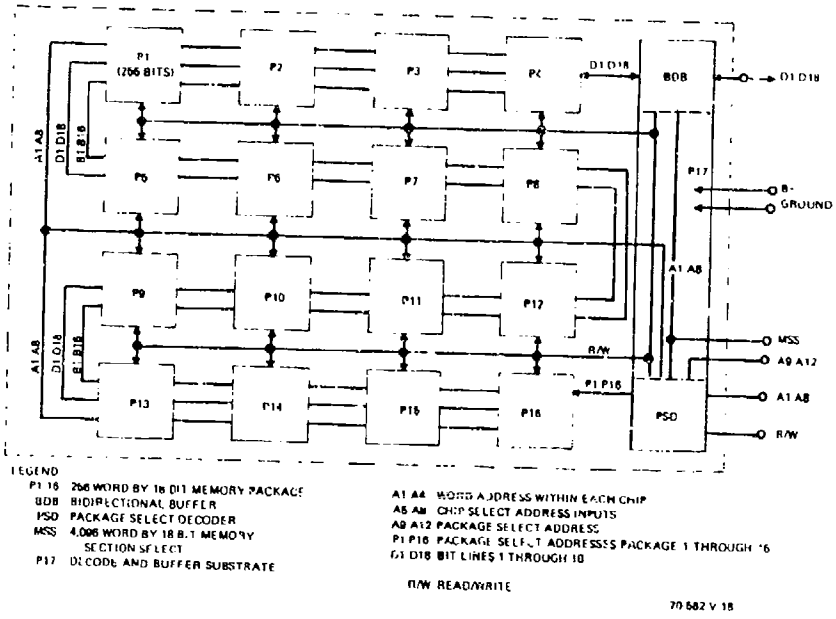

Figure 4. 4,096-Word by 18-Bit Memory Section Composed of 16 Memory Packages

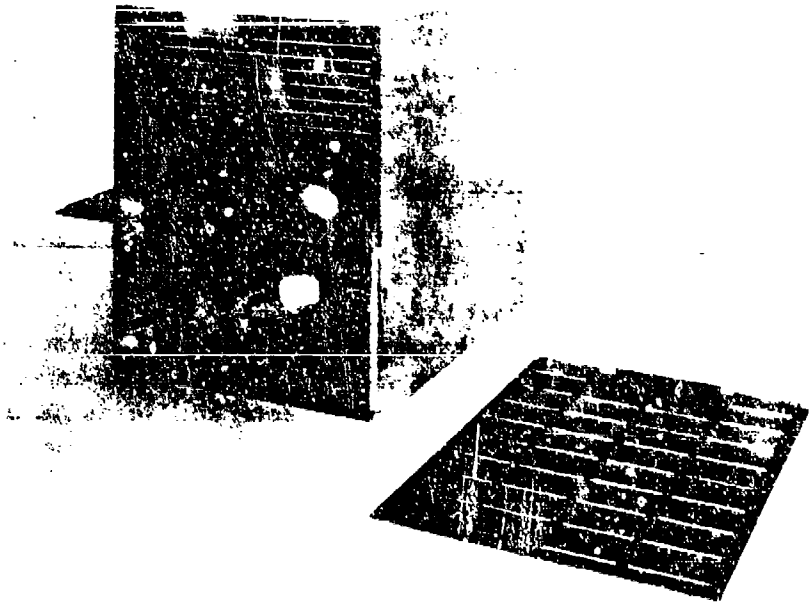

Figure 5. Packaging of 3.6-Million Bit CMOS Memory with Two 4,096-Word by 18-Bit Memory

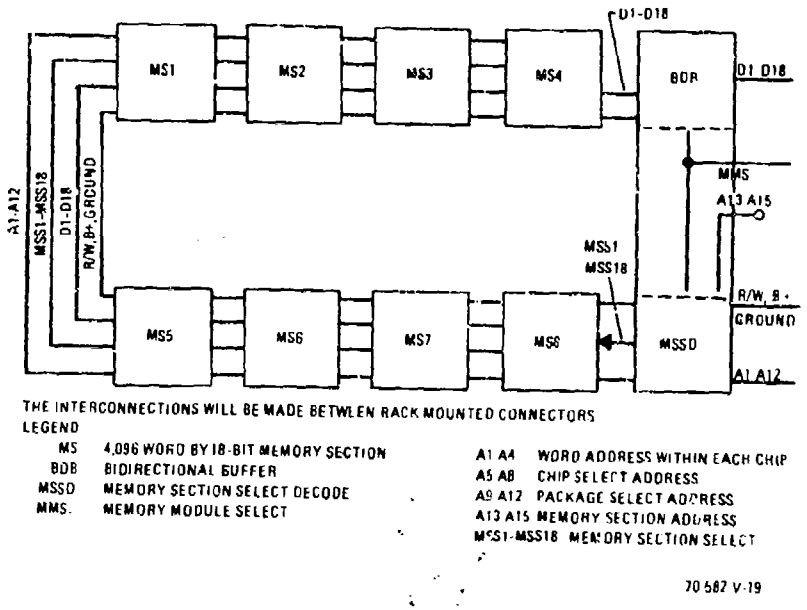

Figure 6. 32,768-Word by 18-Bit Memory Module

A1 through A12 and read/write line (W) and to decode memory section select address lines A13 through A15. A memory module select (MMS) control line would be incorporated within the decode and buffer substrate package so that decode and buffering would not take place unless the memory module select (MMS) is a logic one.

3.6-Million Bit CMOS Memory (204,800 Words by 18 Bits)

Six 32,768-word by 18-bit memory modules and two 4,096-word by 18-bit memory sections may be wire bussed together to form 204,800 words by 18 bits (3.6-million bits) memory. The memory module select decode signal will determine which memory module an/or section is addressed. An additional decode and buffer substrate package will be provided to buffer the data and some address lines A1 through A15, while decoding A16 through A19 for memory module select. A memory module will fit on 4 printed circuit boards; therefore, 6 memory modules and 2 memory sections will fit on 25 printed boards assembled in a card file 10.25(W) by 13.75(D) by 12.75(H) inches as shown in figure 5. The card center-to-center spacing is conservatively set at 0.5 inches and could be reduced. A variation of the present packaging approach is known and proven experimentally that would reduce the volume of the memory packaging

by four. The back panel may be wire wrapped to form various organizations. If a 4,096-word by 900-bit organization is desired, each 4,096-word by 18-bit memory section would be addressed simultaneously, and the data would be presented in parallel.

Weight

Each substrate package weights 37 grams. A printed circuit board as shown in figure 5, 9.75 by 12.75 inches, weights 234 grams. A printed circuit board complete with 34 substrate packages weights 1,492 grams or 3.29 pounds. Twenty-five PC boards as shown in figure 5 weigh 82 pounds. The frame, connectors, and wiring bring the total weight to about 90 pounds.

Timing

The 1.2-microsecond read time is estimated to be apportioned as follows: 350 nsec for address decode and chip select, 400 nsec for chip access time, 450 nsec for the bidirectional drivers. The 0.85 microsecond write time is estimated to be apportioned as follows: 350 nsec for address decode and chip select, 450 nsec for bidirectional drivers running concurrently with address decode, and 400 nsec for chip access time.

Leakage Power

With this CMOS memory design, no refresh cycle is required, and no dc current is used for address or data drivers. If the leakage current associated with one memory cell, 8 devices, is 10 nA, and the supply voltage is 12.5 V, then the power dissipation per memory cell is 0.125 microwatts.

Dynamic Power

The dynamic power dissipation due to a read or write cycle operation is determined by the capacitance that is charged up during each cycle. The power dissipation is calculated by the formula $P = CV^2 f$, where P is expressed in watts, C is expressed in farads, V is expressed in volts, and f is expressed in hertz.

The memory characteristics for the 3.6-million bit mass memory using two memory organizations are summarized on the next page.

a. 204, 800 words by 18 bits

- Access time 1.1 μsec
- Read or write cycle 1.2 μsec
- Power (standby) 0.50 watts
- Power (operating) 0.81 + 0.50 = 1.31 watts
- Size 10.25 by 13.75 by 12.75 inches (1800 in.^{3})
- Weight 90 lb
- Power Supply +12.5 volts
- Environmental -55°C to +125°C

b. 4, 096 words by 900 bits

- Access time 1.1 μsec
- Read or write cycle 1.2 μsec
- Power (standby) 0.50 watts
- Power (operating) 25.3 watts
- Size 10.25 by 13.75 by 12.75 inches (1800 in.^{3})
- Weight 90 lb
- Power Supply +12.5 volts
- Environmental -55°C to +125°C

The results from the reported CMOS memory work show that a mass 10^7 bit CMOS random access memory would be suitable for radar data memories and for the replacement of space tape recorders.

References

1. "Airborne Signal Processor", Naval Air Development Center Contract No. 62269-71-0011, Navy Program Monitor, Jim Davis.

2. "Digital Radar Data Processor", Air Force Avionics Lab, WPAFB, Contract F33615-68-C-1458, Program Director, Capt. D. Mukai and Mr. D. Brewer.

3. "Integrated Circuit Memory Program", Goddard Space Flight Center, NASA, Contract NAS5-10243, Technical Officer, D. H. Schaefer.

4. "CMOS Digital Radar Data Memory", R. M. Trepp, J. R. Cricchi, Government Microcircuit Applications Conference (GOMAC) October, 1970.

A 1280-BIT MNOS RAM

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Abstract

This paper describes the development of a fully decoded 1280-bit random access memory chip utilizing variable threshold MNOS transistors as the storage elements. The voltage polarity requirements led to the development of a unique control circuit. Chip organization, layout and other design considerations are discussed as well. Finally, test results from fabricated circuits are presented.

A 1280-BIT MNOS RAM*

INTRODUCTION

In order to take advantage of the bit densities possible with MNOS variable threshold memory transistors, full decoding and write control must be provided on the chip. A 1280-bit memory chip with a .72 sq. mil/bit single transistor memory cell, full address decoding and write control circuitry has been developed. This paper describes the design, fabrication, and test results of this MNOS memory chip.

In order to have an understanding of the circuit requirements, the properties of the MNOS memory transistor will be discussed. The memory device has the structure of a typical p-channel enhancement mode insulated-gate field-effect transistor (IGFET). By using specially treated silicon nitride as the gate insulating material, charge may be stored in the gate region in such a way that it produces a positive or negative shift in the gate turn-on voltage. These shifts can be retained for a long period of time but are electrically reversible. Once the threshold voltage has been set to a predetermined value, device operation is the same as a fixed threshold insulated gate FET. Information is stored by setting the threshold voltage (V_T) of the IGFET to a high (V_{TH}) or a low (V_{TL}) value. A high (negative) threshold voltage is set by applying a pulse of -30 V between the gate and substrate. The low (V_{TL}) value is obtained by similarly applying a +30 V pulse. Interrogation is accomplished by applying a gate voltage intermediate to the threshold voltage extremes (V_I). Figure 1 shows the idealized drain current vs gate voltage characteristic for the typical memory cell. The V_I gate voltage turns ON the memory transistors that have been set to the V_{TL} threshold level causing a drain current (I_{DL}) to flow. Those memory transistors that have been set to the V_{TH} threshold level remain in the OFF state. The drain current from the ON memory transistors is sensed at the outputs. Figure 2 shows the hysteresis loop of the memory cell.

A decoded MNOS memory chip requires that circuits be provided to control both the positive and the negative voltages needed for setting the desired threshold level in the memory device. In undecoded MNOS chipsthe memory gates are directly accessible and the positive and negative potentials can be applied to the gates from external sources. Since all devices on the decoded chip are p-channel enhancement type, positive (referred to the substrate) voltages cannot be used. The solution to this problem is to provide an isolated substrate region

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for the MNOS memory devices. Then, by applying a negative voltage to the memory substrate and 0 V to the memory gate, the insulator is exposed to the correct positive potential required for setting the threshold to the low (V_{TL}) level. If the memory substrate is held at 0 V and a negative potential is applied to the memory gate, the applied potential across the insulator is such that a high (negative) threshold voltage (V_{TH}) is written into the memory device. The circuit that controls the voltage polarity applied to the memory devices must be controlled by the decoder so that only the selected memory transistors will be exposed to the writing potential. Figure 3 shows the unique approach used to control the polarity of the voltage impressed upon the memory devices. Devices B_D and B_L make up a pair of buffer transistors which function as a source follower or an inverter. This is accomplished by changing the polarity of the voltage applied to the source and drain lines of B_D and B_L under control of an input signal ϕ.

Assume that the ϕ input is low. The common source line of the B_D devices will be at a low level determined by the ϕ driver, and the common drain line of the B_L devices will be high (0 V) due to the inverting action of the $\overline{\phi}$ driver. Device B_D operates as a source follower applying the decoder output level to the gates of the memory devices. The selected decoder output is low and the non-selected output is high (0 V). The inverting action of the substrate driver applies a high (0 V) level to the isolated memory substrate. Thus the selected row of memory devices have a low voltage level applied to their gates and a high (0 V) level on the substrate causing the net voltage across the device to be in the direction that sets a high (negative) threshold. The non-selected rows have 0 V on their gates and 0 V on the substrate.

If the ϕ input is high, the polarity of the common source and drain lines will be reversed and the resistance ratio of the B_D and B_L devices is such that they function as an inverter. In this case the low output of the selected word will be inverted by the buffer and a high (0 V) signal will be present on the memory gates. Unselected rows will have the low level applied to their gates and the memory substrate will be at its low level. Thus the selected row of memory devices will have a high (0 V) level applied to their gates and a low level on the substrate. The net voltage across the memory device is in the direction that sets the threshold to a low level. Non-selected rows have a low level on their gates and a low level on the substrate. The magnitude of the low level applied in either state is determined by the V_{GG} power input. This approach simplifies the hardware needed to satisfy MNOS device voltage requirements to a single polarity power driver (V_{GG}) and a control input ϕ.

The circuit output is designed for current sensing. A single pin on each bit line is used for both input and output. Chip select and voltage level control is determined by the voltage applied to the V_{GG} input. Address inverters are included on the chip and the address inputs accept negative MOS levels. A simplified circuit diagram is shown in Fig. 4.

The chip is organized as 128 words of 10 bits each. Figure 5

shows a block diagram of the circuit organization. Each of the 128 word lines is a common connection of 10 memory device gates. The bit lines consist of a common source and drain diffusion for 128 devices. Figure 6 is a photomicrograph of the 150 mils x 85 mils chip.

The chips are fabricated on a p-type slice with an n-type epilayer. Isolation of the memory substrate is the first step. This is followed by the p-type source and drain diffusions. The fixed gate devices are then deposited, followed by the deposition of the variable MNOS devices. Finally, the aluminum metalization is deposited and the interconnection pattern etched.

A test cycle has been devised which shows the operating states of the circuit as well as the voltages present on the memory control inputs. Referring to Fig. 7, time period 1 shows a Logic 0 (no current) level being read. During time 2 a Logic 1 is written into the same location and read during time 3. Time period 5 shows the bit returned to its original Logic 0 state. Figure 8 is an expanded view of the same sequence with the time periods labeled in terms of read and write memory cycles.

SUMMARY

A 1280-bit fully decoded memory chip has been developed that operates with single polarity input signals. Polarity inversion is performed on the chip by means of a buffer circuit and an isolated memory substrate. The circuit has been fabricated and test results agree with the predicted response.

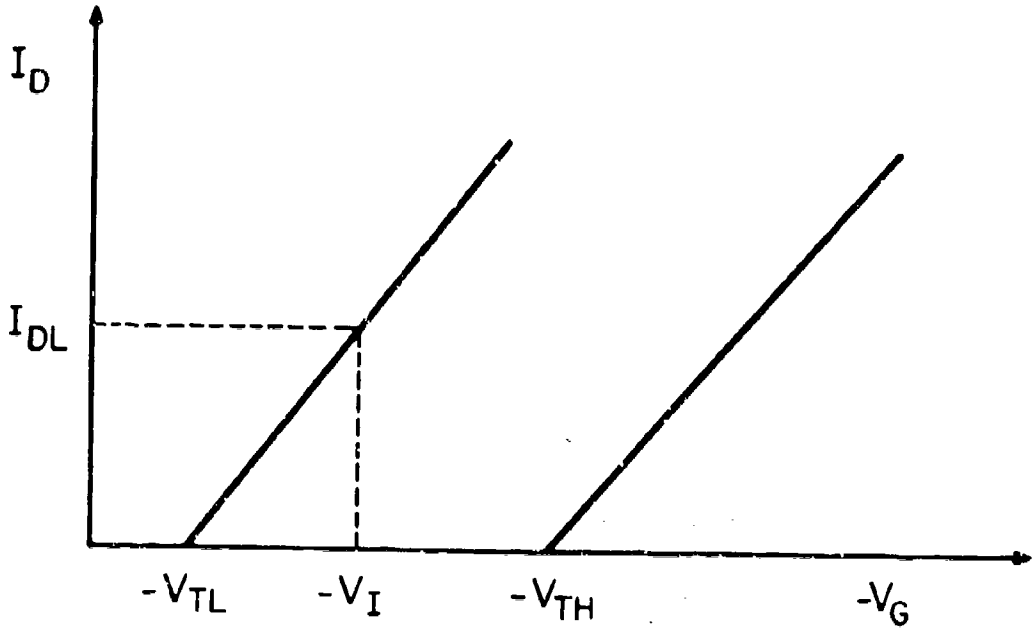


Fig. 1 Idealized Drain Current (I_D) vs Gate Voltage ($-V_G$) Characteristics of Memory Cell.

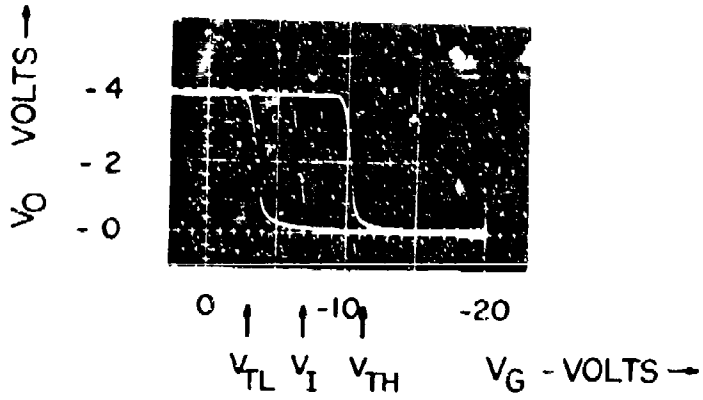


Fig. 2 Memory Transistor Hysteresis Loop

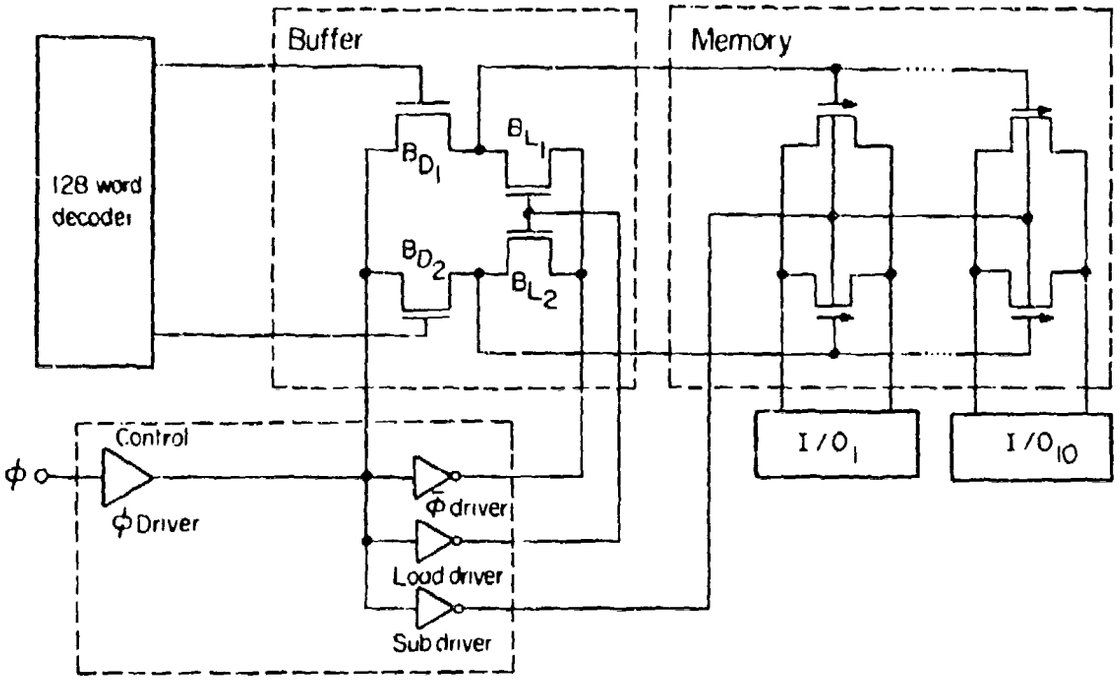


Fig. 3 Buffer Circuit Diagram

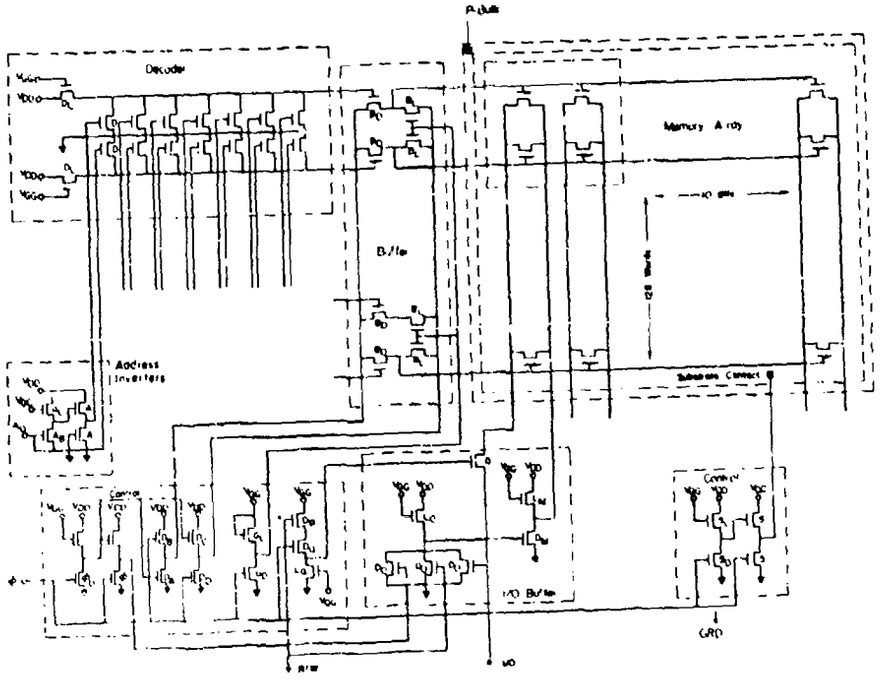


Fig. 4 Simplified Circuit Diagram of 1280-Bit Circuit

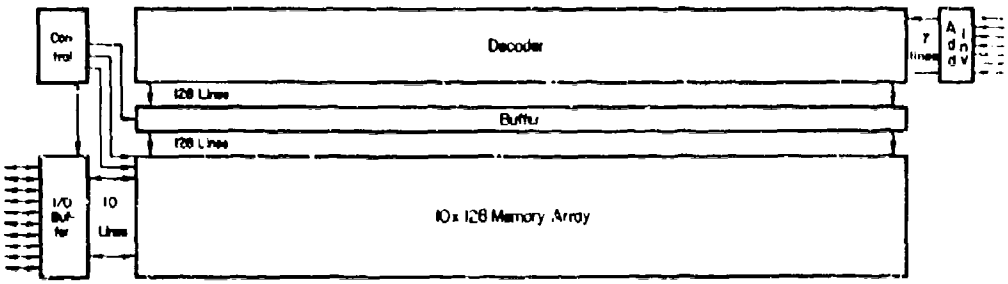


Fig. 5 Organization of 1280-Bit Circuit

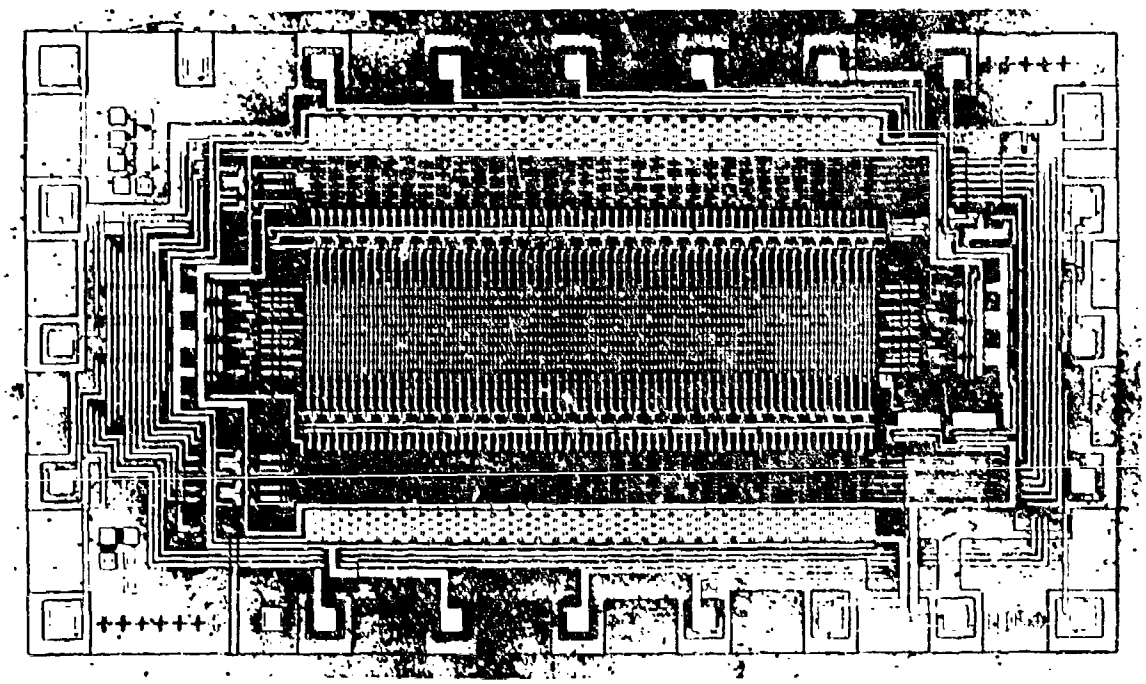
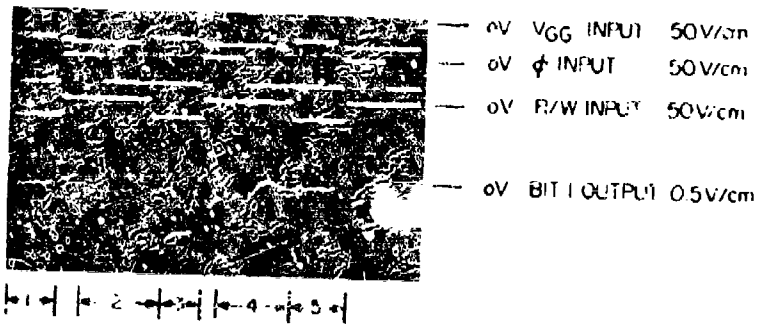


Fig. 6 Photomicrograph of 1280-Bit Circuit

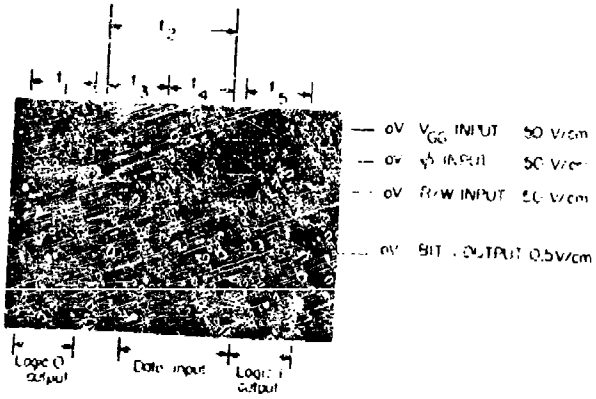


1 - Logic 0 output
2 - Data input -20V (logic 1)
3 - Logic 1 output
4 - Data input 0V (logic 0)
5 - Logic 0 output

Time scale = 5 μs/cm

V_{DD} = -35V

Fig. 7 1280 Read/Write Operation



t_1 — Read cycle
t_2 — Write cycle
t_3 — Clear time
t_4 — Write time
t_5 — Read cycle

TIME SCALE = 2.5 μs/cm

V_{DD} = -35 V

Fig. 8 1280 Read/Write Timing

BUBBLE MEMORY STATUS AND TRENDS IN U.S. GOVERNMENT DATA STORAGE APPLICATIONS

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ABSTRACT

The usage of bubble memories in the various data storage missions of the sponsoring agencies will be discussed from the standpoint of the present status of U.S. Government/NRDC contracts. Projections of availability that can be used to plan future programs are presented.

INTRODUCTION

The U.S. Government interest in bubble domain technology is being well demonstrated by the support that military and civilian agencies are providing to contractors in the areas of materials research, devices, manufacturing technology, systems planning and systems development. The resultant from this investment will be a wide range of memory products that will be capable of operating under diverse environmental conditions to provide a common solution to the many different data storage missions of the U.S. Government. These memory missions run the gamut from the high environmental performance required of satellite systems to economically competitive billion bit mass memories operating in ground based computer systems. In between, strategic data storage missions in aircraft, the mobile army, and surface and submerged naval vessels will be successfully accomplished.

BUBBLE MEMORY CAPABILITIES

The technical capabilities of a bubble memory that allows this new storage media to be adapted to so many different applications are shown in Table 1. Over and above the straightforward technical advantages of NDRO, non-volatility, and no mechanical inertia - the most exciting technical enhancements are the properties of asynchronous, multi-speed operation. No longer must the parent equipment be slaved to the peripherals. With the facility to operate the memory at any speed up to the design maximum and then to be able to stop, hold, or even reverse the direction of data flow, the system designer/user can enhance his throughput and efficiency. While we use the term "average access time" to make comparisons, the ability of bubble memories to stop a data flow and wait for a new start command makes this term

obsolete in many applications. Significant latency times are applicable only when a large address jump is required by the program. The "average access time" is reduced by half when data propagation in two directions is implemented. As the function of Reading & Writing are accomplished by different patterns in the device they operate independently. A Read-Modify-Write can be accomplished on the same data pass through the control elements. By the proper placement of the elements of the detector bridge a check operation can be performed within several bit times of the modify operation.

Table 1

Capability of a Bubble Memory

Asynchronous Operation (forward, stop, reverse)

100 fold improvement in access time (100μS ← 10 mS)

Read/Modify/Write/Check "on the fly"

Passive construction (no diffusion, no semiconductor junctions)

Non-Destructive Readout

Non-Volatile Storage

No Mechanical Inertia

BUBBLE MEMORY MISSIONS

A representative sample of potential bubble memory missions is shown in Table 2. They differ in capacity, data rate, and access time. Environmental design and packaging will be unique for most applications. Satellite usage has a prime consideration for power dissipation; mobile (land, air or sea) usage has temperature range as a prime consideration; and permanent installation tend to optimize data throughput.

Table 2

Typical Bubble Memory Applications

APPLICATIONS	CAPACITY	BIT RATE
Drum Replacement TV Refresh	$7x10^6$ B	$9x10^5$ Bd
Digital Recording	10^8 B	10^8 Bd
Satellite Tape Recorder	$4x10^7$ B	10^4 Bd
Satellite - Radar Data Memory	10^7 B	10^5 Bd
Gnd Base Data Storage 0.15 mS access time	$2x10^7$ B	10^7 Bd
Bulk Memory 1.0 mS access time	10^9 B	10^7 Bd

B = bits; Bd - Baud = bit/sec

Table 3 shows how bubble systems compare against the performance criteria of disks and drums. Given equal capacity and mission, the bubble memory outperforms the competing technology each time. Similar comparisons can be made holding other parameters constant. For example, if data rates are constant, a tape recorder replacement for a collect-store-forward application can make use of the multi-speed capability, and in addition more bits/pound can be provided. In a satellite this can mean an expanded mission or a lighter memory.

Table 3

Rotating Memories Vs Bubble Memories

CHARACTERISTICS	FIXED HEAD ROTATING MEMORIES	BUBBLE MEMORY
Access Time (mS)	2.5 - 16.0	0.150
Transfer Rates (MBd)	2 - 4 (Fixed)	2 (Variable)
Synchronization with Parent Equipment	No	Yes
Write partial block	No	Yes
Size Range	Uneconomical Below 2 MBits	Economical in Smaller Sizes

NR BUBBLE PROGRAM STATUS

At North American Rockwell we are pleased to be working with several agencies in developing and proving the bubble technology. Table 4 shows a comparison of three different bubble films developed with the support of the agencies listed. The attributes and detriments to the usage of each of the films is listed. The Ga:Y,GdIG film on G^3 via CVD is continuing to be perfected under NASA-LRC sponsorship. In addition company funded investigations into LPE technologies are also underway. These CVD and LPE films will be evaluated in our AFML Manufacturing Methods contract to determine an optimum film for production, design the methods of production, and offer it to device experimenters and systems designers. Devices were constructed using Ga:ErIG on a mixed $(GdDy)G^c$ substrate which was developed to allow a wider range of film composition to be investigated. A physical model for stress induced anisotropy was developed. Work under AFML sponsorship is continuing to investigate radiation hardness, wall mobility and velocity improvement, temperature coefficient improvements and resistance to shock and vibration of the bubble materials. Work for the USAECOM is now active in the device area studying high speed propagation.

Table 4

A Comparison of Bubble Garnet Films

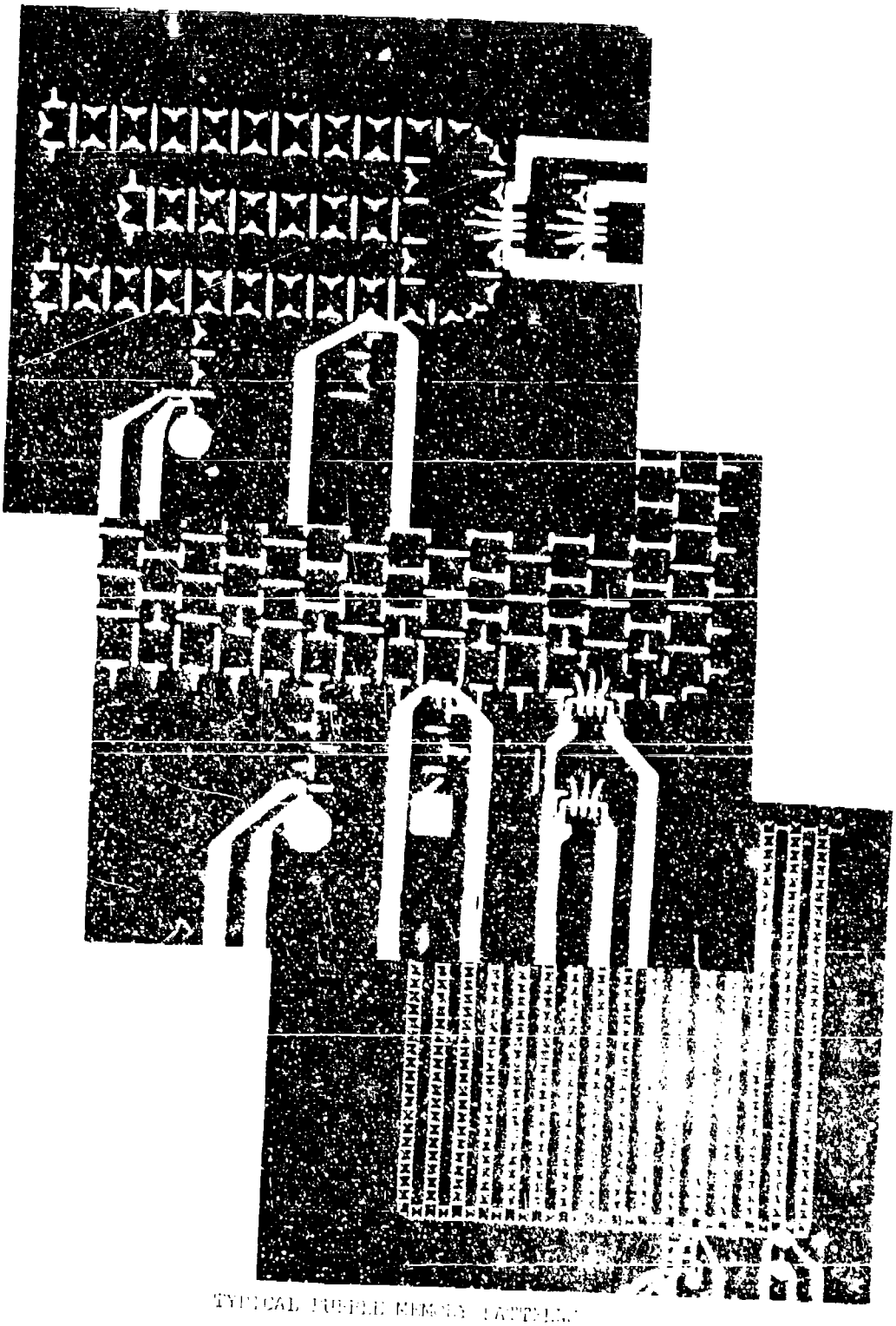
PARAMETERS	Ga YIG	GaErIG	GaYGdIG
Thickness	6.8μm	4.0μm	3.4μm
Bubble Diameter	4.0μm	6.0μm	6.0μm
Nominal Field	44 oe	72 oe	32 oe
Magnetication	90 gauss	175 gauss	160 gauss
Characterization Length	0.7μm	0.9μm	1.3μm
Wall Energy	0.04 ergs/cm^2	0.2 ergs/cm^2	0.26 ergs/cm^2
Anisotropy Field	600-700 oe	660 oe	420 oe
Temperature Coefficient	-0.074 percent/C°	+3.7 percent/C°	+1.6 percent/C°
Wall Mobility	3000 cm $sec^{-1}oe^{-1}$	200 cm $sec^{-1}oe^{-1}$	1300 cm $sec^{-1}oe^{-1}$
Wall Coercivity	<0.2 oe	<0.2 oe	~0.2 oe
Attributes	Best Temp. Coef. bit density, and mobility	Easiest to produce	High Speed, Good Magnetization
Deficiency	Require Highest degree of photo-lithographic technique and detector sensitivity	Low speed, Poor Temp. coefficient	Most Difficult to Produce
Supporting Agency	U.S. Army, Ft. Monmouth	U.S. Air Force, WPAFB	NASA-Langley

Device studies are now underway, sponsored by the AFAL, to optimize the performance of bubble devices under system usage conditions. Some of the patterns that have been utilized are shown in Fig. 1. We have developed devices that operate from external exercisers in all modes. A significant finding in the understanding of bubble control has resulted from our studies. When attempting to explain or design bubble patterns the field created by the bubble itself must be considered in addition to the fields created by the propagation field interaction with the permalloy pattern. A model was formulated which has been proved both theoretically and experimentally. The progress to date fully supports the projections used by our memory system design staff in planning for the introduction of bubble memories into the various U.S. Government agency missions. We are no longer satisfied with just operating bubble devices. By using the model and intensive laboratory experimentation the effort now is to maximize and make congruent the margin of operation of the basic device elements - propagation structure, generator, detector, annihilator, and switches at ever increasing data rates.

BUBBLE FUTURES

The time is now appropriate to enter areas of investigation unique to the requirements for governmental missions. For example, two areas ready for investigation are temperature range and module size. It is desirable to have the bubble maintain a constant diameter over as wide a temperature range as possible. Even as the basic materials are developed to minimize the effect of temperature, a combination of temperature varient magnets and shunts for the bias field will be required to ensure operation over the wide environments found in tactical missions. An effort to develop the basic materials required is appropriate. The volume of controlled flux that the propagation coils create can be traded against power and drive voltages. In aerospace usage, a small modular building block that requires lower voltages (BVCEO) and total power, and which then could be driven in a matrix, may be more useful than one large power-consuming module.

The present state of our development programs indicates that scheduled progress has been attained and program goals are being met. An internal study at NREG indicates that, for aerospace programs, memory requirements will continue to grow logarithmically with linear time. We expect that trend to hold true for non-aerospace applications as well. Figure 2 shows this growth for both replacement functions and added functions in new equipments. The cross-hatched ray shows the present and projected development of bubble memories to overtake and exceed these program needs by the mid 70's. Bubble memory technology and development has progressed to the point where introduction of memory hardware into defined programs can be scheduled. With your continued support bubble memories will be available when they are needed. It is now appropriate for system designers in all agencies to categorize and specify their data storage needs so that feasibility can be proved and detailed equipment designs can be begun.



TYPICAL BUBBLE MEMORY CARTRIDGE
Figure 1

PROJECTED GROWTH IN TOTAL MEMORY CAPACITY
REQUIREMENTS FOR AEROSPACE APPLICATIONS
(EXCLUDING REDUNDANCY)
1960 - 1990

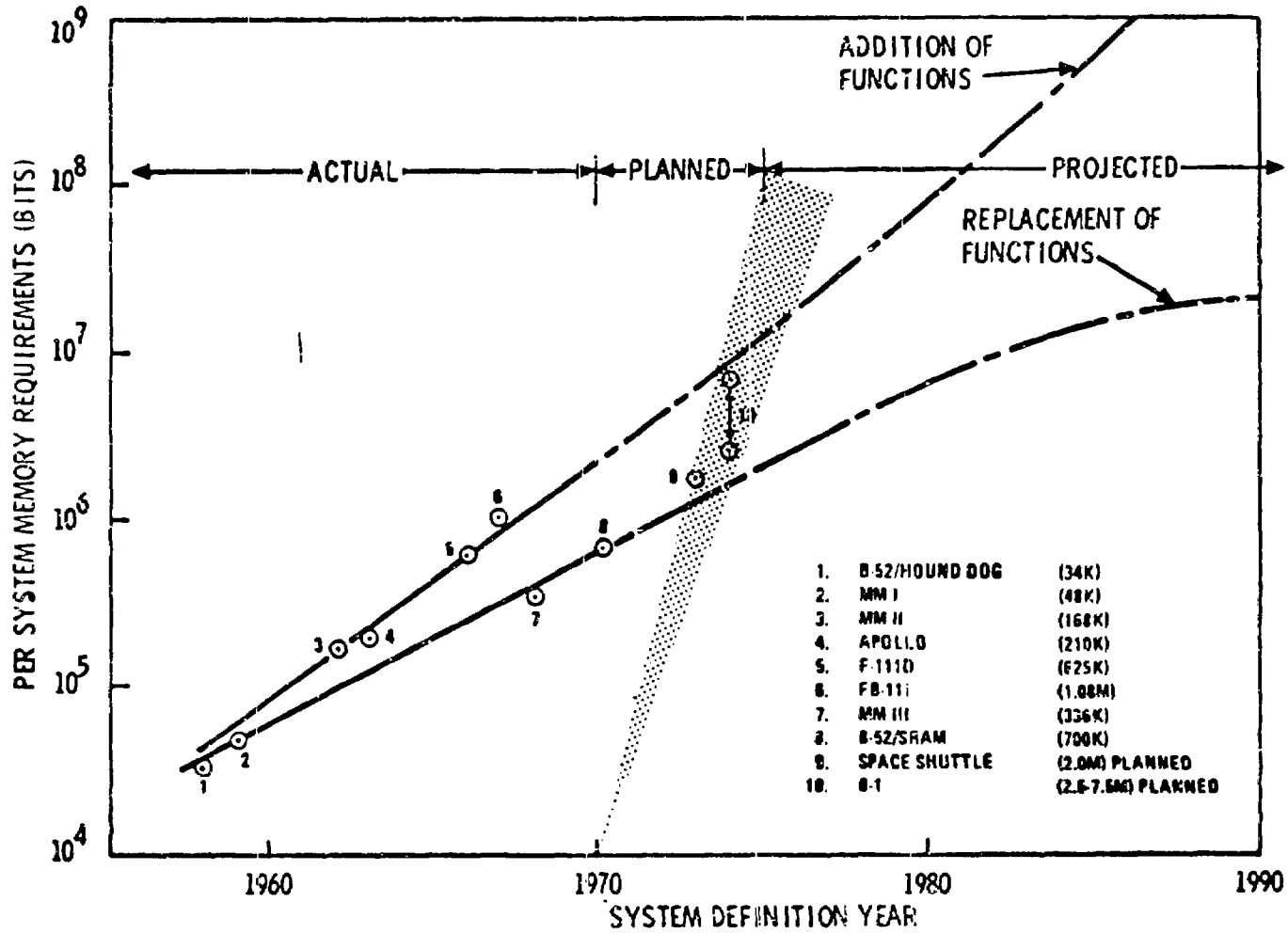


Figure 2

AN LSI MEMORY SYSTEM FOR MILITARY MAINFRAME APPLICATIONS

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Abstract

A random access memory system utilizing 1024 bit dynamic MOS devices has been developed. The system described is nonvolatile, organized 8K words by 33 bits, and meets the requirements of an existing military system.

INTRODUCTION

Semiconductor memories offer numerous advantages as a replacement for core memories in future military systems. Lower cost, improved performance, higher reliability, and greater maintainability are just a few of the potential advantages of a random access memory system utilizing Large Scale Integration (LSI) devices. Studies conducted on the developments in the semiconductor industry have indicated that existing random access memory devices are feasible both technically and economically for use in military mainframe applications. A militarized 8,192 word by 33 bit semiconductor memory system has been developed and evaluated. The system uses MOS (Metal-Oxide-Semiconductor) devices for data storage, and is functionally equivalent to an existing core memory module. The feasibility of such a system has been proven by successful performance in laboratory evaluation and six months of continuous usage in a militarized computer system.

The computer system used for evaluation is a military command and control data processing system produced by Litton Data Systems for the U. S. Army. Its requirements are typical of ground based transportable equipment. The system's basic memory module is an 8K word by 33 bit core memory having an access time of 700 nsec and a cycle time of 2 usec. The entire system is cooled by forced air, and will operate over a temperature range of -30°C to +55°C.

The introduction of 1024 bit memory devices during the past two years made possible the development of a cost effective memory system which could replace the core system. The basic design requirements established for the LSI Memory for use in this system include:

1. Memory device selected must have multiple sources.

2. Exceed performance parameters of the existing core memory system.

3. Memory system nonvolatility.

The latter item has been a primary argument against the use of semiconductor memories as mainframe storage. For most system applications protection is necessary only for power transients of short duration. In real time applications when prime power is lost, the stored data is invalid after a specific period of time. After power is restored, it is necessary to update the information stored in memory. Important programs and data are normally stored on tape, drum, or disc and reloaded whenever prime power is cycled. Therefore, nonvolatility for a long period of time is not necessary for the high speed mainframe memories. The developed system is provided with a battery to allow data to be retained when prime power is interrupted. A one hour minimum nonvolatility requirement was established for the program.

The MOSTEK 4006 device was selected as the storage element for the system after a careful analysis of available devices. The study included the evaluation of the specific technologies, laboratory testing of devices, and a system's cost vs. performance study. Bipolar and Static MOS devices were eliminated early in the investigation because they are not cost effective for most mainframe system application. The MOSTEK device is a 1024 bit dynamic P channel MOS device utilizing Ion Implantation processing. Table 1 contains a summary of the device's characteristics.

SYSTEM DESCRIPTION

The MOS memory is divided into four functional areas which consist of the Port Logic, Timing and Control, Memory Array and Power System. This is illustrated in Figure 1.

The Port Logic provides the interface between the Memory Array and the processing units accessing the memory. This interface is designed to handle requests from up to four processors. Priority is resolved by the Port Logic for simultaneous requests, and data is channeled to or from the selected processor.

The Timing and Control card accepts memory cycle requests from the Port Logic, and provides the required timing signals for all memory operations. Since the storage elements are dynamic MOS devices, the stored data must be periodically refreshed. A low frequency temperature varying oscillator is provided on the Timing card to periodically request Refresh cycles. At lower temperatures the memory devices require less frequent refreshing, and the oscillator frequency is automatically reduced. Logic on the card resolves priority between normal memory and Refresh cycle requests and initiates the proper timing.

The Memory Array consists of the entire 8K word by 33 bits of storage and is contained on eleven circuit cards. Each card is organized 8192 words by 3 bits, and contains 24 memory chips, address buffers, sense circuits, a data register, and a power switch. The power switch greatly reduces system power by reducing the voltage across the memory devices not being accessed. The Memory Array card is shown in Figure 2.

As indicated in Table 1, the MOSTEK 4006 operates on +5 and -12 volts, and has a basic access/cycle time of 400/650 nsec. Figure 3 indicates how the device is organized. The chip consists of an array of 1024 memory cells organized into 32 rows by 32 columns. To access a particular location, 5 binary address bits are decoded to select a particular row of 32 memory cells and 5 additional bits are used to select one cell of the 32.

A basic memory cell is a 3 MOS transistor circuit configured as shown in Figure 4. Information is stored as charge on the gate capacitance of transistor Q1. Because the gate is not a perfect capacitor, charge is continually leaking off, and it is necessary to periodically replace this charge or Refresh the cell. This is accomplished by first reading the data from the cell onto the Read Bus, and into a Refresh Amplifier which restores the data on the Write Bus. Data is restored to the gate of Q1 by enabling Q3. Each device contains 32 Refresh Amplifiers, one per column, and 32 locations are refreshed simultaneously. The entire array is refreshed by cycling through the 32 row addresses and performing a Write cycle or Refresh cycle at each address. A Refresh cycle consists of a Write cycle with the chip's input/output circuitry disabled to prevent the writing of erroneous data.

The Power System provides the necessary power for the memory. It receives input power from two sources, a primary source of 270VDC and a secondary (battery) source of 24 volts. The primary source provides power necessary for normal memory operation. If prime power is lost, the secondary power source provides the power necessary to retain previously stored data until primary power can be restored. During the data retention mode of operation, power is applied to only those circuits required to retain information. The LSI Memory is shown in Figure 5, and Table 2 lists the basic characteristics of the system.

SUMMARY

The feasibility of MOS memory devices for military mainframe application has been demonstrated by the development and evaluation of a militarized memory system. The unit has been successfully tested over the temperature range of -30°C to +70°C, and used in multiport modes of operation.

The improved performance and maintainability of the LSI Memory make it a desirable replacement for the existing core system. The faster access and cycle times provide increased processor throughput, and the modular design simplifies fault isolation. Maintenance costs are reduced because of improved reliability, simplified fault isolation, and the lack of expensive spare items (i.e. corestacks).

The results of the LSI Memory program have been very encouraging. Careful evaluation of both device characteristics and system requirements is extremely important when selecting components for a particular application. The devices can be operated over an extended temperature range without affecting their reliability. Semiconductor memory devices offer too many advantages to be ignored because of the label "limited temperature range", and should be given careful consideration for use in future command and control data processing systems.

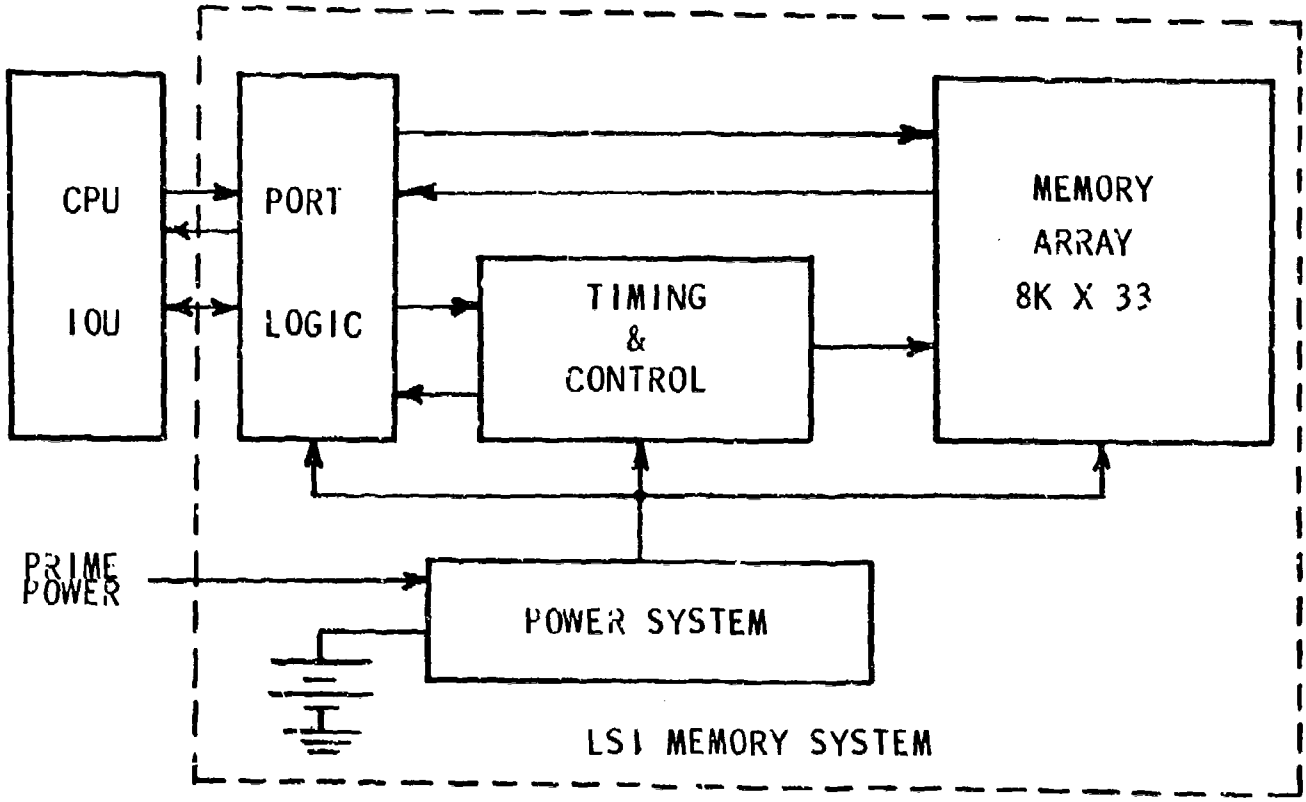


Figure 1. Block Diagram of LSI Memory System

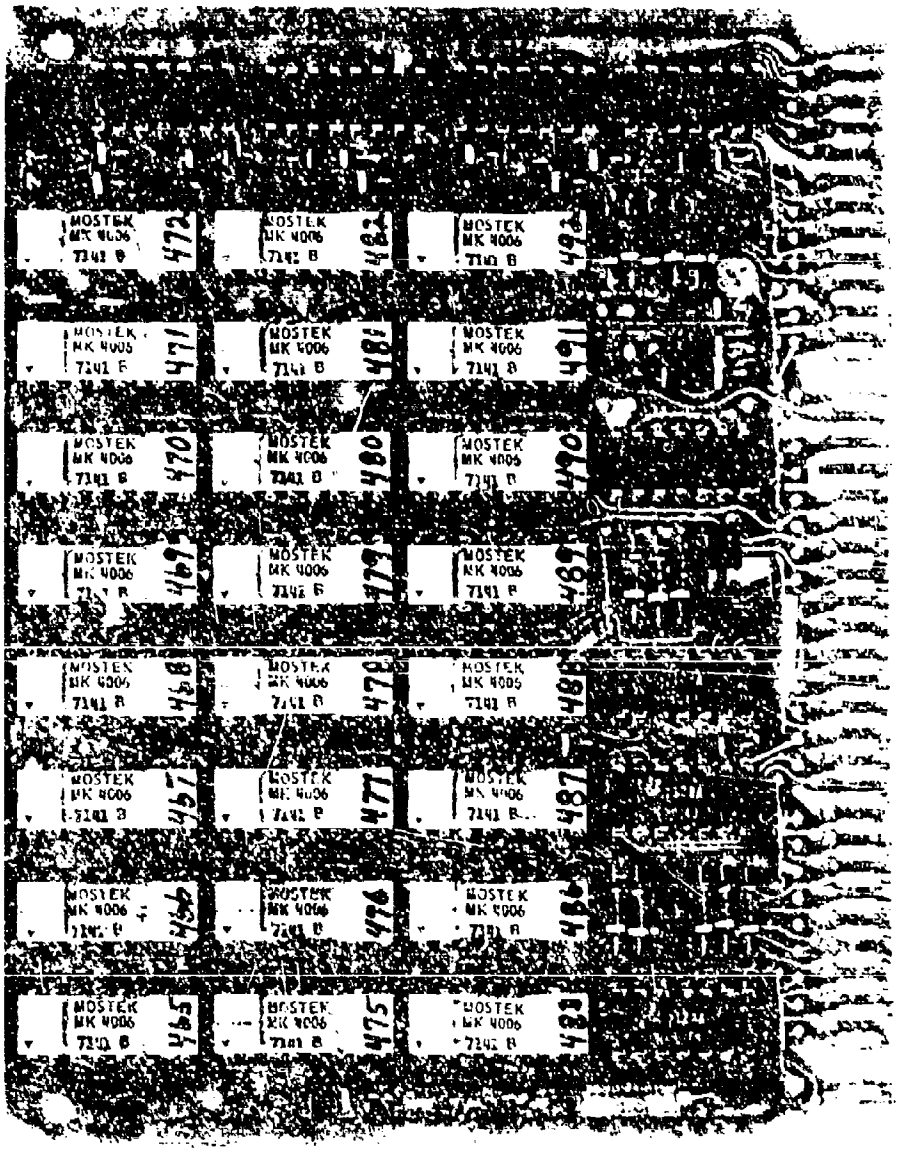


Figure 2. Memory Array Card

Figure 3. MOS Random Access Memory Device

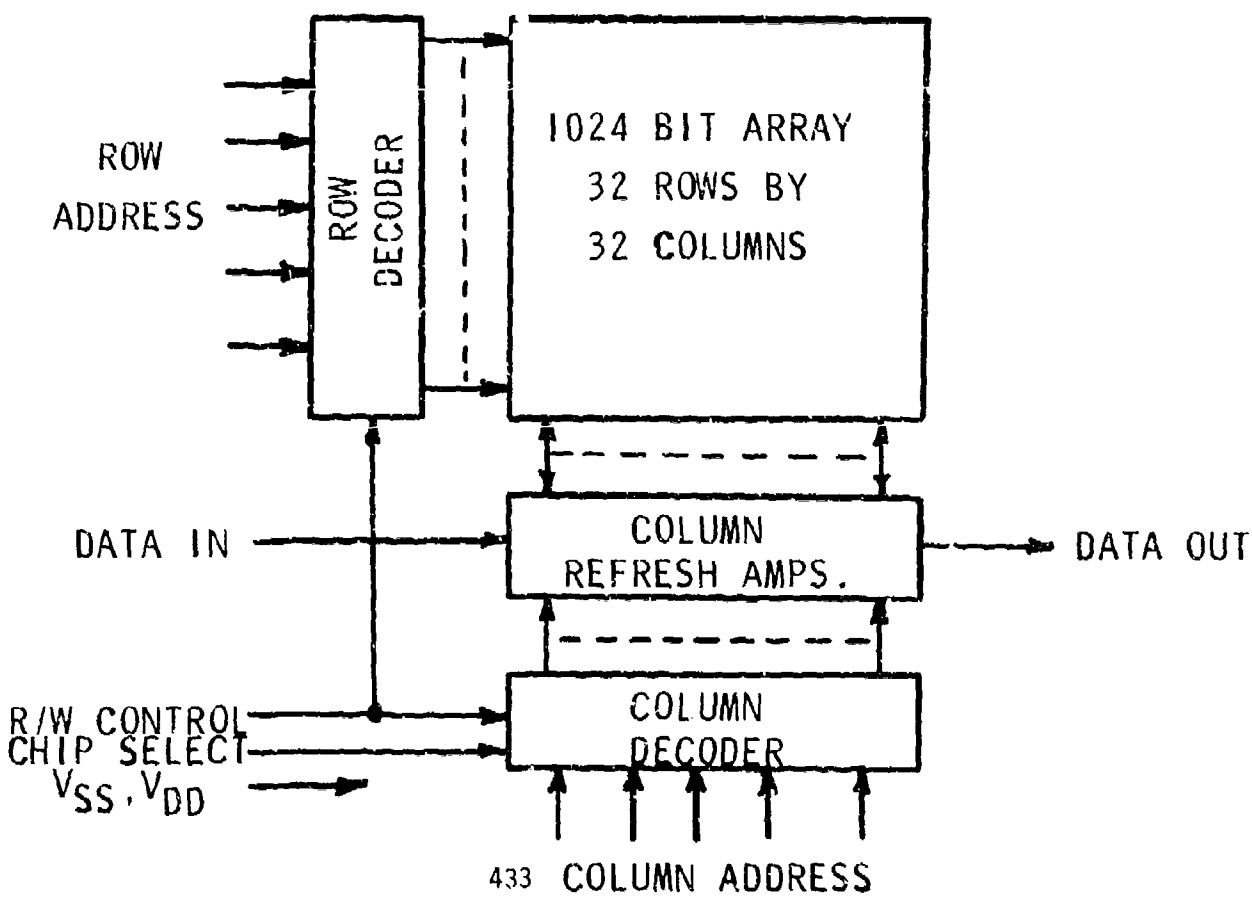
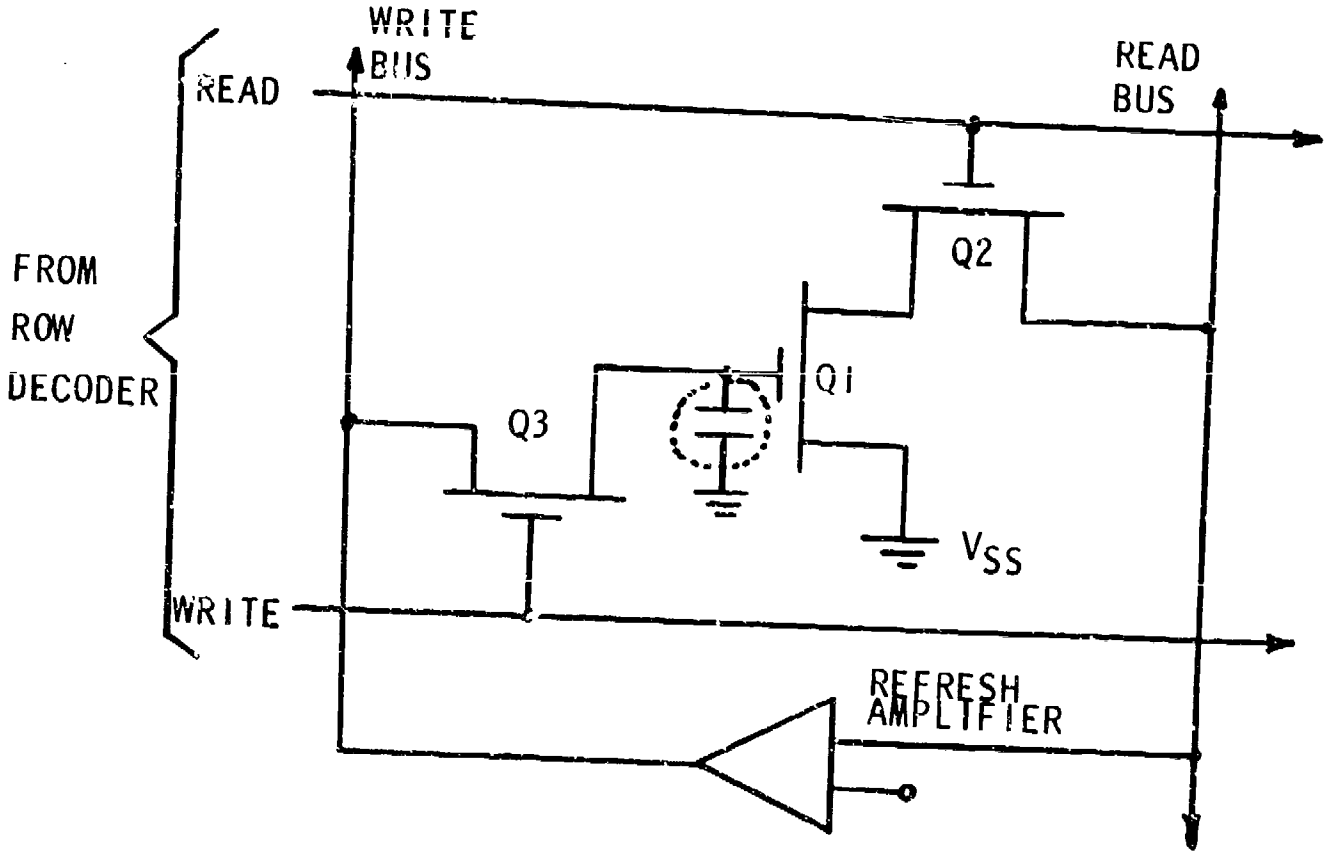


Figure 4. Basic MOS Memory Cell



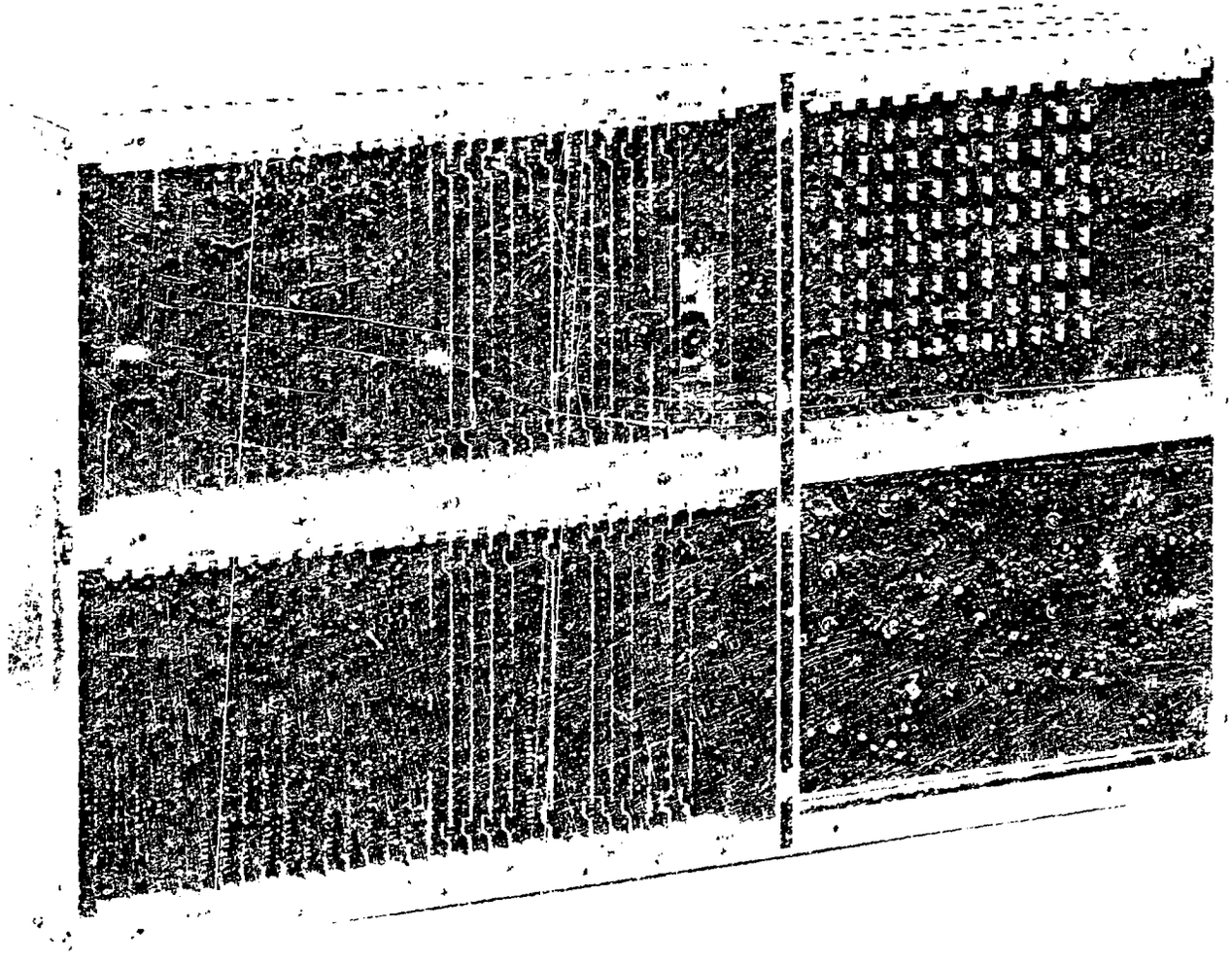


Figure 3. LSI Memory System

Table 1

Characteristics of MOSTEK 4006 Device

Parameter	Characteristic
Technology	Dynamic P Channel MOS; Ion Implantation
Organization	1024 X 1
Voltages Required	+5 ±5% volts, -12 ±5% volts
Access/Cycle Times	400 nsec/400 nsec (READ) 650 nsec (WRITE)
Refresh Period	2 Msec
Input Signals	5 volt level signals
Output Signal	Current sensing required; 1 mA minimum
Maximum Power Dissipation	450 mW (operating); 50 mW (stanby)
Package	16 Pin Ceramic Dip
Specified Operating Temperature Range	$0^{\circ}C \leq T$ ambient $\leq 70^{\circ}C$

Table 2

Characteristics of LSI Memory System

Parameter	Characteristic
Capacity	8192 words X 33 bits; Random Access
Interface	Multiport with Priority Network; Bidirectional Data Lines
Nonvolatility	1 Hour
Operating Temperature Range	$-30^{\circ}C \leq T$ ambient $\leq 70^{\circ}C$
Access/Cycle Time	660 nsec/1.2 usec Read or Write Cycle
Prime Power	270 VDC
Power Dissipation	65 watts (normal operation), 16 watts (data retention) Excluding Converter Losses
Size	Approximately 22" X 6" X 13"
Weight	Approximately 60 lbs.

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